OOPS-ASSIGNMENT

1) What is class in System Verilog and how does it differ from a module?

Ans:

Class:

Class is a user defined data type it is used to implement the oops concepts (inheritance, polymorphism, abstraction, encapsulation) used in testbench to reduce the complicity of verification code, code reusability and randomization.

It contains members and methods to have its logic.

Module:

Module is a synthesizable block used in design side to write the RTL code.

It does not support oops feature.

It contains ports, always block, continuous assignment.

2) How do you instantiate an object of a class in System Verilog?

Ans:

Class creation -> Handle -> Object creation.

Syntax :

Type-1	Type-2

Class_name obj_name; //handle
Obj_name = new(); //object
	Class_name obj_name = new(); //both handle & object

3) Explain how constructors are defined in System Verilog classes and their purpose?

Ans:

Constructors are used to initialize the class members at the time of object creation

Syntax :

```
function new();
        .
        Method logic & members
        .
endfunction
```

4) How are classes used in verification as opposed to modules?

Ans:

Classes are used in verification code it is not synthesisable. Classes supports oops concepts while module not support and module is synthesisable. Class can only be utilized by creating objects inside module block in testbench code.

5) What is the purpose of new method in System Verilog and how does it differ from a constructor?

Ans:

New method is used to create an object of a class which initialize the members with their default values where as constructor inside class will initialize the members of class with the specified format inside the constructor at the time of object creation.

6) What is the scope of a static variable within a System Verilog class and how does it differ from an instance variable?

Ans:

The scope of a static variable is up to the life of the class where as the scope of a instance variable is up to the life of the object.

Static variable are referred to a common location it doesn't change according to the object creation where as instance variable will have new location when ever a object is created.

7) Explain the visibility and lifetime of static variable within a package in system Verilog?

Ans:

The lifetime of the static variable is up to run time of all class objects.

Visibility of the static variable is only for the same package file included block.

8) How a Static Task is Invoked Differently than a Non-Static Task in a System Verilog Class?

Ans: static task can only use static property of the class and non-static class can access both static and non-static variables.