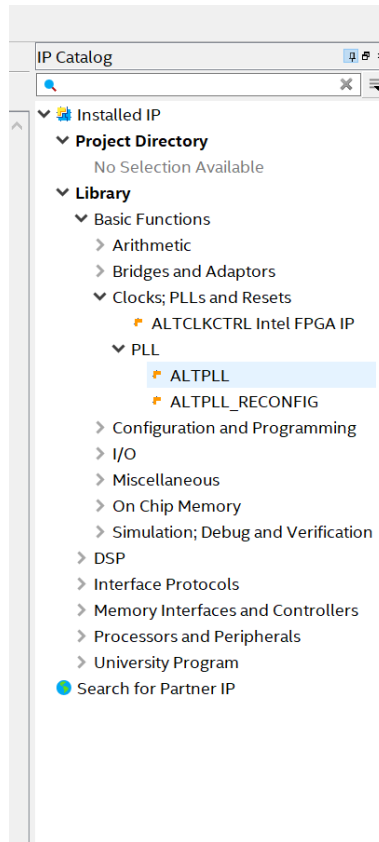


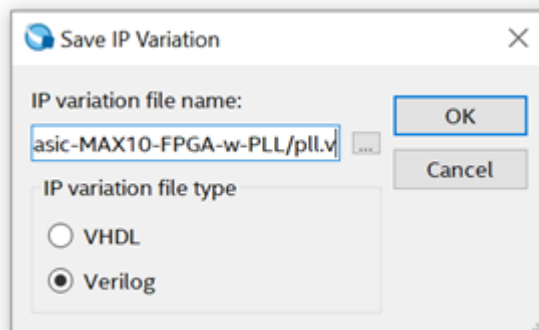
This project needs the ALTPLL IP to be added.

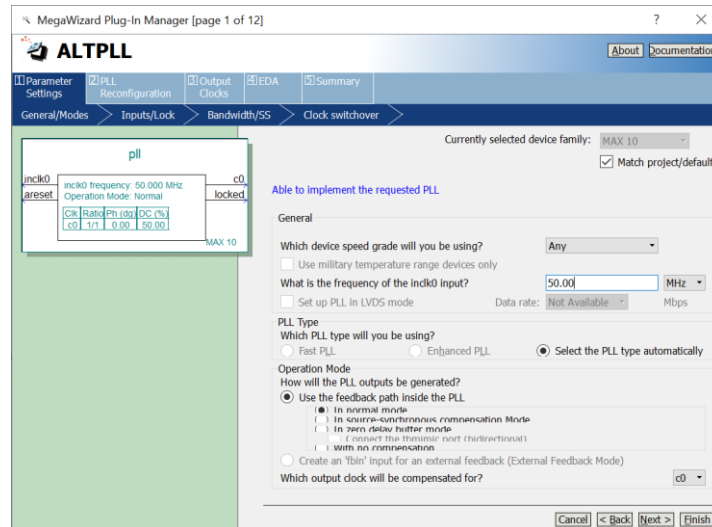
Clock oscillator U15 will provide 50MHz to the MAX10 FPGA which will go through ALTPLL.

To add ALTPLL to the design, go to IP Catalog on the right side of the screen. Under “Clocks; PLLs and Resets” select ALTPLL.



Name the IP variation “pll.v”





Next it brings up the MegaWizard for IP creation.

Set the input frequency to 50MHz (see above)

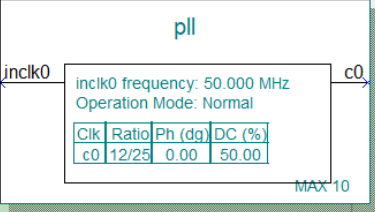
- Uncheck everything on “Inputs/Lock”
- Leave Bandwidth/SS as-is
- Leave Clock Switchover, PLL Reconfiguration as-is
-

MegaWizard Plug-In Manager [page 6 of 12] ? X

**ALTPLL** About Documentation

1 Parameter Settings 2 PLL Reconfiguration 3 Output Clocks 4 EDA 5 Summary

clk c0 > clk c1 > clk c2 > clk c3 > clk c4 >



**c0 - Core/External Output Clock**  
Able to implement the requested PLL

☒ Use this clock

Clock Tap Settings

☒ Enter output clock frequency 24 MHz Actual Setting: 4.000000

☐ Enter output clock parameters:

Clock multiplication factor: 1 Actual Setting: 12

Clock division factor: 1 Actual Setting: 25

Clock phase shift: 0.00 deg Actual Setting: 0.00

Clock duty cycle (%): 50.00 Actual Setting: 50.00

Note: The displayed internal settings of the PLL is recommended for use by advanced users only

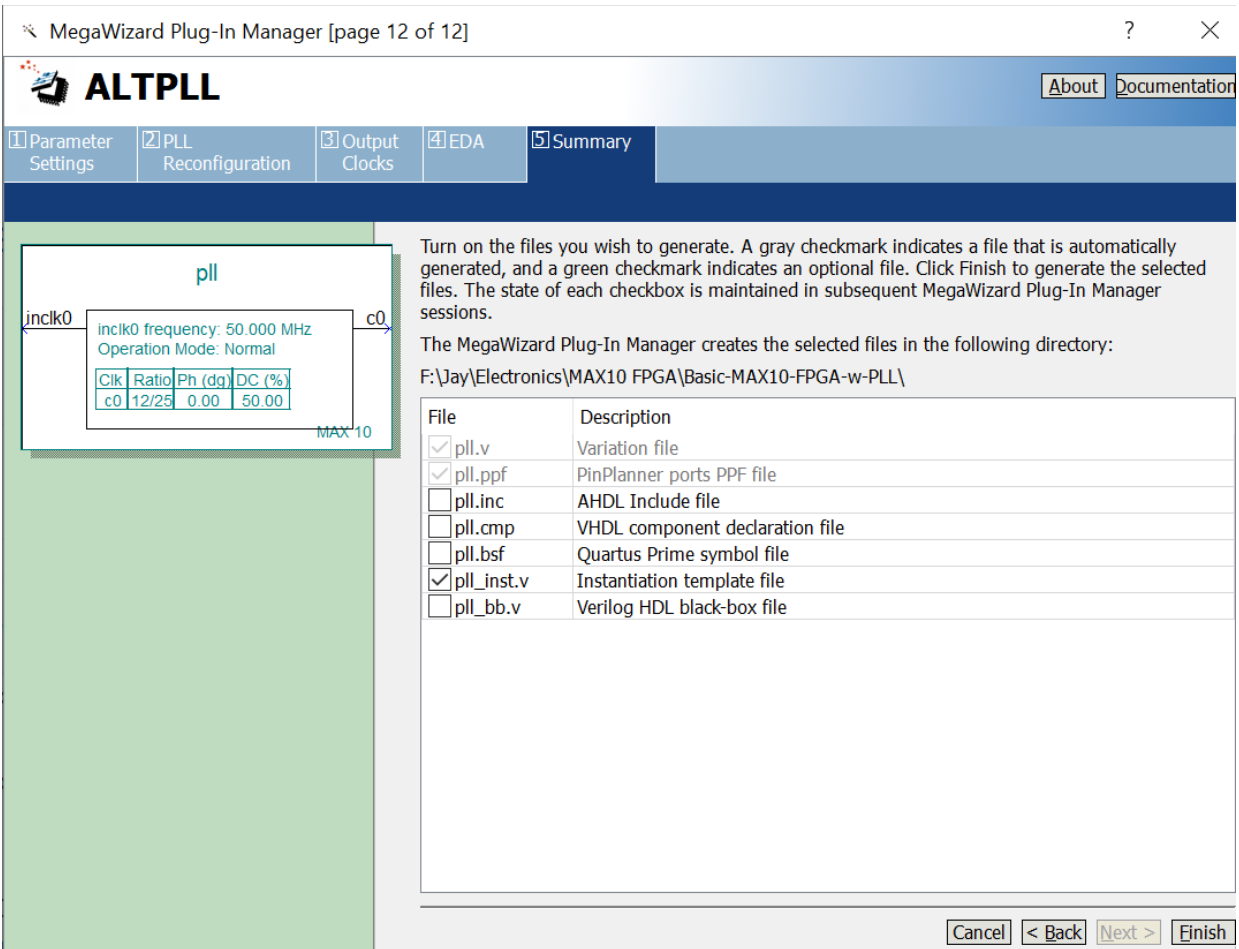
Description: Primary clock VCO frequenc... 6

Per Clock Feasibility Indicator: c0 c1 c2 c3 c4

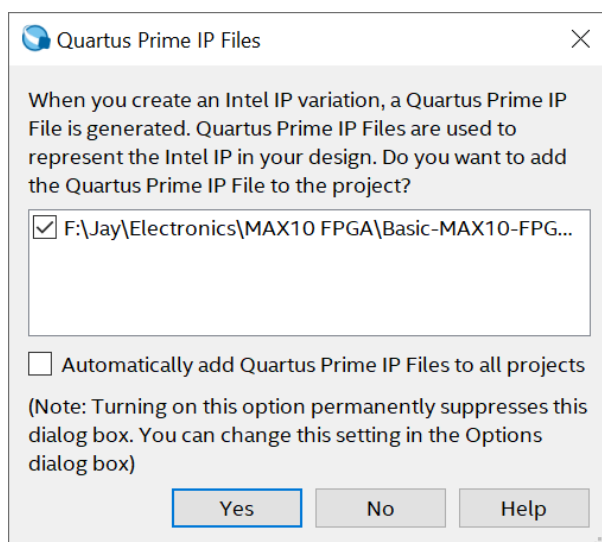
Cancel < Back Next > Finish

Under Output Clocks: C0, check 'use this clock' and click the radio button to select 'Enter output clock frequency' and enter 24MHz under 'Requested Settings'.

EDA tab, just skip,



Under summary check pll\_inst.v Instantiation template file.



Check 'add IP files to project'

When you select 'Hierarchy' you see pll:pll\_inst is added to the design.

Run through compile design as usual.

The screenshot displays the Quartus Prime Lite Edition interface. The top toolbar shows the 'Hierarchy' button (a blue square with a white 'H') being clicked. The 'Project Navigator' on the left shows the design hierarchy: MAX10: 10M50DAF484C6GES, led\_top, ledled\_inst, and pll:pll\_inst. The 'Logic Cells' column shows 47 (1) for led\_top, 46 (46) for ledled\_inst, and 0 (0) for pll:pll\_inst. The 'Compilation Report - led' window on the right shows the source code for led\_top.v, which includes a module definition and an instantiation of pll:pll\_inst. The 'Tasks' window at the bottom shows the compilation tasks: Compile Design, Analysis & Synthesis, Fitter (Place & Route), Assembler (Generate programming files), Timing Analysis, and EDA Netlist Writer, with their respective times.

Entity/Instance	Logic Cells
MAX10: 10M50DAF484C6GES	
led_top	47 (1)
ledled_inst	46 (46)
pll:pll_inst	0 (0)

```
1 2
3 4
5 6
7 8
9 10
11 12
13 14
15 16
17 18
19 20
21 22
23 24
25 26
27 28
29 30
31 32
33 34
35 36
37 38
39 40
41 42
43 44
45 46
```

```
module led_top(
    input INPUT_CLK,
    input reset_n,
    output logic led0, led1
);
    logic clk;

    pll pll_inst (
        .inclk0 ( INPUT_CLK ),
        .c0 ( clk ),
    );

    led led_inst(
        .clk (clk),
        .reset_n (reset_n),
        .led0 (led0),
        .led1 (led1)
    );
endmodule: led_top
```

Task	Time
Compile Design	
Analysis & Synthesis	00:00:07
Fitter (Place & Route)	00:00:06
Assembler (Generate programming files)	00:00:03
Timing Analysis	00:00:02
EDA Netlist Writer	00:00:01
Edit Settings	
Program Device (Non-Programmer)	