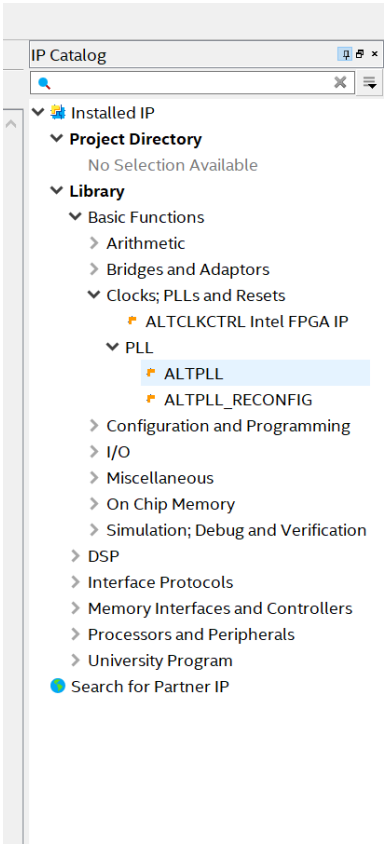
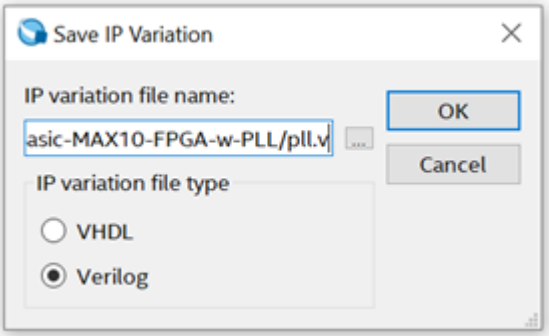
This project needs the ALTPLL IP to be added.

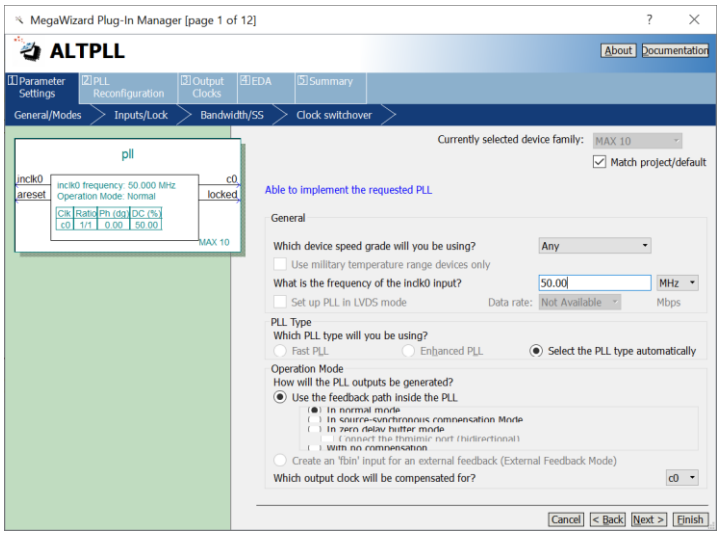
Clock oscillator U15 will provide 50MHz to the MAX10 FPGA which will go through ALTPLL.

To add ALTPLL to the design, go to IP Catalog on the right side of the screen. Under “Clocks; PLLs and Resets” select ALTPLL.



Name the IP variation “pll.v”

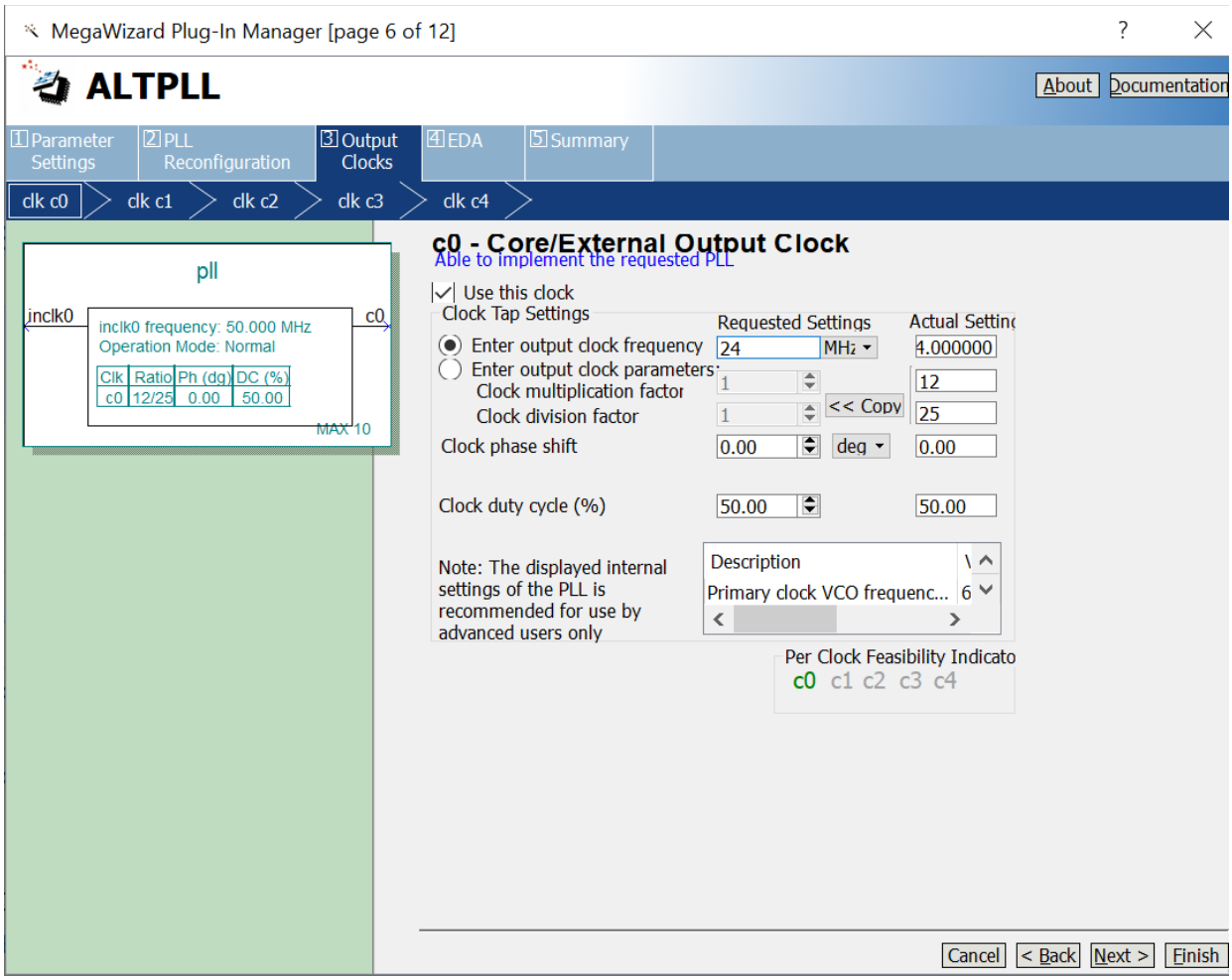




Next it brings up the MegaWizard for IP creation.

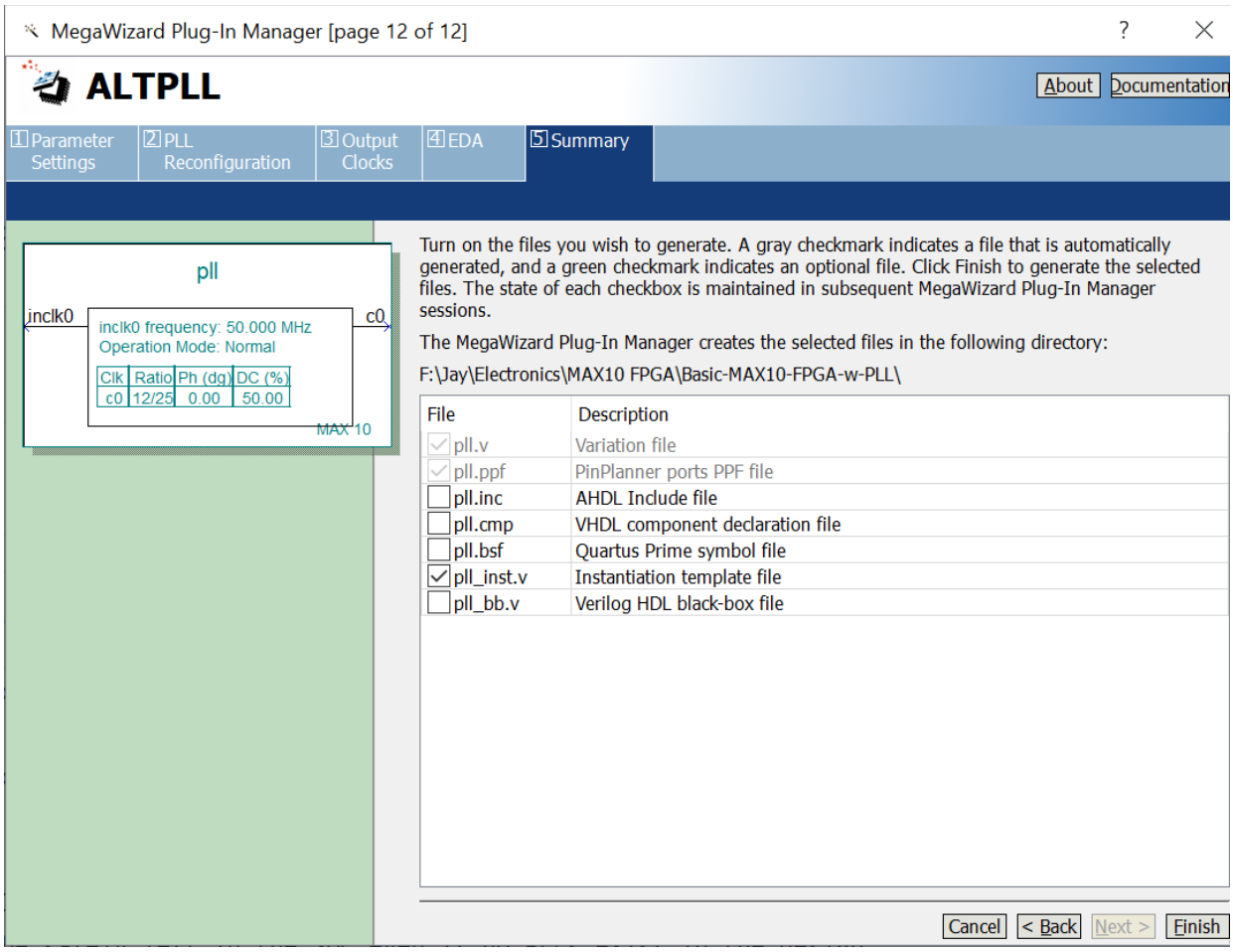
Set the input frequency to 50MHz (see above)

- Uncheck everything on “Inputs/Lock”
- Leave Bandwidth/SS as-is
- Leave Clock Switchover, PLL Reconfiguration as-is
-

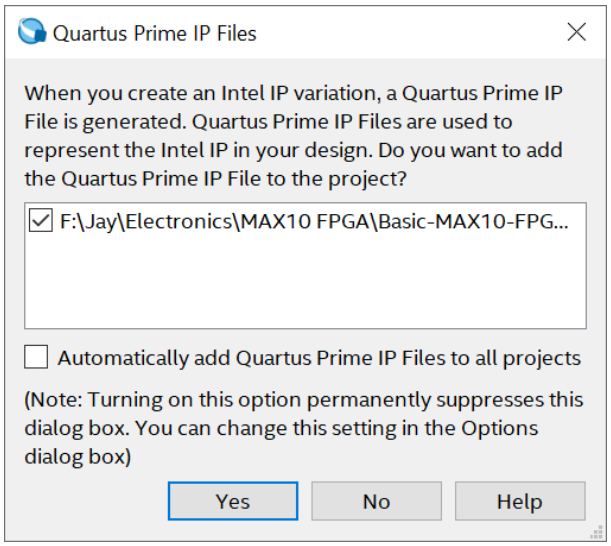


Under Output Clocks: C0, check ‘use this clock’ and click the radio button to select ‘Enter output clock frequency’ and enter 24MHz under ‘Requested Settings.

EDA tab, just skip,



Under summary check pll_inst.v Instatiation template file.



Check ‘add IP files to project’

When you select ‘Hierarchy’ you see pll:pll_inst is added to the design.

Run through compile design as usual.