PDMBRD REV A User Guide

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Features

- Converts analog audio and ultrasound signals to Pulse Density Modulation (PDM) format
- Jumper selection for options
- Accepts analog input signals via 3.5mm stereo jack, SMAs, or jumper wire
- Powered from USB
- On-board voltage regulator

Equipment Required

- USB Micro cable for 5V power
- Analog source
- SMA and/or jumper wires to connect test equipment
- 3.5mm male stereo jack if using audio input
- PDMCLK source/PDMDAT Sink

Description

The BDMBRD REV A board converts analog single channel or stereo audio signals into digital Pulse Density Modulation (PDM) format data using two OnSemi FAN3852 Analog to Digtal Converters (ADCs). The board can be used to characterize and test audio front ends with PDM input for ASICs, FPGAs, and microcontrollers in a controlled manner, to test the effect of clock jitter on PDM audio quality, and as a non-acoustic (quiet) production testing method of machine learning ASIC models which require PDM audio input data. The board is powered by USB Micro and features an on-board ultra low noise regulator to supply power to the ADCs.

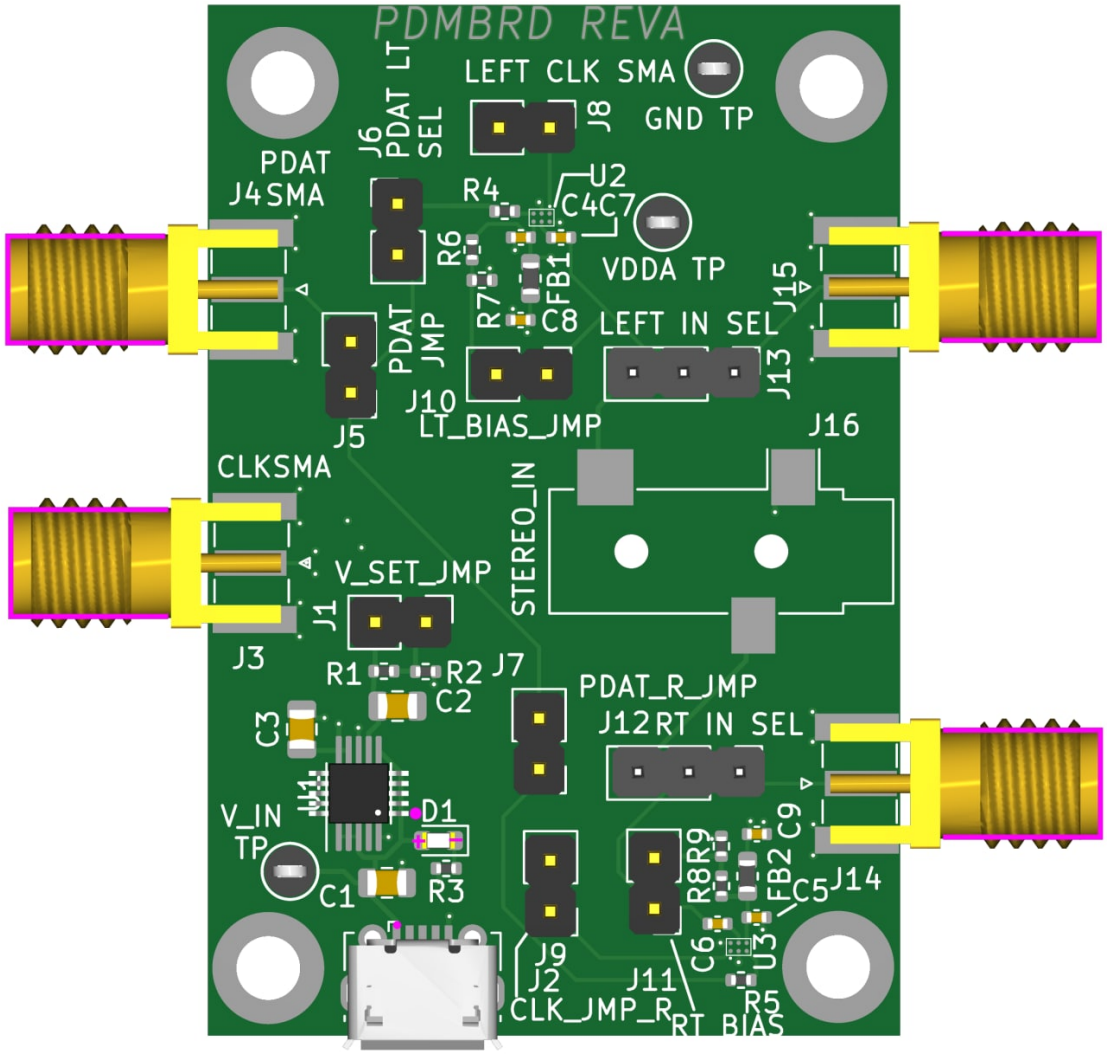


Figure 1
PCB Top Drawing

Refer to Figure 1, above for the PCB Top drawing of the board.

Test Point Listing

Test Point	Name	Description
TP1	V_IN	Test Point for 5V In
TP2	GND	Ground
TP3	VDDA	Test point for 3.3V or 1.8V regulated output

Jumper Listing

Jumper	Name	Description
J1	V_SET_JUMP	Open - set VDDA to 3.3V Closed - set VDDA to 1.8V
J2	USB_B_MICRO	5V power in via USB
J3	CLK_SMA	SMA jack for PDMCLK
J4	PDAT_SMA	SMA jack for PDAT
J5	PDAT_SMA_JMP	Open - J5.1 supplies PDAT via jumper Closed - PDAT supplied to J4
J6	PDAT_L_JMP	Open - Left channel does not drive PDAT Closed - Left channel drives PDAT
J7	PDAT_R_JMP	Open - Right channel does not drive PDAT Closed - Right channel drives PDAT
J8	CLK_JMP_L	Open - Left channel PCLK not driven by CLK_SMA (J3). Use if supplying left channel CLK via jumper wire Closed - Left Channel PCLK driven by CLK_SMA
J9	CLK_JMP_R	Open - Right channel PCLK not driven by CLK_SMA (J3). Use if supplying right ch CLK via jumper wire Closed - Right Channel PCLK driven by CLK_SMA
J10	LEFT_BIAS_JMP	Open - left ADC input not biased. Closed - add bias to ADC See FAN3852 DS
J11	RIGHT_BIAS_JMP	Open - right ADC input not biased.

Jumper	Name	Description
		Closed - add bias to ADC See FAN3852 DS
J12	RT_IN_SEL	J12.2-1 - SMA (J14) ADC input for Right channel J12.2-3 - Audio Jack input for Right channel
J13	LEFT_IN_SEL	J13.2-1 -SMA (J15) ADC input for Left channel J13.2-3 - Audio Jack input for Left channel
J14	RIGHT_SMA	Input for right channel if J12 set to 2-1 and not using J16 audio jack. Useful for connecting signal generators to ADC input.
J15	LEFT_SMA	Input for left channel if J13 set to 2-1 and not using J16 audio jack. Useful for connecting signal generators to ADC input
J16	AudioJack3	3.5mm Audio Jack. J12 and J13 must be set to 2-3 Tip - Left Ring - Right Sleeve -GND

Configuration

Configure the audio input source using jumpers J13 for the left channel and J12 for right channel. J13.2-1 selects J15 SMA input for the left channel and J12.2-1 selects the right channel as SMA input. J13.2-3 selects the left and J12.2-3 selects the right channels for the 3.5mm (⅛”) stereo jack.

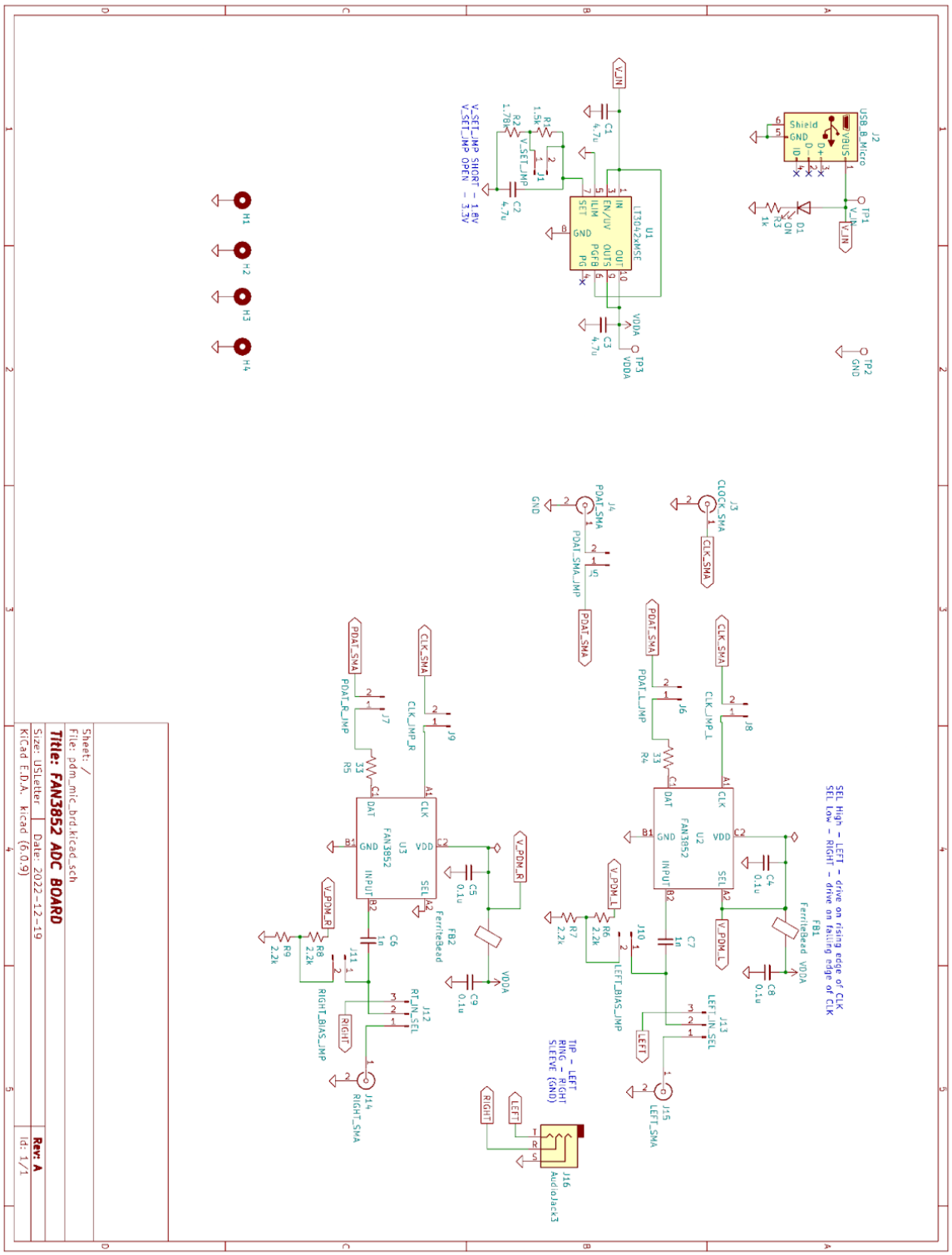
Bias to the ADC inputs, for example when connecting ECM microphones to the left and right channels, can be enabled by shorting J10 for the left microphone J11 for the right microphone. If bias is not required, leave these jumpers unpopulated.

Operation

FAN3852 datasheet figures 5 and 6 show best SNR at -6dB FS which corresponds to 275mV peak to peak (not RMS) with SNR and THD dropping until 0dB FS which corresponds to 550mV pk-pk.

The FAN3852 datasheet lists FCLK min as 1.0MHz however, the ADCs have been tested to work down to at least 768kHz.

Schematic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File: pdm_mic_brd.kicad_sch
Title: FAN3852 ADC BOARD
Size: USLetter
Date: 2022-12-19
KiCad E.D.A. kicad (6.0.9)
Rev: A
Id: 1/1
SEL High - LEFT - drive on rising edge of CLK
SEL Low - RIGHT - drive on falling edge of CLK
TIP - LEFT
RING - RIGHT
SLEEVE (GND)
V_SET_JMP SHORT - 1.8V
V_SET_JMP OPEN - 3.3V

Fabrication

KiCAD files are on the github repo.

To fabricate the board, upload the Gerber .zip file, BOM-pdm_mic_brd.csv BOM and XY file CPL-pdm_mic_brd.csv to JLCPCB

Bill of Materials

Designator	Value	Type	PKG	Vendor	Vendor Part	LCSC	Mouser
C1,C2,C3	4.7uF	Capacitor, X7R	0805	Murata	GRM21BR71E475KA73L	C162427	
C4,C5,C8,C9	0.1uF	Capacitor, X7R	0402	YAGEO	CC0402KRX7R7BB104	C60474	
C6,C7	1nF	Capacitor, X7R	0402	Murata	GCM155R71H102KA37D	C126532	
D1	ON LED	Grn/Yel LED		Yongyu Photoelectric	SZYY0603YG	C434423	
FB1,FB2	FerriteBead	Ferrite Bead	0603	Murata	BLM18AG601SN1D	C19330	
J1,J10,J11,J5 ,J6,J7,J8,J9	2 Pin Jumper	2x2.54mm		ZHOURI	2.54-1*2	C5116481	
J12,J13	3 Pin Jumper	3x2.54mm		HCTL	PZ254-1-03-Z-8.5	C2894926	
J14,J15,J3,J4	SMA	Coax Conn		Shenzhen Kinghelm Elec	KH-SMA-KE8-G	C530661	
J16	3.5mm Jack	Audio Jack		CUI	SJ-3523-SMT-TR		490-SJ-3523-SMT-TR
J2	USB_B_Micro	USB Micro		MOLEX	1050171001	C505111	
R1	1.5kΩ	Resistor	0402	YAGEO	AC0402DR-071K5L	C226693	
R2	1.78kΩ	Resistor	0402	YAGEO	AC0402DR-071K78L	C226695	
R3	1kΩ	Resistor	0402	UNI-ROYAL	0402WGF2001TCE	C4109	
R4,R5	33Ω	Resistor	0402	UNI-ROYAL	0402WGF330JTCE	C25105	
R6,R7,R8,R9	2.2kΩ	Resistor	0402	YAGEO	RC0402FR-072K2L	C114762	
TP1	V_IN	Test Point		Keystone	5002	C238123	
TP2	GND	Test Point		Keystone	5001	C238122	
TP3	VDDA	Test Point		Keystone	5003	C238124	
U1	LT3042xMSE	LDO	MSOP-10	ADI	LT3042EMSE#TRPBF	C461518	
U2,U3		PDM ADC		OnSemi	FAN3852UC16X		863-FAN3852UC16X

Revision History

Date	Revision	Description
12/24/2022	0.1	Initial Version