Unit 4 Buses

Structure:

4.1 Introduction

In the previous units we discussed about many important components of the computer system like memory, CPU, motherboard, memory slots, etc., which are required for a computer? But, when you have various important components together the question arises as to how they could be linked and communicated between each other so that the data in the form of information or address of the memory location can be transferred. This question is answered by the use of electric wires. These are called Buses. Specifically *Bus* is an electric cable or collection of cables that are used to transfer the data, information or the address of the memory location. In this unit we will discuss the importance of this data travelling agent and list the different types and parts of the Bus. We will explain the importance of AGP

and help you to use of expansion Buses to connect the expansion devices. IBM came to a conclusion that connecting the expansion elements which are required and leaving the other functions of the expansion devices which can connect with the plugin through the Bus was a feasible choice.

Objectives:

After studying this unit you will be able to:

- Define a Bus.
- Identify a Bus in the computer system
- Classify and explain the different types of Bus in detail.
- Differentiate between the types of Bus
- Resolve the basic Bus problems through troubleshooting

4.2 BUS

As we discussed above Bus is a collection of cables that is used to communicate between two or more components of the computer system. Bus consists of three major types such as address Bus, data Bus and control Bus. Address Bus is the one which carries the formation of the location of the information. Data Bus is the one which carries data between the different components of the computer. Control Bus is the one which allows transferring the control instructions from CPU to memory or I/O devices. A typical diagram of the connectivity of the Buses is as shown in the figure 4.1. In this figure you can observe that the data Bus allow two way transfers between CPU, I/O and the memory. Address Bus and Control Bus allow only the control flow from CPU to I/O and memory.

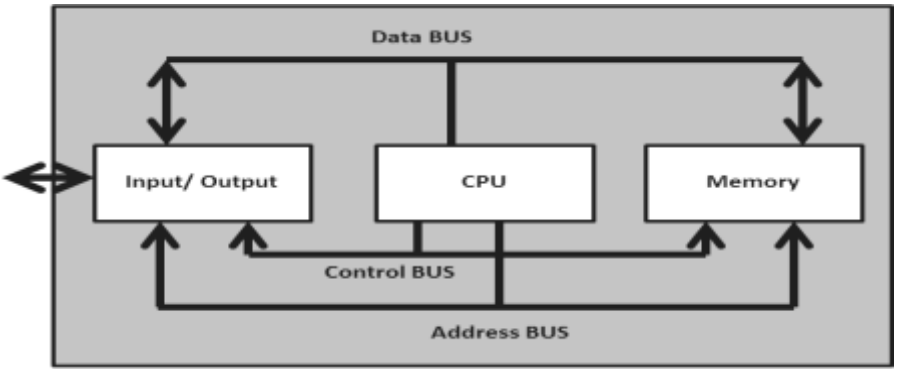

Figure 4.1: Bus connection

The control Bus helps in performing the specific operations by the respective devices. Address Bus is used to send and specify the address of the specific location. The data bus is used to transfer instructions from memory to the CPU for execution. It carries data to and from the CPU and memory as required by instruction translation.

All Buses are measured in terms of clock speed and measured by MHz. Width specifies the amount of data transferred in one time. For example 8 bit Bus can transfer 8 bit data. Buses are connected to number of devices which are working at different speed, some are faster and some or slow. When the devices operates which can perform slower than other devices cannot send or receive the data. Therefore clock speed needs to set so that all the devices interact with each other at same speed. A Bus is also called as backbone because it connects the computers through one cable.

As discussed in unit 3 sections 3.2.2 most of the CPUs use the expansion slots to connect the add-on rather than connecting the extended device. Expansion Buses are used to connect the system with the peripheral devices like printer, monitor, scanner, etc. This has made the PC a flexible machine that can be configured to the requirement of the external devices or add-ons. This has given rise to different types of Buses. In order to make the application execution faster and the transfer of data bits faster, *fast Bus* is used. *Local Bus* is used to directly connect the data transfer to the CPU.

Buses can be *serial* and *parallel*. *Serial Buses* are those which allow the data to travel in single bit-serial form. *Parallel Buses* are those that allow data transfer in multiple wires in a parallel form. Based on the type of Bus used with the particular devices as mentioned above Bus can be *unidirectional* and bidirectional. Unidirectional Buses allow data transfer from one device to another in one way path. For example control Bus allows transfer from CPU to I/O and Memory and not backward. *Bidirectional Buses* allows data to travel through it from one device to another in both the direction. For example data Bus allows the data to travel to and from the CPU to I/O and memory. *Internal* and *external Buses* are used to connect the internal and external devices. *Internal Bus* allows connection between internal components like sound card and CPU. *External Bus* allows the connectivity between any external devices like USB. Therefore different architectures were designed to support the different kinds of Buses and the

computer system and its components. Generally with respect to this kind of architecture, the Bus has been divided into three major types. They are *ISA, PCI* and *AGP*.

Self Assessment Questions

1. _____ is the electric wire that is used to answer the question of linking and communication between different components.
2. State whether the following statements are true or false:
   a. Control Bus is the one which carries data between the different components of the computer.
   b. Local Bus is used to directly connect the data transfer to CPU.
3. Buses are measured in terms of _____ and measured by _____.
4. _____Buses are used to connect peripherals.
5. The three major types of Buses are _____, _____ and _____.

4.3 Industry Standard Architecture (ISA)

As you have already studied meaning of ISA in unit 3 section 3.2.2 we will directly discuss on the architecture of ISA. Industry Standard Architecture Buses were also referred to as PC Buses. The use of standardized Buses helped to support the operating system and many application software. ISA made a path to the manufacturers to produce faster and supportable PCs and expansion devices. Depending upon the architecture used by the processor two versions of ISA was used.

They were:

- 8-Bit ISA
- 16-Bit ISA

4.3.1 8-Bit ISA

8-bit ISA was used by PC/XT Bus. The PC/XT is commonly referred to as the XT, was IBM's successor to the original IBM PC. XT stands for extended technology. The XT was designed to serve the enhanced machine for commercial purpose.

8-Bit ISA was the original ISA found on IBM machines which was 8 bits wide indicating the 8 bit data of the 8088 processor. 8-bit ISA consisted of 62 pins

out of which 20 address and 8 data lines were available. It ran with a speed of 4.77 MHz. Diagram of Simple 8-bit Bus is given below in figure 4.2

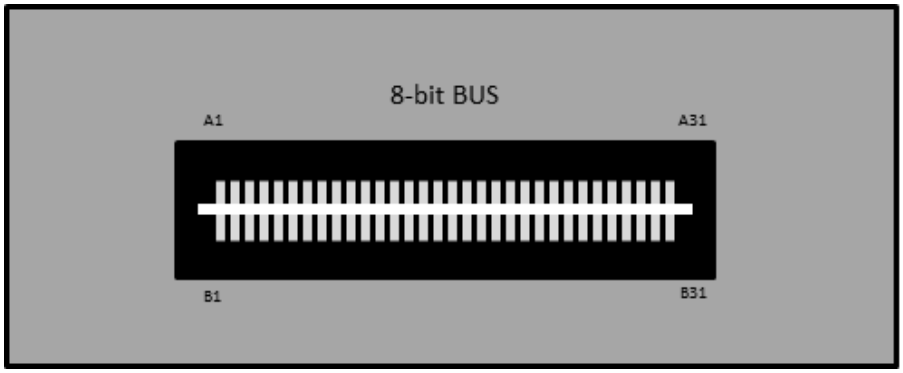

Figure 4.2: Diagram of 8-Bit Bus

The 8-bit ISA Bus consists of single card edge connector with 62 pin contacts. The Bus provides 8 data lines and 20 address lines which allow the board to be placed in the conventional memory. The Bus supports connection for 6 interrupts (IRQ2-IRQ7) and three DMA channels (DMA0-DMA2).

All though each connector on the Bus is supposed to work in the similar fashion, the PC which is designed with eight expansion slots requires any card inserted in the eighth slot to provide a special signal called “card selected” on pin labelled B8. Timing requirement for the eighth slot are also tighter.

Interrupts and DMA (Direct memory access) channels are supported by this Bus. The table below shows the DMA channel that has expansion with its specific standard function. An *interrupt* is an event in hardware that triggers the processor to jump from its current program counter to a specific point in the code. DMA channels are system pathways used by many devices to transfer information directly to and from memory.

Table 4.1: DMA channel expansion

DMA Channel	Expansion	Specific function
0	No	It can refresh dynamic RAM
1	Yes	For Add-on cards
2	Yes	Floppy disk controller
3	Yes	Hard disk controller

The oscillator pin in both PC/XT and PC/AT ISA Bus configuration provides the system oscillator signal to the expansion Bus. An oscillator is a circuit which creates a waveform output from direct current input. When the PC needs to be reset, the RESET DRV pin drives the whole system into the reset state. The 20 address pins connects an expansion board to the system address Bus. When address signals are valid, the Address Latch Enable (ALE) signal indicates that the address may now be decoded.

When errors occur on the expansion board the -I/O channel Check (-I/O CHCK) signal applies flags to the mother board. The minus sign before the signal indicates that the active low logic is used in the signal. The 6 hardware interrupts are IRQ2, IRQ3, IRQ4, IRQ5, IRQ6, and IRQ7 which are used by the expansion board to seek the attention of the CPU. Interrupt 0 and 1 handles the high priority of the timer chip and keyboard. Therefore these interrupts will be busy handling timer chip and the keyboard and it is not available to the Bus.

4.3.2 16-bit ISA

16-bit ISA is an expansion of 8-bit ISA with the connection of 36-pin connector added along with the 62-pin connector as add-on. 8-bit Bus is replaced by 16-bit Bus by doubling the number of data bits and adding pin connectors. 16-bit was used in PC/AT Bus. The IBM Personal Computer/AT are also called as PC AT or PC/AT, was IBM's second-generation PC, designed around the 6 MHz Intel 80286 microprocessor and released in 1984 as machine type 5170. The name AT stands for "Advanced Technology", and was chosen because the AT offered various technologies that were then new in personal computers. . This diagram of 16-bit Bus is as shown in the figure 4.3

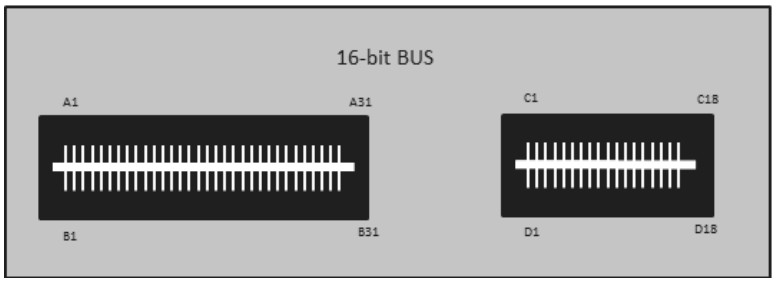

Figure 4.3: diagram of 16-bit Bus

The diagram consists of 62 pin connector of 8 bit Bus and an additional 36 pin connector is used with label C and D. An extra 8 bits were used to normalize the total 16 bit data bus. These 8 bits didn't have any effect on the working of the 16-bit Bus. The table shows the pin assignments of a 32 pin connector.

In addition to 8-bit data, 16-bit Bus consists of extra 8 bits, five interrupts and three DMA channels. One extra bit is used for +5dc volts which is not included in number of bits. It is also added with four additional address lines. The speed is increased from 4.77 MHz to 8.33 MHz.

You should observe that though in ideal situation PC/XT should run on PC/AT expansion slots, it is far from reality with most of the older version of XT slots.

Therefore there was an idea of mixing both 8-bit Bus and 16-bit Bus architecture which consist of 32-pin connector and could be expanded without starting from scratch for the sake of expansion. Now, ISA Bus architecture has retired since most of the systems are adopting PCI and AGP architecture.

Self Assessment Questions

6. _____ Buses are also called as PC Buses.
7. The two versions of ISA are _____ and _____.
8. 8-bit ISA was used by _____ Bus.
9. 8-bit ISA consists of _____ pins out of which of _____ and _____ are address and data liens respectively.
10. 16-bit Bus consists of extra _____ bits, _____interrupts and _____ DMA channels.
11. The speed is increased from _____ to _____ MHz.

4.4 Peripheral component Interconnect (PCI)

As you have already studied meaning of PCI in unit 3 section 3.2.2 we will directly discuss on the architecture of PCI. Graphics processing cards became difficult to process with 32-bit Bus processors with 8.33 MHz speed. During the development of versions there were two architectures which were merged and named as VL and PCI. VL stands for VESA Local Bus. (VESA) Video Electronics Standards Association local bus acted as high speed path for DMA and memory mapped I/O. This is different from ISA Bus as ISA Bus handles interrupts and port mapped I/O.

The disadvantage with VL was its Bus performance was dependent on CPU speed. The manufacturer failed to give the standard specifications.

PCI was developed in mid-1992 by the integration of Intel and a group of manufacturers. In section 4.4.1 and 4.4.2 you will study about the configuration, layout and signals of PCI.

4.4.1 PCI configuration

PCI is a vast improvement over ISA Bus architecture with the increase in its speed from 8.33 MHz. to 33 MHz frequency. This increased the data transfer from 5MB/Sec to 132MB/sec. Another important characteristic was that it gave automatic configuration property to the switches and peripherals. This feature also automatically adjusts the interrupts requests, DMA assignments, the addresses of the requests and data used by the PCI peripheral. The following are the features supported by PCI Bus which are used today.

- Linear Bursts: whenever memory sends data to the peripheral devices it will be in linear address order. *Linear Burst* is a method of continually filling the data line in the Bus by transferring the data. Linear address order is the process of increasing the next byte in the order which read or write the large amount of data into the single address. This is the important feature of PCI. This helps in increasing the performance rate of PCI when compared to Bus which does not have linear burst capability by almost double the time.
- Low access latency: *access latency* is the time taken by the CPU to permit the request access by the peripheral for its control. Reducing this time increases performance of the PCI. Since this kind of expansion slot

support lower access latency the system can easily send the data to the CPU.

- Bus mastering: Bus mastering is a feature of PCI which helps in any intelligent peripheral to have a control of the Bus which is used in boosting the throughput of the architecture. This supports in handling the task according to the priority base. The high priority task can be handled and throughput can be increased.
- Concurrency: when a processor chip works with BUS masters simultaneously rather than waiting for them to complete, the process is called concurrency. Wait state may be sometimes zero at the time of concurrency
- Dual voltage architecture: *dual voltage* features expects two different voltages to be supported. PCI Bus supports +5 volts as well as +3.3 volts which are called as low voltage mode.

4.4.2 PCI Bus Layout

For any architecture there must be proper borders and boundaries. This is given to the PCI architecture by their layout. The layout of the figure to show How it is arranged is given in figure 4.4.

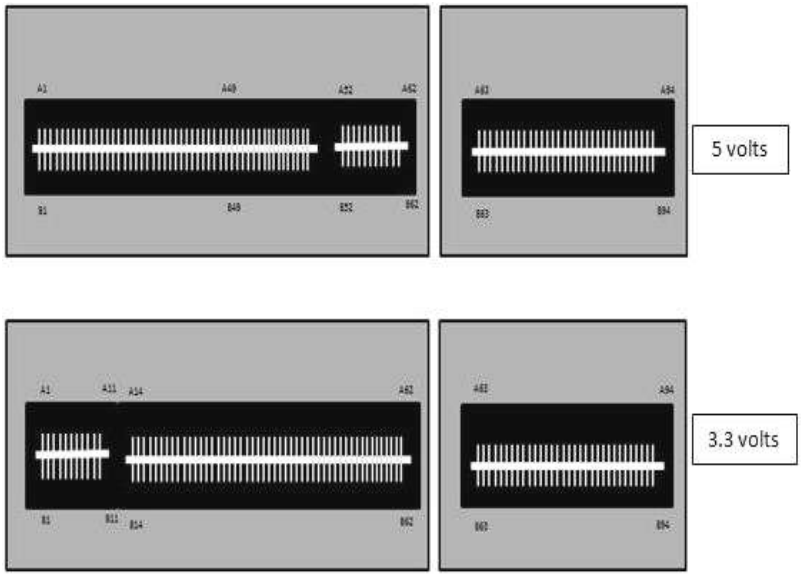

Figure 4.4: PCI Bus layout

In the figure it is observed that +5 volts connector is divided into two segments. A +3.3 volts connector is added with a key at the 12th position of

the Bus just to avoid any insertion of the +5 volts board to +3.3 volts Bus.

A +5 volts connector is added with a key at the 50th position to avoid the wrong insertion of +3.3 volts board into the +5 volts slot.

In general the same system resources cannot be used by the other devices. This is an exemption is PCI. PCI Bus has its own internal interrupts which handle the requests on the BUS. To avoid the confusion PCI Buses are named as A1, A2, A3,……., B1, B2, B3, …….. C1, C2, C3,…… and D1, D2, D3,…….. PCI uses a technique which holds the signal dynamically and whenever there is a requirement it can be reassigned. This technique is called Interrupt ReQuest (IRQ). IRQ can be shared by two or more PCI devices. These IRQs can be accessed during CMOS setup routine.

4.4.3 PCI signals

There are various signals which serve different functions in the PCI Bus. The PCI configuration is differentiated as asynchronous and synchronous based on the dependence of the FSB speed. FSB stands for Front sided Bus which is responsible for data transfer between CPU and one of the two chips of the Core logic chipset on the mother board. An asynchronous configuration is found in the latest motherboards whose PCI speed can be set independent of FSB.FSB derives the Bus clock of the PCI. You can see some of the signals below in the table along with its functions**.**

Table 4.1: The function of PCI signals

Signals	**Functions**
Clock signal	Provides timing for the PCI Bus It can be varied from 0Hz to 33 MHz
Reset Signal	Reset all PCI devices
Command/-Byte enable signal	Defines which of the bytes are transferred
Parity/PAR64 signal	Represents the Parity across address/data and byte enabled lines
-Request (-REQ) signal/line	Initiates the Bus mastering
-Grant (-GNT) signal/line	Approves the Bus mastering request

-Frame Signal	Clock Frame is driven true when valid PCI Bus cycle is in progress.
Target Ready (-TRDY) signal	Target Ready signal is driven true, if within the given Bus cycle the device is able to complete the transaction
Initiator Ready (-IRDY) signal	Indicates that the Bus is ready to accept the data or confirms that the data in the Bus is valid.
Stop (-STOP) signal	This indicates the initiator to terminate or halt the current data transfer.
Initialization Device Select (IDSEL) signal	This also works as Chip select during read and writes transaction of PCI configuration.
Device Select (DEVSEL) signal	As an Input, it has to indicate the current transfer status to know whether it has assumed the control As an output, it has to find out itself as the target for current Bus transfer.
Lock (-LOCK) signal	Prevents the other initiator to modify the locked addresses or selected expansion device.
Primary and secondary error reporting (PERR and SERR)	Reports data parity errors and address parity errors in the PCI BUS.

Self Assessment Questions

12. _____ is a high speed intelligent Buses
13. State whether the following statements are true or false.
    a. In VL architecture the performance of the Bus is independent of CPU speed.
    b. PCI gave automatic configuration property to switch and jumper-less peripherals.
    c. Linear bursts helps in increasing the performance rate of PCI when compare to Bus which do not have linear burst capability by almost double the time.
14. _____ is the time taken by the CPU to permit the request access by peripheral for its control.
15. _____ is the technique which holds the signal dynamically and wherever there is a requirement it can be reassigned.
16. _____ derives the Bus clock of the PCI.
17. FSB stands for _____.

4.5 Accelerated Graphic Port (AGP)

AGP stands for Accelerated Graphics Port which is designed to provide throughput demands of 3 D graphics. The growth in the field of computer science and engineering gave a significant improvement in the PC. The visualization of the information is improved in its quality in colour depth resolutions and wide range of special effects which creates the requirement of more storage place. This is not only demands for more memory but also requires huge bandwidth for data transfer. This was fulfilled by Accelerated Graphics Port (AGP) which is well applicable for 3D applications.

You can visually experience the life like realism with the use of 3D images. AGP helps you to accelerate between the text and 3D images and the PCs graphic controller will be coordinating with the system memory to store and transfer the graphics data. AGP has many additional characteristics which make AGP a useful technology for graphics. The following are the characteristics of AGP.

- It accelerates graphics performance by giving high speed Bus
- Graphic controller is enabled
- Helps in speeding up the data flow from CPU to graphics controller. In this case the data is about the decoded data of video.
- It provides high bandwidth

Structure of AGP

Since the AGP's performance is directly proportional to the bandwidth, the device is fixed in such a position that increases the bandwidth. An architecture is developed which act as an interface between chipset and graphic controller. The architecture is as shown in the figure below:

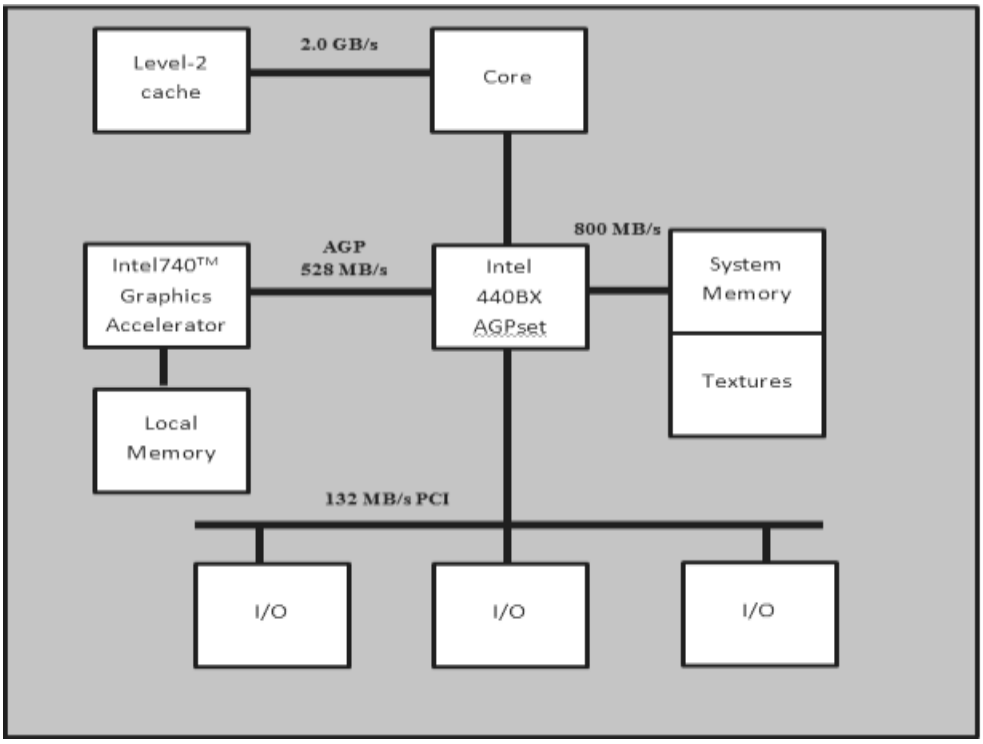

Figure 4.5: Block diagram of AGP architecture

The AGPset is used to accelerate the graphic performance and is directly connected to the system memory through a dedicated high speed Bus. 3D texture data is provided to the AGPset through the system memory. AGP enables the hardware called as graphic accelerated controller to execute texture maps directly from system RAM or local memory. An AGP interface is placed between PC's chipset and graphic controller which helps in increasing the bandwidth. The graphic accelerator controller and the AGPset is connected through AGP Bus. This AGP helps to speed the flow of decoded video from the AGPset to the graphic controller and vice-versa. Another dedicated high speed Bus is connected to L2 cache through the core data controller. In addition to the conversion of texture mapping, offloading this tremendous data overhead from the PCI Bus leaves PCI free to handle drive data transfers and other I/O controllers.

With the help of AGP that offers the bandwidth which is twice the bandwidth of PCI, 2 bytes of data can be made to pass through the AGP CLOCK with a bandwidth of 532 MB/s. More refinement or adjustment to the AGP handles

the data and allow 4 Bytes to be passed with the bandwidth of more than 1 GB/s on every AGP clock. This means that the bandwidth is doubled when the AGP clock refines the data byte.

4.5.1 AGP vs PCI

Before studying the difference between AGP and PCI we should throw a glance on its similarities. Both Buses use at least one PCI slot. AGP was not created to replace PCI, but to create a new dedicated Bus which is used to help the graphic cards functioning.

The important feature of AGP specification is that a 32-bit AGP will easily fit into PCI configuration. But still there are many features which differentiate AGP from PCI with advance advantages.

They are:

- The bandwidth capacity of AGP is 4 times greater than PCI with pipelining or super-pipelining features.
- AGP supports optimized 3D graphics
- AGP uses clock speed up to 66 MHz where the PCI used a fixed clock speed of 33 MHz.
- AGP makes multiple requests for the transaction and PCI will make only one request at a time and wait until the earlier requests are executed completely.
- There is no sharing of bandwidth with other devices in AGP whereas PCI shares it with other devices.

The result of the significant improvement and additions in 32-bit AGP intended in optimising for high performance 3D graphics. The most important difference is the clock speed. The PCI users fixed 33 MHz Bus whereas the clock speed of AGP varies up to 66 MHz.

The basic comparison between PCI and AGP has been shown in the below table.

Table 4.2: Comparison between PCI and AGP

PCI	AGP
Address/data is multiplexed	Address/data is de-multiplexed
Non pipelined	Request is pipelined
Data bytes will be high at 133 MB/s with 32 bits	Data bytes will be peak at 533MB/s with 32 bits

Multiple target and multiple master	Single target and single master
Connected to the entire system	Connected to only read/write memory. this is not connected to I/O operations
There is High/low priority queues	No priority queues

4.5.2 AGP layout

AGP is used on ATX and NLX machines. NLX (New Low Profile Extended) was a form factor proposed for low profile, low cost, mass-marketed retail PCs. NLX specification defines the motherboard size, hole mounting locations, riser card location, and maximum component heights on motherboard. It has three variations 3.3 V, universal and 1.5V. Though the signal layout is similar the key locations are different. Therefore, these cards arenot interchangeable. While checking compatibility between video card and the motherboard In AGP you can ignore the speed multiplier as it is negligible and interchangeable. The table below will help you in understanding the important functions of the different graphics card.

Table 4.3: AGP cards and its functions

AGP card	Type of connector	Description
3.3V Card	3.3V slot	It Supports 3.3V signalling and has the available speeds1x, 2x.
1.5V Card	1.5V slot	It Supports 1.5V signalling and has the available speeds1x, 2x, 4x.
Universal Card	Double slotted	It Supports 3.3V and 1.5V signalling and has the available speeds 1x, 2x at 3.3V and 1x, 2x, 4x at 1.5V.
3.0 Card	1.5V slot	It Supports 0.8V signalling and has the available speed4x, 8x.
Universal 1.5V 3.0 Card	1.5V slot	It Supports 1.5V and 0.8V signalling and Available speeds are 1x, 2x, 4x at 1.5V and 4x, 8x at 0.8V.
Universal 3.0 Card	Double slotted	Supports AGP 3.3v, 1.5V, and 0.8V signalling. Speeds available are 1x, 2x at 3.3V and 1x, 2x, 4x at 1.5V and 4x, 8x at 0.8V.

Note that different slots will have different key positions in the card.

4.5.3 AGP signals

In order to work in an advance performance mode the full bandwidth needs to be utilized and with the Bus is queued by the target. The following are some of the signals which helps in operating the AGP card by asserting them.

Table 4.4: AGP Signal and its functions

Signal	Function
PIPE #	This request is asserted by the current master It indicates that the target has to queue up the full width request.
Read Buffer Full signal (RBF#)	Indicates whether the pre-requested low priority read data can be readily accepted by the Master. Once RBF# is asserted, the arbiter cannot initiate the request of taking back the low priority read data to the master.
Write Buffer Full signal (WBF#)	Indicates Whenever there is data keying from the core program to ensure that whether master is ready to accept the data Once WBF# is asserted the arbiter cannot initiate the request to provide data.
GNT#	Indicates that the signals have some meaning to the master
FRAME#	Indicates the output form the core logic
AD Bus Strobe 0 signal (AD_STB0)	2x data transfer mode on address line is provided Data providing agent drives this signal
SideBand Strobe signal (SB_STB)	Timing for SBA is provides and driven by AGP master
CLOCK (CLK)	Provides timing for both AGP signals

Clock divisors help in under clocking or overclocking the FSB in the motherboard. Wider range of FSB gives greater variety of clock divisors.

Self Assessment Questions

18. _____ Port is applicable for 3D applications.
19. State whether the following statements are true or false
    a. Performance of AGP is directly proportional to the bandwidth
    b. The bandwidth capability of AGP is 4 times greater than PCI
    c. RBF# indicates the pre-requested low priority read data can be readily accepted by the master.
    d. GNT# indicates that the Whenever there is data keying from the core program to ensure that whether master is ready to accept the data
20. AGP is used on _____ and _____ machines.

4.6 Front Sided Bus (FSB)

FSB stands for Front Sided Bus and used to connect CPU to the computer system and CPU with the various other components of the system. FSB is two directional flows of data. It means various components send and receivethe data from the processor. FSB is also called as processor Bus because its acts as a main path for the data flow from processor to other parts of the motherboard. The speed of FSB ranges from 66MHz, 100 MHz, 133 MHz, 266MHz, 400MHz and above. This is one of the most important considerations while buying motherboard.

The important feature of the FSB is its bit size. It is observed that 32 bit FSB performs 100% more than that of 16 bit FSB. Therefore the measure of data transfer delivered in one tick (part of 1 CLOCK cycle) is an important consideration of FSB.

The communication between various components is done by FSB through the Chipset. The chipset consists of two processors namely *Northbridge* and *Southbridge*. Both the bridges act as controllers and policemen between the CPU and various components of the system which is responsible for data transfer among them. Northbridge has its own heat sink since it works continuously and easily gets heated up fast. Northbridge is also called as Memory Controller Hub (MCH) and Integrated Memory Controller (IMC).The Southbridge is the chip that controls all the functions of the computer peripherals. The Southbridge can usually be distinguished from the north bridge by not being directly connected to the CPU.

The main difference between Northbridge and Southbridge is that Northbridge will take care of traffic of the faster components of the CPU and the Southbridge will controls the slower traffic components. The faster components of the CPU are video cards and random access memory. Sometimes Northbridge also handles the control of CPU cache. The slower components as I/O devices, DMA controller and system clock fall in to the control of Southbridge and it is also called as I/O controller Hub (ICH). The speed of these Buses depends on speed of FSB. When the CPU is fast and it is connected with low performance FSB then there is a result of data bottlenecks. In this case Processor performs faster than FSB for one activity and waits for FSB to send the new instruction. This state of CPU is called idle state. Therefore to utilize the faster CPU you should also have faster FSB.

Self Assessment Questions

21. FSB is also called as _____.
22. The chipset consists of two processors namely _____ and _____.
23. The state of CPU that it performs faster than FSB for the activity and waits for FSB to send the new instructions is called _____.

4.7 Dual Independent Bus (DIB)

Dual Independent Bus is architecture to connect the processor, memory, and L2 cache. L2 cache is a set of memory circuits which is designed to speed up access to frequently used data. One bus connects the processor to L2 cache and a second connects the processor to main memory. The two Bus features of DIB enables the data flow simultaneously or in parallel processing method rather than queuing up in a single sequential method and waiting for a long time to complete one instruction and CPU going to idle state. In DIB one Bus connects the CPU to level-2 cache and other Bus connects memory to level-2 cache. The main use of this connection is that level-2 cache helps in increasing performance of the Bus externally.

The following are the features of DIB:

- Increase of speed due to double Bus
- Scale up of the performance externally independent of the speed of the Bus.

- Allows access to faster cache.
- Allows multiple and parallel cache requests through the process of pipelining cache to the processor.

Self Assessment Questions

24. DIB connects _____ to _____ and _____.
25. DIB allows single sequential method for processing. (True/ false)

4.8 Troubleshooting

Generally trouble shooting of the Busis not done since it is more of a passive connector. It can be very easily replaced. But for some of the major signals which are connected to the motherboard you might need to trouble shoot. This happens at the POST board. Normally you could do this process by using LED lights in the POST boards. A light-emitting diode (LED) is a semiconductor light source. These are used as indicator lamps in many devices, and are increasingly used for lighting. LED light is used in POST board to indicate the status of the power supply, control signals and clock time. When the LED is missing in the board then it means that there is some error in connection in the motherboard.

You can note the following hints to rectify the Bus errors.

- You can use the multi-meter to check the *voltage* level in the Bus. Irrespective of low voltage or standard Bus you have to find the -12 volt dc and +5 volt dc. You should ensure that a low voltage Bus should have +3.3 Volt dc. Otherwise, you need to conclude that there is fault in the Bus and need to replace power supply.
- You can adjust the CLOCK signal between 0 Hz and 33 MHz. The timing signals for the external device and slots is provided by CLOCK signal. If the CLOCK signal is 0 then the expansion device will not work and you need the check the motherboard circuitry and rectify it.
- After correction or rectifying the expansion device, it can be set to its original settings by reinitializing with the help of *Reset* signal. You should always note that Reset signal should be active only once or twice after the power is supplied.

Some of the important considerations while connecting Bus to the various components are as follows.

- You should take care of the Bus slot versions. For example a PCI interface of 2.4 may not work with its full functionality when it is connected to a PCI interface of version 2.3 or lower versions. They are compatible with the only slots to which they are designed for.
- As the connectors are mechanical devices, they are more likely to worn out. When you are connecting the device be careful while fixing the motherboard because if the connections are wrong some of the functionality of the motherboard may fail or it may also cause severe motherboard damage. If you are more likely connecting and disconnecting the expansion devices, it may result in unreliable connections.
- It is always better to remove the faulty board or replace it. You should always remove and reinsert the board since board is a metallic device. If the board develops metallic oxides it will not work properly. By removing metallic oxide you can remove the dust from the expansion slots.
- When you find a faulty board, after removing it from the system test it on another board before replacing it to confirm the problem is related to motherboard itself. Sometimes the signal in Bus may also cause for different kind of component failure.

When the Bus slot gets failed, then very small methods you can apply.

- You can block the slot and damaged slot should not be used
- Replace the damaged Bus slot with the new Bus slot connector.
- Replace completely the motherboard.

Self Assessment Questions

26. Troubleshooting of Buses can be done at _____.
27. _____ is used to find the faulty Buses.
28. CLOCK signal can be adjusted between _____and _____.

4.9 Summary

Bus has been the little passive interrupt which has the capability to be an agent for communication between CPU, memory and various components of the computer. Bus is divided into three types of Bus, address Bus, data

Bus and control Bus. It is a backbone of the network allowing the data to pass through various computers and network. These are the electric wires which help in transferring the data. There are various types of Buses based on the type of its use such as expansion Bus, local Bus, internal and external Bus, unidirectional and bidirectional Bus. The Bus architecture is divided into 3 major types like ISA, PCI and AGP. The other kinds of Buses are FSB and DIB which are responsible for connecting the various components to motherboard. Industry Standard Architecture which are not in use were used to connect the system with video cards, sound cards, networking cards, etc. This is bigger in size than the PCI and is black in colour. ISA Buses were also referred as PC Buses. ISA has its two versions namely 8-bit ISA and 16-bit ISA.

Peripheral Component Interconnect (PCI) is a high speed, intelligent Bus. PCI supports many features like, linear burst low access latency, Bus mastering, etc.

AGP is best suited for 3D applications. AGP's performance is directly proportional to the bandwidth; its bandwidth is twice than that of PCI. The important feature of AGP specification is that a 32-bit AGP will easily fit into PCI configuration. It can process multiple request rather than waiting for a long time for the new instruction and making the CPU sit idle.Bus is queued by signals.

FSB stands for Front Sided Bus and used to connect CPU to the computer system and CPU with the various other components of the system. FSB is two directional flows of data, i.e. means various components send and receives the data from the processor.

DIB which stands for Dual integrated Bus enables the data flow simultaneously or in parallel processing method rather than queuing up in a single sequential method and waiting for a long time to complete one instruction and CPU going to idle state.

Troubleshooting with respect to Bus is done at POST boards and rectified using LED lights.

4.10 Glossary

Term	Description
I/O	The term I/O is used to describe any program, operation or device that transfers data to or from a computer and to or from a peripheral device. Every transfer is an output from one device and an input into another. Devices such as keyboard.
Back bone	A central conduit designed to transfer network traffic at high speeds.
Interrupt	An *interrupt* is an event in hardware that triggers the processor to jump from its current program counter to a specific point in the code. It is a signal that says that an event has occurred.
LPT Port	Line Print Terminal is the original, and still common, name of the parallel port interface on IBM PC-compatible computers. It was designed to operate a text printer that used IBM's 8-bit extended ASCII character set.
PC/AT	The IBM Personal Computer/AT are also called asPC AT or PC/AT, was IBM's second-generation PC, designed around the 6 MHz Intel 80286 microprocessor and released in 1984 as machine type 5170. The name AT stood for "Advanced Technology", and was chosen because the AT offered various technologies that were then new in personal computers
DMA Channel	Direct memory access (DMA) channels are system pathways used by many devices to transfer information directly to and from memory.
Expansion	IN the computer an opening is there where a circuit board can be inserted to add new capabilities to the computer called expansion slots.
COM3	A COM3 (or Communications 3) port is a communications channel on the computer that is used to transmit data from hardware devices to the processor.
IRQ	IRQ stands for Interrupt ReQuest, and refers to special numbered *channels* that are used by devices to get the processors attention.
PC/XT	The IBM PC/XT (also written PC-XT or PC XT), commonly referred to as the XT, was IBM's successor to the original IBM PC.

4.11 Terminal Questions

1. Explain the working of Bus connection.
2. Bring out the different DMA channels with its specific functions
3. After the development of two versions of architecture of Buses, why was PCI Bus selected?
4. Explain the features supported by PCIBus?
5. List the different PCI signals along with their functions?
6. What are the characteristics of AGP?
7. Explain the architecture of AGP along with its figure?
8. Compare between PCI and AGP?
9. How do you troubleshoot Bus problem?

4.12 Answers

Self Assessment Questions

1. Buses
2. a. False , b. True
3. CLOCK speed and MHz
4. Expansion
5. ISA, PCI and AGP
6. ISA
7. 8-bit and 16-bit
8. PC/XT
9. 62, 20, 8
10. 8, 5, 4
11. 4.77 MHz to 8.33 MHz
12. PCI
13. a. False , b. True , True
14. Access time
15. Interrupt ReQuest (IRQ)
16. FSB
17. Front Sided Bus
18. AGP

19. a. True m b. True , c. True , d, False
20. ATX and NLX
21. Processor Bus
22. Northbridge and Southbridge
23. Idle state
24. Level-2 cache, CPU and Memory
25. False
26. POST board
27. LED lights
28. 0 Hz to 33 MHz

Terminal Questions

1. Refer Section 4.2. BUS
2. Refer section 4.3.1, 8-bit Bus, Table 4.2. DMA channel expansion
3. Refer Section 4.4, Peripheral component Interconnect
4. Refer Section 4.4.1, PCI configuration
5. Refer Section 4.4.3, PCI signal, table 4.1, the functions of PCI signals
6. Refer Section 4.5, Accelerated Graphic Port
7. Refer Section 4.5, structure of AGP
8. Refer Section 4.5.1, AGP vs PCI
9. Refer Section 4.8, Troubleshooting

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