Unit 10 Data Converter: DAC/ADC

Structure:

10.1 Introduction

In the previous unit, we studied about the MODEM, digital multimeter and digital versatile disks. An electronic circuit that transforms a continuous analog signal into digital samples is termed an analog-to-digital converter (ADC). The other-way conversion is done by the circuit named digital-to-analog converter (DAC). An ADC takes in analog continuous signal and converts it into corresponding digital signal. DAC's convert digital sampled values to a continuous physical entity, mostly an analogue voltage. In this unit we will study about the working principles of analog-to-digital converter and digital-to-analog converter.

Objectives:

By the end of Unit 10, the learners are able to:

- explain the working principle of ADCs.
- explain the working of DACs
- define monotonicity and resolution of DAC

10.2 Working Principle & Circuits of Analog to Digital Converters

An analog-to-digital converter is a device that converts a continuous physical quantity (usually voltage) to a digital number that represents the quantity's amplitude.

The **analog-to-digital** conversion involves quantization of the input, so it introduces a small amount of error. Instead of doing a single conversion, an ADC often performs the conversions ("samples" the input) periodically. The result obtained is a sequence of digital values (i.e. digital signal) which is discrete both in time and amplitude.

Now let us study some important concepts.

Resolution

The resolution of the converter is the number of discrete values it can produce over the range of analog values. In other words, the count of samples that the circuit can generate over a range of analog values is indicated by the measure called *resolution*. The sampled values are usually shown in bits as it is stored in binary format electronically. The count of the samples available is normally a power of two. For example, an 8-bit resolution ADC can sample an input signal into $2^8 = 256$ distinct levels. The values can represent the ranges from 0 to 255.

Resolution is often specified electrically and represented in volts. In this term, resolution can be defined as voltage range divided by the count of distinct intervals as mentioned in the formula below:

$$Q = \frac{E_{FSR}}{2^M} = \frac{E_{FSR}}{N}$$

Where,

Q stands for resolution (volts per output code or step)

E_{FSR} is the reference voltage range, which is equal to $V_{RefHi} – V_{refLo}$ and M is the resolution of the circuit in bits.

Count of the distinct intervals is depended number of levels available, which is $N = 2^M$.

Examples below illustrates better:

Example 1:

Reference voltage measurement range = 0 to 5 volts

Resolution of the ADC: 10 bits (Quantization levels: $2^{10} = 1024$)

Voltage resolution of the ADC is: (5v - 0v)/1024 levels = 5/1024 = 0.00488 volts /code or 4.88mV/code.

Example 2:

Reference voltage measurement range = -5 to 5 volts

Resolution of the ADC: 12 bits (Quantization levels: $2^{12} = 4096$)

Voltage resolution of the ADC is: (5v – (-5v))/4096 levels = 10/4096 = 0.00244 volts /code or 2.44mV/code

Example 3:

Reference voltage measurement range = 0 to 8 volts

Resolution of the ADC: 3 bits (Quantization levels: 2^3= 8)

Voltage resolution of the ADC is: (8v – 0v))/8 levels = 8/8 = 1 volts /code or 1000mV/code.

In practice, the smallest output code ("0" in an unsigned system) represents a voltage range which is 0.5X (half-wide) of the ADC voltage resolution (Q) and the largest output code represents a voltage range which is 1.5X (50% wider) of the ADC voltage resolution. The other N-2 codes are all equal in width and represent the ADC voltage resolution (Q) calculated above. Doing this centers the code on an input voltage that represents the Mth division of the input voltage range. For example, with the 3-bit ADC for an 8V range, each of the N divisions represent 1V, except the 1st ("0" code) which is 0.5V wide, and the last ("7" code) which is 1.5V wide. Doing this the "1" code spans a voltage range from 0.5 to 1.5V, the "2" code spans a voltage range from 1.5 to 2.5V, etc. Thus, if the input signal is at 3/8ths of the full-scale voltage, then the ADC outputs the "3" code, and will do so as long as the voltage stays within the range of 2.5/8ths and 3.5/8ths. This is called "Mid-Tread" operation. This type of ADC can be modeled mathematically as:

$$ADC_{Code} = ROUND((\frac{2^M}{V_{RefHi} - V_{RefLo}}) * (V_{In} - V_{RefLo})).$$

The exception to this convention seems to be the Microchip PIC processor, where all M steps are equal width. This practice is called "Mid-Rise with Offset" operation. Since signal-to-noise ratio determines resolution of ADC, If there is too much noise present in the analog input, it will be impossible to accurately resolve beyond a certain number of bits of resolution, the "effective number of bits" (ENOB). In case a preamplifier is used before ADC, the noise injected by the amplifier plays a major role in overall signal-to-noise ratio. Hence the result produced by ADC will be inaccurate as the lower bits will simple be measuring noise. Advised signal-to-noise ratio is around 6dB per bit of resolution required.

Response type:

Linear Analog-to-Digital converters

Even though analog-to-digital conversion process is a non-linear process, majority of the conversion circuits are known as of the type linear. The reason why the processor is non-linear is because sampling and mapping of continuous space into discrete digital space is a piecewise operation. Linear as used here to refer the type of the ADC, stands for the linear relationship between the output values to the corresponding input value. In other words, an output value p is supposed to be from a range of input values:

n(p+b) to n(p+1+b),

where, n and b are constants. Here b is typically 0 or −0.5. When b = 0, the ADC is referred to as mid-rise, and when b = −0.5 it is referred to as mid-tread

Non-linear Analog-to-Digital Converters

Signal-to-noise ratio with respect to quantization noise takes the best value in case the probability density function (PDF) of a signal is uniform. Hence, normally, the signal is made to pass through the cumulative distribution function (CDF) of it before quantization. As a result, regions which are more relevant get better resolution quantization. An inverse CDF will be required in the dequantisation process. This concept is the same that is employed in companders used in communication systems and tape recorders and is related to maximization of entropy.

For example, a voice signal having Laplacian distribution denotes that the region around 0 carries more information than the regions with higher amplitudes. Because of the same reason, voice communication systems widely uses logarithmic ADCs to boost the dynamic range of value that can be represented by keeping the fine-fidelity in the regions with low amplitude. An 8 bit a-law or the μ-law logarithmic ADC covers the wide dynamic range and has a high resolution in the critical low-amplitude region that would otherwise require a 12-bit linear ADC.

Accuracy

ADC's are vulnerable to various kinds of errors. Quantization error and non-linearity comes with very nature of any ADC. Clock jitter causing errors called aperture error comes in light when digitizing a signal. The unit called

least significant bit (LSB) used to measure these errors. In a 10-bit ADC, one LSB error is 1/1024 of the full reference signal range, which is about 0.097%.

Quantization error

Quantization error is due to the finite resolution of the ADC, and is an unavoidable imperfection in all types of ADC. Quantization error ranges from 0 to half of one LSB. Generally, actual signal is larger than one LSB. During this, quantization error is not correlated and has a consistent distribution. Standard deviation of the distribution gives the RMS value as mentioned below:

$$\frac{1}{\sqrt{12}}\text{LSB} \approx 0.289\ \text{LSB}$$

For the 10-bit ADC discussed above, this represents 0.0282% of the signal. Quantization error becomes more dependent on the input signal in lower levels causing disturbances. This distortion is created after the anti-aliasing filter, and if these distortions are above 1/2 the sample rate they will alias back into the audio band. A noise with an amplitude 1 quantization step is included to the signal in order to make the quantization error independent of the input signal. This reduces signal-to-noise ratio slightly and eliminates the distortion completely. It is also known as *Dither*.

Non-linearity

Physical implementation imperfections cause all the ADCs to suffer from non-linearity errors resulting in deviation of the output from the linear relationship (or whatever relationship in case of non-linear type) with the corresponding input. Alleviation and prevention of these errors can be done by calibration and testing. Integral non-linearity (INL) and differential non-linearity (DNL) are important arguments for linearity.

Imagine that we are digitizing a sine wave $x(t) = A\sin 2\pi f_0 t$. Provided that the actual sampling time uncertainty due to the clock jitter is Δt, the error caused by this phenomenon can be estimated as

$$E_{ap} \leq |x'(t)\Delta t| \leq 2A\pi f_0 \Delta t$$

One can see that the error is relatively small at low frequencies, but can become significant at high frequencies. This effect can be ignored if it is

relatively small as compared with quantizing error. Jitter requirements can be calculated using the following formula:

$$\Delta t < \frac{1}{2^q \pi f_0}$$

Where q is a number of ADC bits.

Sampling rate

ADC has to convert the analog signal which is continuous in time into a flow of digital values. Hence the sampling rate of the analog signal plays a major role. Sampling rate or sampling frequency is the rate at which new digital values are sampled from the analog signal. The rate of new values is called the sampling rate or sampling frequency of the converter. If the sampling rate is higher than double the maximum frequency of the signal, a reliable faithful reproduction is possible which is based on Shannon-Nyquist sampling theorem.

Due to finite amount of delay that an ADC takes in converting a signal, the input is expected to remain constant over the time of conversion (termed conversion time). So, a sample and hold circuit performs this function – essentially, using a switch to connect the analog input signal to the capacitor where it is stored. Sample and hold sub-module is incorporated in almost all ADC integrated circuits.

Aliasing

Sampling input signals at regular intervals of time, is the way ADCs work. So, the output of an ADC can be pictured as an abstract representation of the input behavior. No information about the input signal between the two sampling instants is available. This depends on the input signal characteristic, i.e. if the input signal is a slowly changing one with respect to the sampling rate, then the value between the two sampling points could be almost the same as either of them. However, if the input change is faster compared to sampling rate, then the assumption no longer holds valid.

Output produced by the ADC is always expected to be well enough to be reconstructed back to the original input analog signals, if at all in some later stage it is made to undergo a digital to analog conversion. But, as discussed above, if the rate of change of input analog signals is much faster than the sampling rate, exact regeneration fails and unauthentic signals termed

aliases are produced at the output analog signal of a DAC. In this case, frequency of the output analog signal (aliased signal) will be difference between the input signal frequency and the sampling frequency. For example, a 5kHz sine wave sampled at 4kHz may be reconstructed as 1kHz sine wave. This is what is known as aliasing.

Aliasing is better resolved by making the input signal low pass filtered before passing it into the ADC so that the high frequency components above half of the sampling rate are filtered out. Because of this functionality, the filter is called anti-aliasing filter. This is an essential component for a real time ADC especially the ones that work on high frequency signals.

Aliasing, an undesired phenomenon in most of the systems may be used to provide down-mixing of a band limited high frequency signal.

Oversampling

As the quantization introduces white noise which is spread all over the pass band of the converter, signals are sampled at the minimum required rate. If the input signal is sampled at frequency higher than the Nyquist frequency and then filtered to limit it to the bandwidth of the signal, three main advantages results:

- Digital filters can have better properties like sharper roll off, phase etc. than analogue filters, so a sharper anti-aliasing filter can be implemented and the signal can be down sampled to give a better result
- A 20-bit ADC can be made to act as a 24bit ADC with 256x oversampling
- The signal-to-noise ratio due to quantization noise will be higher than if the whole available band had been used. So effective resolution larger than what is provided by ADC can be achieved with this technique.

Dither

You can increase the ADCs, performance by using *dither*. This is a very small amount of random noise (white noise), which is added to the input before conversion. Amplitude of the noise is set to be about half of the LSB. This mainly cause oscillating the state of LSB to switch between 0 and 1 in case of very low levels of input, rather than sticking at one constant value. It improves the effective range of signals that the ADC can convert rather than signal getting cut off at the low level with the trade-off of slight increase in noise – essentially, quantization error is included in across a series of noise

values which far more bearable than a cutoff. More accurate representation of the signal over time is possible with this. A filter at the output tuned properly can recover the small variations caused.

Without dither, a sampled audio signal of low level becomes unpleasant and disturbed. Low level always yields a '1' from the analog to digital if done without dithering. With dithering, the true level of the audio may be calculated by averaging the actual quantized sample with a series of other samples that are recorded over time. A process similar to dithering is often employed in photographic image quantization to a lesser number of bits per pixel. Even though the image becomes noisier, eye fails in recognizing those and hence sees the original realistic picture which is otherwise banded. Similar effect is what is happening in case of analogue audio that is converted to digital.

Integrating systems like electricity meters also makes use of dithering. Since the values are added together, the dithering produces more reliable results than the LSB of ADC.

Dither improves only the resolution of the sampler, it doesn't affect linearity and hence accuracy doesn't seem to improve.

ADC structures

Most common ADC implementation ways are the following:

- Flash ADCs or Direct conversion ADCs has a bank of comparators each firing for their decoded voltage range. A logic circuit follows this comparator bank which generates a code for each voltage range created. These converters are faster, but normally have only 8-bits resolution (i.e. 255 comparators as 2^n-1 is the number of comparators required) or lesser since it needs a big and expensive circuit. This type demands a large die size, high input capacitance and are prone to have glitches in the output (as outputting is out of sequence). As device mismatch is a dominant design limitation, scaling to newer submicron technologies doesn't do any better. Direct conversion ADCs are mainly employed in applications like video, wideband communications and other fast signals.
- Successive approximation ADCs makes use of comparators to eliminate the ranges of voltages, gradually settling on a final voltage range. Successive approximation continuously compares the input voltage to the

analog output voltage of the inbuilt DAC (working on the current value of approximation) until the right approximation is obtained. In every single step in the process, approximation is stored in a successive approximation register (SAR) in binary format. A reference voltage is used by the SAR for the comparison. For example, if the input voltage is 6V and the reference voltage is 10v, during the first cycle the comparison of the input voltage is done with the value 5V, (i.e. the half the value of the reference voltage: This is the voltage at the output of the inbuilt DAC when the input is a '1' followed by zeros) and the voltage output from the comparator is positive as 6V is greater than 5V. The first binary digit is set to '1' at this point. In the next clock cycle, the input voltage is compared with 7.5V (which is half value between 5V and 10V: This is the output of the inbuilt DAC when its input is '11' followed by zeros) and as 6V is lesser than 7.5V, the comparator output becomes negative. Second binary digit is therefore set to '0'. In the next clock cycle, input voltage is compared with 6.25V (half value between 5V and 7.5V: This is the output voltage of the inbuilt DAC when its input is '101' followed by zeros). Now the output of the comparator becomes negative as 6V is less than 6.25V and the third bit is set to '0'.So on, next clock cycle comparison happens with 5.625, and the fourth bit goes to '1' as 6V is greater than 5.625. Hence the result in the binary form would be 1001. This process is also termed as bit-weighting conversion. This is kind of rounding an analog signal into a binary form. As the approximations are not successive, each bit resolution will require one clock cycle. Hence clock frequency will have to be same as the value obtained by multiplying the number of bits of resolution and sampling frequency. For example, to sample audio at 44.1 kHz with 32 bit resolution, a clock frequency of over 1.4 MHz would be required. This type of ADC has better resolution and wide ranges. But it is more complex than other implementations.

- Ramp-compare ADC which is also known as dual-slope or integrating or multi-slope ADC produces a saw-tooth signal. A counter starts counting as the ramp starts. When the ramping voltage matches with the input voltage, comparator flags and the timer value is recorded. Timed ramp converters demands least number of transistors. The ramp time is sensitive to temperature because the circuit generating the ramp is often just some simple oscillator. There are two solutions for this: using a

clocked counter for DAC and then a comparator to store the counter value or improving the timed ramp. For the comparison of a second signal, just another comparator is what is required and another register to store the voltage value. This is one major advantage of the ramp-compare system. Implementation of ramp-converter can be as simple as a combination of a microcontroller, a resistor and a capacitor. A filled capacitor can be taken from an integrator, time-amplitude converter, sample and hold circuit or peak and hold circuit and discharged. As slow comparator cannot be disturbed by fast input changed, this is the major advantage of this system.

- Delta encoded ADC employs an up-down counter that feeds a DAC. Both the input signal and the DAC go to the comparator and then it is this comparator that controls the counter. This converter has a wide ranges and high resolution. Conversion time often depends on the input signal and hence it will have a guaranteed worst-case. This type of converter is a good option to deal with real-world signals. Signals in physical systems don't change abruptly. Delta and successive approximation properties are combined in some kind of converters and can very well be employed when high frequencies are known to be small in magnitude.
- Pipeline ADC make use of subranging in two or more steps. Primarily a rough conversion is performed. Then the difference from the input signal is determined using a DAC. The difference obtained is used for finer conversion and the results are combined at the end. This is a kind of refined successive approximation ADC where, interim conversion of a whole range of bits is contained in the feedback reference signal, rather than next MSB. Due to the combined merit of both the converters, this converter is faster, has got higher resolution and only requires a little die size.
- Sigma delta ADC which is also termed as Delta-Sigma ADC samples the input signal by a large factor and filters out only the required signal band. A flash ADC is placed after the filter which is used to convert smaller number of bits than that is actually required. The output signal which contains the error generated by the Flash is fed back and subtracted from the input. Due to the negative feedback, noise shaping of the error due to Flash happens and hence it doesn't appear in the

expected signal frequencies. A digital filter follows the ADC which reduces the sampling rate, filters off unwanted noise signal and increases the resolution of the output (sigma-delta modulation, also called delta-sigma modulation).

Nonelectric ADCs usually use some scheme similar to one of the above.

Commercial analog-to-digital converters

ADCs are mainly integrated circuits. 6 – 24 bits of resolution is used by many converters to sample and generate lesser than 1 mega sample per second. Thermal noise generated by the passive components limit the resolution to a maximum value of 24-bits. In room temperature and for application like audio, this noise is normally less than 1 μV of noise. If the Most Significant Bit corresponds to a standard 2 volts of output signal, this translates to a noise-limited performance that is less than 20~21 bits, and obviates the need for any dithering. Full speed analog video to digital conversion in digital video cameras, TV tuner cards and video capture cards are done with mega sample converters. Commercial converters usually have ±0.5 to ±1.5 LSB error in their output.

Pins are the most expensive part of an integrated circuit, as the package size depends on them and each pin has to be connected to the silicon chip. In order to save pins, ADC's are slowed down to send the transfer data serially one bit at a time to the computer with the next bit coming out when a clock signal state change happens from 0V to 5V. Hence quite a few pins on the ADC package are reduced and mostly it doesn't affect the complexity of the design. An analog multiplexer is used to feed the same converter from the ADCs that have several inputs. Sample and hold circuits, instrumentation amplifiers or differential inputs are included in different models of ADCs, where the quantity measured is the difference between two voltages.

Applications

Application to music recording

Music reproduction technology uses ADCs extensively. Most of the present music production happens in computer. And hence, the PCM data stream that is sent to the disc is obtained by converting the analog recorded signal using an ADC. Sample rates up to 192kilohertz can be achieved utilizing the current crop of the ADCs. Due to Nyquist-Shannon sampling theorem, many

people consider this a capability and pure marketing hype. Typically, recording techniques of high-fidelity is sampled at 44.1kHz for standard CD or 48kHz for radio/TV broadcast and analog waveform is said to have enough information in it to necessitate such high sampling rates. Cheaper or faster anti-aliasing filters of less severe filtering slopes can be used because of this kind of bandwidth headroom. Because of the gentler slopes of shallower anti-aliasing, it produces less hampering effect on sound quality. Few support on avoiding filter with ADC stating that aliasing cause lesser trouble on sound perception than pre-conversion filter. Even though, there is enough literature works on this matter, commercial considerations always overrule. Most high-profile recording studios record in 24-bit/192-176.4 kHz PCM or in DSD formats and then down sample or decimate the signal for Red-Book CD production.

10.3 Digital to Analog Converters

A digital-to-analog converter (also known as DAC, D/A, D2A or D-to-A) converts digital data (usually binary) into an analog signal (current, voltage, or electric charge). DACs are commonly used in music players to convert digital data streams into analog audio signals and in televisions and mobile phones to convert digital video data into analog video signals which connect to the screen drivers to display monochrome or color images. As per the Nyquist–Shannon sampling theorem, a DAC can reconstruct the original signal from the sampled data provided that its bandwidth meets certain requirements (e.g., a baseband signal with bandwidth less than the Nyquist frequency). Digital sampling introduces quantization error that manifests as low-level noise added to the reconstructed signal.

Practical operation

Usually the sequences of numbers update the analog voltage at steady sampling intervals instead of impulses. A clock signal is used a reference to write the numbers in to the DAC. These numbers are latched in sequence and during which the output voltage of the DAC changed rapidly from previous value to the value corresponding to the currently latched number. Resulting waveform as shown in figure 10.1 is a piecewise constant or staircase shaped as the output voltage is held in time until the next input number is latched. This affects the frequency response of the reconstructed signal and is equivalent to a zero-order hold operation.

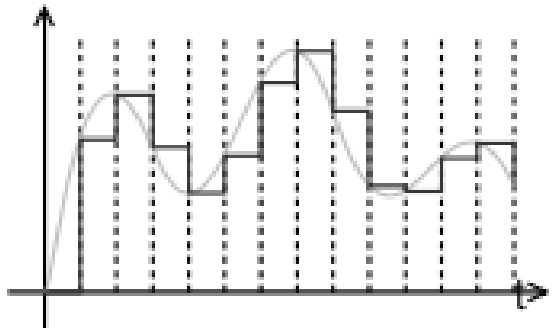

Figure 10.1 Piecewise constant output of an idealized DAC

The fact that DACs output a sequence of piecewise constant values (known as zero-order hold) or rectangular pulses causes multiple harmonics above the Nyquist frequency. So a low pass filter placed at the output removes this and hence it acts as a reconstruction filter. This filter indicates that there is an inbuilt effect of the zero-order hold over the overall frequency response of the DAC causing mild roll-off of gain at the higher frequencies and depending on the phase distortion and filter. High frequency roll-off is not the property of the sampled data but the output characteristic of DAC.

Applications

Audio

Presently audio signals are stored in digital form and it has to be converted to analog signal in order to hear it through speakers. Hence DAC's are employed in digital music player, PC sound cards and CD players.

The figure 10.2 shows the Top-loading CD player and external digital-to-analog converter.

Figure 10.2: Top-loading CD player and external digital-to-analog converter.

High-end hi-fi systems make use of specialized stand-alone DAC's as well. The digital output of a CD player is taken in and converted to a line-level

output that can then be fed to the pre-amplifier to drive speakers. Such kind of DACs can be found in USB speakers and in sound cards.

Video

Before a video signal that is stored in a digital storage such as computer is to be displayed, it has to be converted back to analog form. Until the year 2007, analog inputs were more widely used than digital, but as flat panel displays with DVI and HDMI port came up digital inputs started dominating. Device called RAMDAC combines DAC with a memory (RAM) which stores the conversion tables for contrast, brightness and gamma corrections.

Digitally controlled potentiometer which is used to digitally control an analog signal is one device that is similar to DAC

DAC types

The most common types of electronic DACs are:

- **Pulse Width Modulator** is the simplest type of DAC. A stable current or voltage is switched into a low-pass analog filter and duration is determined by the digital input code. This is a commonly used technique in speed control of electric motor and is now commonly used in high fidelity audio applications.
- **Oversampling DACs** or **Interpolating DACs** such as the **Delta-Sigma DAC**, use a technique termed pulse density conversion. Use of lower resolution DAC is allowed because of the usage of the oversampling technique. As the oversampled result is inherently linear, a simple 1-bit DAC is often selected. In a technique named delta-sigma modulation, DAC is driven with a pulse density modulated signal which is created with step non-linearity, negative feedback loop and a low pass filter. In effect, quantization noise gets high pass filtered and thus driving the noise out of the low frequencies in to the high frequency which is of little interest. This technique is called noise shaping. An analog low-pass filter at the output removes the quantization noise at the high frequencies. Due to high linearity and low cost, most of the very high resolution DACs is of this type. Increased oversampling rate can reduce the specification overhead on the low pass filter and support further reduction of the quantization noise. Delta sigma DACs make resolution of 24-bits and speed greater than 100 thousand samples per second is achievable.

- **Binary weighted DAC** is constructed with one resistor and a current source for bit of the DAC connected to a summing point. Correct output value is the sum of these precise voltages and currents. This is one of the fastest converters but this has got poor accuracy. This is because of the high precision required for each individual voltage or current. This type of converter is normally limited to 8-bit resolution or less as the high-precision resistors and current sources are expensive.
- **R-2R Ladder ADC** is a binary weighted DAC in which resistors of values R and 2R are repeatedly cascaded. Due to the easiness in producing equal valued resistors (or current sources), precision is high for this kind type of converters. But as RC-constants increases for each R-2R link, converter performance is slow.
- The **Successive-Approximation** or **Cyclic DAC** successively onstructs the output during each cycle. Note that individual bits of the digital input are processed each cycle until the entire input is accounted for.
- **Thermometer coded DAC** makes use of equal resistor or current source segment for each of the values the DAC output can possibly take. A 10-bit thermometer will have 1024 segments and a 5-bit thermometer will have 32 segments. Even though it is costly, this may be the fastest and highest precision DAC implementation.
- **Hybrid DACs** combines above techniques in a single implementation. In order to achieve low cost, high speed and high precision in one device, mostly DACs are implemented in this fashion.
    - Segmented DAC combines binary weighted principle for the LSBs and thermometer coded principle for MSBs. Hence, a compromise is reached between the resister or current source count and precision.

DAC performance

DACs are very important for the system performance. The important features of these devices are:

- **Resolution:** This is number of possible output levels the DAC is designed to reproduce. It is represented as the base two logarithm of the number of levels and is stated as the number of bits it uses. A 5-bit DAC reproduce 32 levels whereas a 10 bit DAC is developed for 1024

levels. Actual resolution attained by the DAC is measured in terms of Effective Number of Bits (ENOB).

- **Maximum sampling frequency:** This is maximum speed at which the DACs operate and still produce the correct output. Shannon-Nyquist sampling theorem says a signal must be samples at a frequency greater than or equal to twice the highest frequency value of the signal. In order to reproduce signals of frequency 30 kHz, DACs should operate at a minimum of 60 kHz. Standard CD samples audio at 44.1 kHz (audio frequency comes in the range of 20 kHz) and thus DACs of this frequency are used.
- **Monotonicity:** This is the ability of the analog output of DAC to increase with increase in digital code or vice versa. This feature is crucial for DACs used as a low frequency signal source or as a digitally programmable trim element.
- **THD+N:** This is the measure that projects the noise and distortions introduced into the signal by the DAC. It is expressed as a percentage of the noise and total power of undesired harmonics in the signal. This feature plays a major role for dynamic and small signal applications.
- **Dynamic range:** This is a measurement of the difference between the largest and smallest signals the DAC can reproduce and is expressed in Decibels. This is usually related to DAC resolution and noise floor.

DAC figures of merit

DAC contains characteristics like

- Static performance:
  - DNL (Differential Non-Linearity) shows how much two adjacent code analog values deviate from the ideal 1LSB step.
  - INL (Integral Non-Linearity) shows how much the DAC transfer characteristic deviates from an ideal one. That is, the ideal characteristic is usually a straight line; INL shows how much the actual voltage at a given code value differs from that line, in LSBs (1LSB steps).
  - Gain
  - Offset
  - Noise is ultimately limited by the thermal noise generated by passive components such as resistors. For audio applications and in room

temperatures, such noise is usually a little less than 1 μV (microVolt) of white noise. This limits performance to less than 20~21 bits even in 24-bit DACs, and cannot be corrected unless one resorts to extremely low temperatures to create superconductivity: clearly an impractical proposition.

- Frequency domain performance
  - SFDR (Spurious Free Dynamic Range) indicates in dB the ratio between the powers of the converted main signal and the greatest undesired spur
  - SNDR (Signal to Noise and Distortion Ratio) indicates in dB the ratio between the powers of the converted main signal and the sum of the noise and the generated harmonic spurs
  - HDi (i-th Harmonic Distortion) indicates the power of the i-th harmonic of the converted main signal
  - THD (Total harmonic distortion) is the sum of the powers of all HDi
  - If the maximum DNL error is less than 1 LSB, then a D/A converter is guaranteed to be monotonic. However many monotonic converters may have a maximum DNL greater than 1 LSB.
- Time domain performance
  - Glitch Energy or Glitch impulse area
  - Response Uncertainty
  - TNL (Time Non-Linearity)

Self Assessment Questions

1. The errors which occur due to physical imperfections are known as _____ errors.
2. _____causing errors called aperture error comes in light when digitizing a signal.
3. Delta encoded ADC employs an _____counter that feeds a DAC.
4. Use of lower resolution DAC is by usage of the oversampling technique called _____.
5. The _____ has poor accuracy and need high precision resistors.
6. Actual resolution attained by the DAC is measured in terms of _____.

7. Noise is ultimately limited by the thermal noise generated by active components such as diodes.(True or False ?).
8. SFDR stands for _____.

10.4 Summary

Let us recapitulate the important concepts discussed in this unit:

- An analog-to-digital converter is a device that converts a continuous physical quantity (usually voltage) to a digital number that represents the quantity's amplitude.
- The resolution of an ADC is the number of discrete values it can produce over the range of analog values.
- Even though analog-to-digital conversion process is a non-linear process, majority of the conversion circuits are known as of the type linear.
- Due to finite amount of delay that an ADC takes in converting a signal, the input is expected to remain constant over the time of conversion
- Aliasing, an undesired phenomenon in most of the systems may be used to provide down-mixing of a band limited high frequency signal.
- *Dither* is a very small amount of random noise (white noise), which is added to the input before conversion.
- Ramp-compare ADC which is also known as dual-slope or integrating or multi-slope ADC produces a saw-tooth signal.
- A digital-to-analog convert converts digital data (usually binary) into an analog signal (current, voltage, or electric charge).
- Oversampling DACs or Interpolating DACs such as the Delta-Sigma DAC, use a technique termed pulse density conversion.
- R-2R Ladder ADC is a binary weighted DAC in which resisters of values R and 2R are repeatedly cascaded.
- Resolution of a DAC is number of possible output levels the DAC is designed to reproduce.
- Monotonicity is the ability of the analog output of DAC to increase with increase in digital code or vice versa.

10.5 Terminal Questions

1. Explain the following as applied to ADC.
    a) Resolution
    b) Quantization error
    c) Dither
2. Write a short note on DAC Types.
3. Explain the following as applied to DAC.
    (i) Monotonicity
    (ii) THD+N
    (iii) Dynamic range

10.6 Answers

Self Assessment Questions

1. Nonlinearity
2. Clock jitter
3. Up-down
4. Pulse density conversion
5. Binary weighted DAC
6. ENOB
7. False
8. Spurious Free Dynamic Range

Terminal Question

1. Refer to section 10.2
2. Refer to section 10.3
3. Refer to section 10.3

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