BACHELOR OF COMPUTER APPLICATIONS

SEMESTER 3

DCA2103

COMPUTER ORGANIZATION

Unit 12

Multiprocessor Configuration

Table of Contents

1. INTRODUCTION

Till now, you have studied the process organization and peripheral devices. In this unit, we will introduce you to the concept of multiprocessors. A multiprocessor is a tightly linked computer system having more than one processing unit, each sharing principal memory, and peripherals, in order to process programs simultaneously. So, you can say that a multiprocessor is a computer system that shares the same main memory and peripherals, and is having two or more processing units the main purpose of multiprocessors is to increase the speed of execution of the system and sometimes other goals such as fault tolerance.

In this unit, you will learn about multiprocessing, different types of multiprocessors, and contention problems in multiprocessor systems.

1.1 Objectives

After studying this unit, you should be able to:

- *Define the concept of multiprocessing*
- *Describe various multiprocessor configurations*
- *Recognize the contention problems in multiprocessor systems*
- *Explain the concept of coprocessor*
- *Explain the concept of the I/O processor*

2. MULTIPROCESSING

Multiprocessing is concerned with the capability of a computer system to provide support to more than one processor or the capability to accomplish more than one program simultaneously. The term multiprocessing is also used to describe interconnected computers' configurations or computers with two or more independent CPUs that have the ability to simultaneously execute several programs. In such a system, instructions from different and independent programs are processed at the same time by different CPUs or the CPUs may execute different instructions from the same program. The multiprocessing system is depicted in figure 12.1.

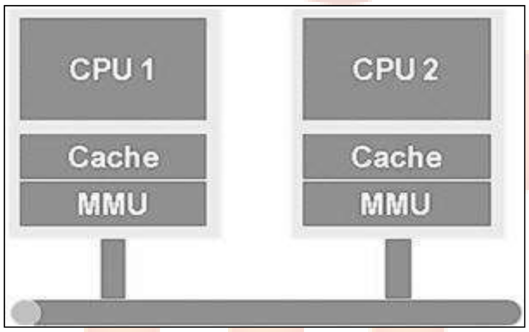

Figure 12.1: The Multiprocessor System

There are several combinations of CPUs and main memory in multiprocessing. They are as follows:

- Each CPU has its own main memory,
- All the CPUs have a common memory,
- Each CPU has access to both separate and common memories.

Also, there are several possible ways to install a multiprocessing system. They are as follows:

- In some systems, several small CPUs are linked together to perform the major processing. If even a single CPU collapses, the other CPUs will involuntarily assume its job.
- In some other systems, CPUs are connected to a complex computer network. In these systems, small CPUs called front-end processors are used for scheduling and controlling all jobs entering the system from remote terminals and other input devices. The main CPU or CPUs called host computers or backend processors are used only for major processing jobs and not for data communication.
- In some multiprocessing systems, each CPU performs only specific types of applications. For e.g., in the case of a multiprocessing system with two CPUs, one may be used to process only online jobs while another is used for batch processing.

However, these systems are so designed that in case there is a breakdown of even a single CPU, the other assumes the entire workload until repairs are made.

2.1 Advantages And Disadvantages Of Multiprocessing

These are several benefits of multiprocessing. A few of them are as follows:

- It makes the functioning of computer systems better by permitting parallel processing of program segments. Improved performance is decided by better throughput and lower task completion period of such systems.
- Besides the CPUs, it also makes possible increased efficiency in the utilization of every other device of the computer system.
- It offers a fitted backup. Even if a single CPU collapses, the other CPUs will automatically bear the workload of the other till the time the faulty CPU is repaired. Consequently, an absolute breakdown of such a system is extremely unusual.

Multiprocessing has the following limitations:

- It needs a sophisticated operation of the system to plan, maintain equilibrium and harmonize the input, output, and processing activities of numerous CPUs.
- The design of this operating system is quite a prolonged job and it needs extremely accomplished computer professionals.
- A huge main memory is needed for holding together the complicated operating system as well as several programs of users.
- Such systems are extremely costly, additional high charges have to be paid initially. The routine operation and maintenance of such systems are also quite expensive.

2.2 Multiprogramming Vs. Multiprocessing

Multiprogramming is the interleaved (interleaving is a method to organize data in an unconnected way to boost performance.) implementation of two or more processes by a sole CPU computer system. In other words, it includes executing a part of one program, after that a segment of another, etc. in small successive time periods.

On the contrary, multiprocessing is the execution at the same time of more than two processes by a computer system having greater than one CPU. A multiprocessor causes the system to work at the same time on a number of program segments of one or more programs.

Why choose a multiprocessor?

Multiprocessor has many advantages over a single CPU. Some of them are:

- A single CPU can only go fast up to a limit
- Share hardware between CPUs
- Multiple users
- Multi-tasking inside an application
- Multiple applications
- Throughput and/or responsiveness

Many times, there is confusion between the terms 'Multiprocessor' and 'Multiprocessing'. Multiprocessing is a kind of processing where two or more processors work in a combined way to process one program simultaneously, while the term Multiprocessor refers to the hardware architecture that enables multiprocessing.

Cache Coherency: cache coherence or cache coherency refers to the consistency of data stored in local caches of a shared resource. Coherence defines the behavior of reads and writes to the same memory location. In a shared-memory multiprocessor system with a separate cache memory for each processor, it is possible to have many copies of any one instruction operand: one copy in the main memory and one in each cache memory.

When one copy of an operand is changed, the other copies of the operand must be changed also. Cache coherence is the discipline that ensures that changes in the values of shared operands are propagated throughout the system in a timely fashion. Multiprocessor systems with caches use a coherency protocol, which ensures that writes by one processor eventually become visible to all other processors and that no two processors write to the same memory location simultaneously.

Memory Consistency

A memory consistency model determines in which order processes get notice of memory accesses by other processes. They define correct shared memory behavior in terms of loads and stores (memory reads and writes) without reference to caches or coherence. A multiprocessor system is sequentially consistent if the result of any execution is the same as if the operations of all the processors were executed in some sequential order, and the operations of each individual processor appear in this sequence in the order specified by its program

Self-Assessment Questions - 1

1. ______________________is the interleaved execution of more than two processes by a sole CPU computer system.
2. Multiprogramming makes the performance of computer systems better by permitting parallel processing of program segments. (True/False)

Activity 1

With the help of internet, prepare a timeline of Multiprocessing starting with its earliest history and its applications in various fields from past to present. Also include a short paragraph telling your thoughts on its future application.

3. COUPLED MULTIPROCESSORS

Multiprocessors can be configured in two ways. They can be either closely/tightly-coupled or loosely-coupled. These are explained in the following sub-sections.

3.1 Closely/Tightly-Coupled Multiprocessors

Closely or tightly-coupled multiprocessor systems contain multiple CPUs. In closely/tightly-coupled multiprocessors, all processors are tied up together in some manner to have secure communication with one other. These multiprocessors use common data structures, a common system clock, and the main memory in a combined way. It is controlled by the operating system.

A tightly-coupled multiprocessor system consists of multiple CPUs and these CPUs are linked jointly at the bus level. These CPUs may have access to a Uniform Memory Access (UMA) or central shared memory/ Symmetric Multiprocessing (SMP) or, may take part in a memory hierarchy with both shared and local memory (NUMA-NonUniform Memory Access). An example of tightly-coupled multiprocessor architecture is shown in figure 12.2.

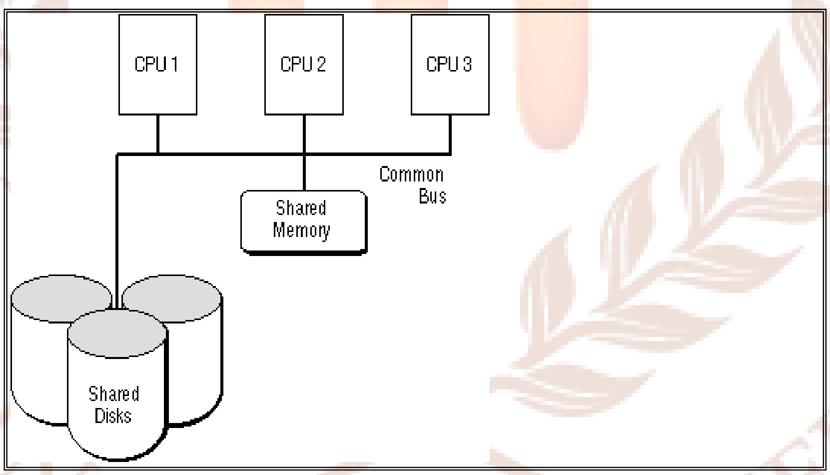

Figure 12.2: Tightly-Coupled Multiprocessor

SMP refers to **Symmetric Multiprocessing**. SMP denotes that all processors are equal and there is no master-slave relationship between them. The IBM p690 Regatta (IBM p690 Regatta is one of IBM's 64-bit, symmetric multiprocessing SMP servers) depicts an instance of a high-end symmetric multiprocessing system. In shared memory **UMA**, all memory addresses are reachable as fast as any other address.

Chip multiprocessors: The greatest form of tightly-coupled multi-processing comprises several processors located on a single chip.

Mainframe systems along with multiple processors tend to be frequently tightly-coupled. Tightly-coupled multiprocessors are usually smaller in size as compared to loosely-coupled multiprocessors. These are also better in terms of performance. This is due to the fact that there is a short delay faced at the time the message is sent from one computer to the other while there is a high data rate.

Tightly-coupled multiprocessors are expensive as compared to loosely coupled multiprocessors.

3.2 Loosely-Coupled Multiprocessors

In very simple words, a loosely-coupled multiprocessor is a multiprocessor configuration in which each processor has its own I/O channels and memory. 'Clusters' is the name often given to a loosely-coupled multiprocessor system. One common example of a loosely-coupled system is the Linux Beowulf cluster. Loosely-coupled multiprocessor architecture is shown in figure 12.3.

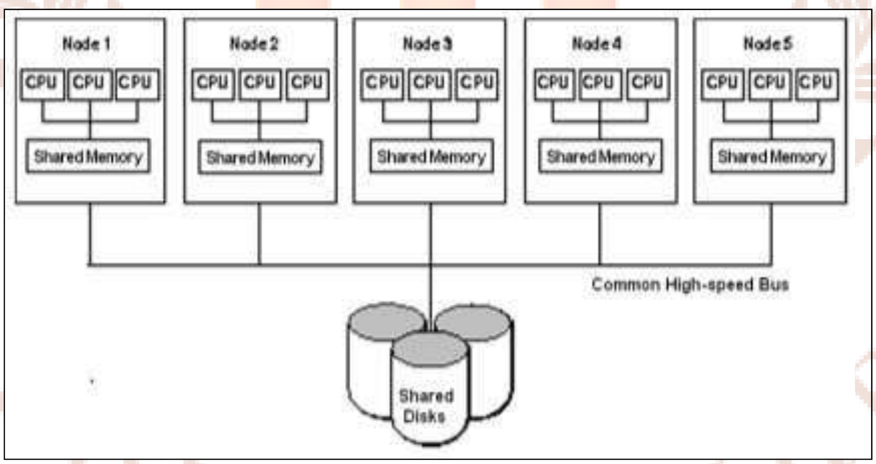

Figure 12.3: Loosely-Coupled Multiprocessor

Multiple standalone dual or single processor commodity computers unified through a high-speed communication system form the basis of loosely- coupled multiprocessors. Gigabit Ethernet is one of the most common high-speed communication systems.

A brief comparison between tightly-coupled and loosely-coupled multi-processors is given in table 12.1.

Table 12.1: Tightly- vs. Loosely-Coupled Multiprocessor

	Criterion	Tightly-Coupled	Loosely-Coupled
1.	**Capacity**	Low system capacity	High system capacity
2.	**Availability**	Less easily available	Easy availability
3.	**Cost and Maintenance**	Usually inexpensive andcan be recycled	Huge initial investments may depreciate quickly
4.	**Power Consumption**	More energy efficient	Use components that are unnecessary for such a system

Self-Assessment Questions - 2

3. SMP refers to____________________________.   .
4. Chip multiprocessors is the most extreme form of loosely-coupled multiprocessing. (True/False)
5. A Loosely-coupled multiprocessor system is often referred to as_____________________
6. _______________________ is one of the common examples of a loosely- coupled system.

4. CONTENTION PROBLEMS IN MULTIPROCESSOR SYSTEMS

The contention ratio in computer networking refers to the ratio of the probable maximum demand to the real bandwidth. If the contention ratio is higher, the number of users that may be attempting to utilize the actual bandwidth at any single time will also be greater and, as a result, the effective bandwidth offered will be lower.

A shared memory multiprocessor system develops the problem of contention due to memory sharing. Contention occurs because different processors strive for the same memory space. Contention results in loss of performance of the system.

There are mainly three types of contention in a multiprocessor system, which we are going to study now.

4.1 Memory Contentions

In a shared-memory multiprocessor system, when several processors request the same memory module at the same time, it results in memory contention the problem of memory contention is resolved by using an arbiter. Arbiter permits the requester to precede one request at a time. But this procedure results in a loss of performance of the system as the processor has to wait to complete its memory cycle in case of waiting.

4.2 Communication Contention

Communication contention occurs when various processors are unable to complete their access because of the interconnection network limitations. Communication contention may also occur in a situation when the processors request access to different memory modules. In order to avoid the problem of severe contention, it must be kept in mind that the bandwidth of the interconnection network should be proportional to the count of processors, as the traffic of processor memory is directly proportional to the count of processors as well. Therefore, communication contention is easily prone to occur in a system containing a large number of processors, if various processors request a common link/resource in the interconnection network.

4.3 Hot Spot Contention

Hot spot is another common type of contention problem in a multiprocessor system. It is a situation where several processors repeatedly access the same memory location, resulting in the creation of a hot spot in the memory location or the interconnection network.

It is symbolic of the situation that the network is overloaded with the processor requests. It finally results in the creation of a bottleneck for system performance.

4.4 Techniques For Reducing Contention

After studying various types of contention problems in a multiprocessor system, we will now briefly study about the techniques to reduce contention.

There are mainly four ways to reduce contention as discussed below.

a) **Memory allocation:** Memory contention can be also reduced by taking care of the proper memory allocation. For this, the local memories should store the code and data structures private to the processors to which they link (See the figure 12.4 (a)).

b) **Cache Memory:** Attaching a separate cache memory to each processor in a multiprocessor system may help to reduce the memory traffic. Therefore, it proves beneficial in reducing the problem of memory and communication contention (See the figure 12.4 (b)).

c) **Local and Global Memories:** To resolve the problem of memory contention, the memory module can be partitioned into two categories: Local memory and Global Memory. Local memory (or the private memory) is the memory that is linked to the processor and therefore, can be directly accessed by the processor, whereas, global memory (or shared memory) is the memory that can be accessed through the interconnection network only. This will help to greatly reduce the network traffic (See the figure12.4 (c)).

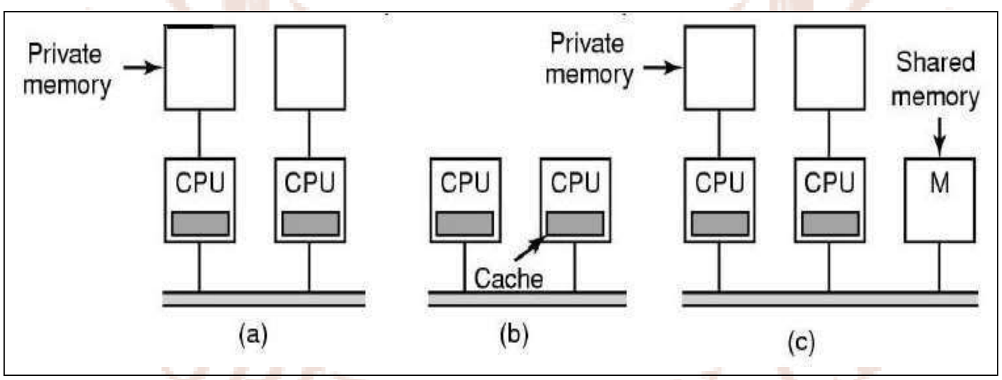

Figure 12.4: Ways to Reduce Contention

d) **Better Interconnection network**: Communication contention can be reduced by using a high bandwidth network such as multi-port memories, crossbar switches, or a multistage network. Techniques such as pipelining several memories may also prove beneficial in a bus-based system. The combining technique is utilized to resolve the performance degradation problem caused due to hot spot contention. In a shared data structure, the data allocation must be uniformly distributed across the shared memory requests which result in reducing memory contention problem. Proper allocation of the data structure must be done by the compiler.

Self-Assessment Questions - 3

7. There are mainly ________________ types of contention in a multiprocessor system.
8. Contention occurs because same processors strive for the same memory space. (True/False)

5. COPROCESSOR

Coprocessor is a relatively new concept in the area of multiprocessing. A coprocessor refers to a computer processor which is utilized as an addition to the functions of the CPU (the primary processor). A coprocessor is also known as a **math processor** or a **numeric processor.** It is capable of carrying out a large number of computations, thereby helping the main processor. Various types of operations that may be performed by the coprocessor are floating-point arithmetic, graphics, signal processing, string processing, or encryption. Coprocessors are capable of enhancing the system performance by relieving the main processor of processor-intensive tasks. Coprocessors allow a line of computers to be customized so that customers who do not need the extra performance need not pay for it.

Coprocessors mainly perform three functions:

i. **Computation:** Coprocessor is capable of performing various types of numeric computations. It thus helps to reduce the load from the microprocessor and speed up the performance of the system.

ii. **Speed Enhancement:** One of the major functions of the coprocessor is to speed up the rate at which the various programs and applications run in the system.

iii. **Offloading:** Coprocessors process helps to reduce the workload of the multiprocessor. The motherboard assigns some of the work to the coprocessor, which otherwise would have been assigned to the multiprocessor. Therefore, with the help of the coprocessor, the multiprocessor is offloaded of its work.

Figure 12.5 shows the above three functions of coprocessors.

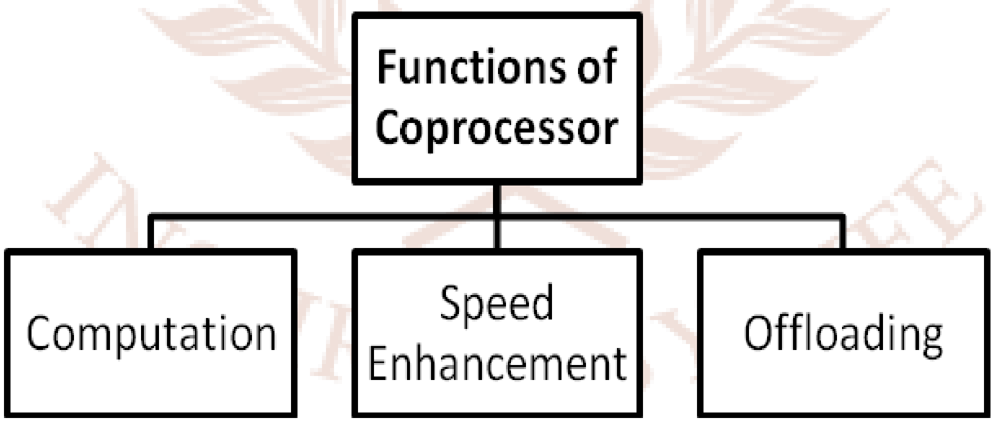

Figure 12.5: Functions of Coprocessor

Self-Assessment Questions - 4

9. The main functions of a multiprocessor include Computation, Speed Enhancement and________________________- .
10. A coprocessor is also known as a math processor or a numeric processor. (True/False)

Activity 2

Prepare a short report on use of coprocessors in the field of computergames and ecommerce. You can take the help of internet.

6. I/O PROCESSOR

A system may assimilate one or more external processors and assign them the duty of direct communication with all I/O devices. An Input-Output Processor (IOP) may be termed as a processor with the ability of direct memory access which communicates with I/O devices. In this configuration, the computer system may be segregated into a memory unit and a number of processors comprised of one or more IOPs and the CPU. Each IOP takes charge of output and input tasks thereby, reducing system tasks of the CPU which are involved in I/O transfers.

The IOP is similar to a CPU with the exception that it is planned to handle the tiny details of I/O processing. In relation to a DMA controller which requires to be set up completely by the CPU, the IOP is able to fetch and execute its personal instructions. These IOP instructions are specifically designed to ease I/O transfers. Additionally, the IOP has the ability to perform other processing tasks, like logic and arithmetic operations, code translation, and branching.

Figure 12.6 depicts the block diagram of a computer along with an I/O Processor. It is obvious that the memory unit holds a central position and has the ability to communicate without difficulty with each processor with the help of direct memory access. The CPU is in possession of processing data required in the solution of computational jobs. The IOP depicted here offers a pathway for the transfer of data between the memory unit and several peripheral devices.

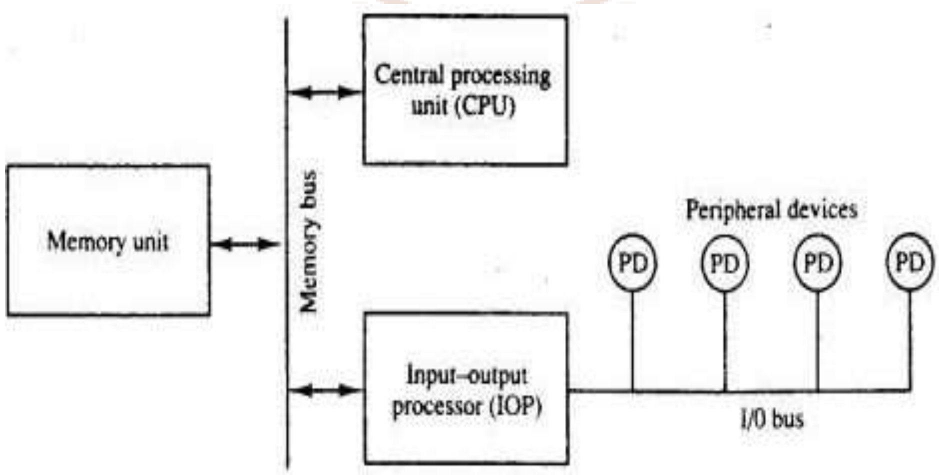

Figure 12.6: Block Diagram of a Computer with I/O Processor

The data formats of CPU data and memory are dissimilar to the data formats of peripheral devices. So, IOP should construct data words from many varied sources. For example, it may be mandatory to acquire eight bytes from an input device and group them into a single 32-bit word prior to its transfer to memory. Data are collected and transferred in the IOP at the bit capacity and device rate at the same time as the CPU is executing its personal program.

The communication between the devices attached to the IOP and the IOP itself is just like the program control ways of transfer. The methods by which the IOP and CPU communicate rely on the sophistication level included in the system. In the majority of computer systems, the CPU denotes the master whereas the IOP denotes a slave processor. The CPU is accountable for assigning the job of starting all operations; however, I/O instructions are implemented in the IOP. The instructions of the CPU are needed to initiate an I/O transfer as well as to test the I/O status settings needed for deciding several I/O activities. The IOP, in turn, generally calls for the attention of the CPU by way of an interrupt. It also reacts to CPU requests by inserting a status word in an already fixed location in memory to be inspected afterward by a CPU program. As soon as an I/O operation is needed, the CPU instructs the IOP where to locate the I/O program and then passes on the transfer details to the IOP.

6.1 CPU-IOP Communication

There are various methods of communication between CPU and IOP. In most cases, the memory unit denotes a message center wherein every processor passes on information to the other. To describe the working of a typical IOP, we will demonstrate by a particular example, the process by which the IOP and the CPU communicate. Figure 12.7 shows a flowchart of the sequence of operations. Firstly, an instruction is sent by the CPU to test the IOP path. Then, the IOP responds by placing a status word in memory for the CPU to verify. The bits of the status word depicts the condition of the I/O device and IOP, like “IOP overload condition”, “device busy with another transfer”, or “device ready for I/O transfer”. The CPU then decides what to do next by referring to the status word in memory. If all conditions are set, the CPU dispatches the instruction to initiate I/O transfer. The memory address which gets this instruction informs the IOP about the location of its program.

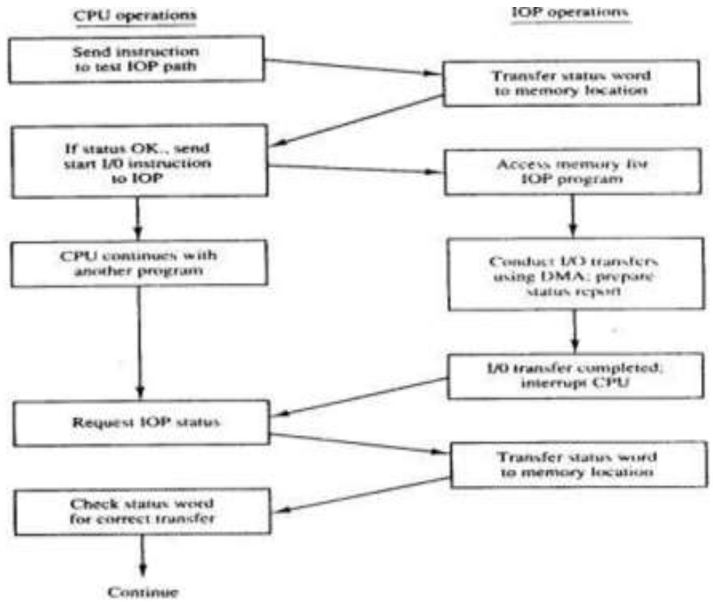

Figure 12.7: CPU-IOP Communication

The CPU is now free to carry on with another program even as the IOP is occupied with the I/O program. Both programs denote memory by means of DMA transfer. As soon as the IOP finishes the execution of its program, it dispatches an interrupt request to the CPU. Then the CPU reacts to the interrupt request by releasing an instruction in order to interpret the status from the IOP. After this, the IOP reacts by inserting the contents of its status report in a particular memory location. The IOP looks after all data transfers between the memory and several I/O units at the same time as the CPU is occupied with processing another program. The CPU and IOP are both competing with each other for the utilization of memory, that's why the number of devices that can be in working mode is limited by the time of access of the memory.

6.2 Channel

Channel I/O is a general term that denotes a high-performance input/output (I/O) architecture that is executed in several forms on numerous computer architectures, particularly on mainframe computers. A particular computer system configuration comprises numerous channels with every channel linked to one or several I/O devices. There exist basically three kinds of channels. Table 12.2 lists these three types of channels.

Table 12.2: Types of Channels

	Channel	Explanation
a)	**Multiplexer**	The multiplexer channel can be linked to numerous medium and slow-speed devices and has the ability to operate with numerous I/O devices at the same time.
b)	**Selector**	The selector channel is planned to control a single I/O operation at one time and is usually utilized to control a single high-speed device.
c)	**Block-multiplexer**	The CPU has direct communication with the channels by way of dedicated control lines and indirect communication bymeans of reserved storage areas in memory.

The I/O instruction format consists of three fields: channel address, operation code, and device address. Figure 12.8 shows the fields of the I/O instruction format.

Figure 12.8: I/O Instruction Format

The computer system might have numerous channels, and every channel is allocated an address. Likewise, every channel may be linked with several devices and every device is allocated an address.

Thus, these three fields are explained below:

i) The operation code specifies the I/O instructions. There exist eight I/O instructions namely, start I/O fast release, start I/O, halt I/O, test I/O, halt device, clear I/O, store channel identification, and test channel.

ii) The addressed channel reacts to each of the I/O instructions and implements it. It also decides one of four condition codes in a processor register called Processor Status Word (PSW). The CPU has the ability to check the condition code in the PSW to find out the outcome of the I/O operation.
The condition codes normally specify the conditions given below:
- Whether the device or the channel is occupied,
- Whether or not it is functional,
- Whether interruptions are awaiting if the I/O operation had initiated successfully, and
- Whether a status word was saved in memory by the channel.

iii) The device address indicates the specific I/O device to be utilized. As soon as the I/O operation is finished, the IOP saves its status bits in the status word position and interrupts the CPU. The CPU has the ability to refer to the status word to make sure whether the transfer has been concluded successfully or not.

An example of a channel program is shown in below-given table 12.3.

Table 12.3: BM-370 Channel Program Example

Command	Address	Flags	Count
Write tape	4000	100000	60
Write tape	6000	010000	20
Write tape	3000	000000	40

It comprises three command words. The initial word causes a byte to move into a magnetic tape from memory beginning at address 4000. The next two command words carry out a similar function with a separate part of memory as well as a byte count. The six flags in every control word indicate particular interrelations between counts. The first flag is fixed at 1 in the first command word to indicate "data chaining." It leads to a combination of the 60 bytes from the initial command word with the 20 bytes of its successor into a single record of 80 bytes. These 80 bytes are written on tape with no gaps or separation although two memory sections were used.

The second flag is fixed at 1 in the second command word to indicate "command chaining." It instructs the channel that the subsequent command word will utilize the same 'I/O' device, the tape, as seen in this case. The channel instructs the tape unit to begin placing a record gap on the tape and continues to read the next command word from memory. The 40 bytes present at the third command word are subsequently written on tape like a separate record.

As soon as all the flags are equivalent to zero, it denotes the conclusion of I/O operations for the specific I/O device

Self-Assessment Questions - 5

11. In the IBM 370, the I/O processor computer is known as a.____________________ .
12. There are many forms of the communication between CPU and IOP. (True/False).

7. CASELET: MULTIPROCESSOR OPERATING SYSTEM TYPES

The multiprocessor operating systems are complex in comparison to multi programs on a uni-processor operating system because the multiprocessor executes tasks concurrently. Therefore, it must be able to support the concurrent execution of multiple tasks to increase processor performance.

Depending upon the control structure and its organization the three basic types of multiprocessor operating systems are:

1) Separate supervisor
2) Master-slave
3) Symmetric Supervision

Separate Supervisors: In a separate supervisor system each process behaves independently. Each system has its own operating system which manages local input/output devices, files system, and memory as well as keeps its own copy of kernel, supervisor, and data structures, whereas some common data structures also exist for communication between processors. The access protection is maintained, between the processor, by using some synchronization mechanism like semaphores. Such architecture will face the following problems:

1. Little coupling among processors.
2. Parallel execution of single task.
3. During process failure it degrades.
4. Inefficient configuration as the problem of replication arises between supervisor/kernel/data structure code and each processor.

Master-Slave: In master-slave, out of many processors one processor behaves as a master whereas others behave as slaves. The master processor is dedicated to executing the operating system. It works as a scheduler and controller over slave processors. It schedules the work and also controls the activity of the slaves. Therefore, usually, data structures are stored in its private memory. Slave processors are often identified and work only as a schedulable pool of resources, in other words, the slave processors execute application programs.

This arrangement allows the parallel execution of a single task by allocating several subtasks to multiple processors concurrently. Since the operating system is executed only by master processors, this system is relatively simple to develop and efficient to use. Limited scalability is the main limitation of this system because the master processor becomes a bottleneck and will consequently fail to fully utilize slave processors.

Symmetric: In symmetric organization all processors configuration are identical. All processors are autonomous and are treated equally. To make all the processors functionally identical, all the resources are pooled and available to them. This operating system is also symmetric as any processor may execute it. In other words, there is one copy of the kernel that can be executed by all processors concurrently. To that end, the whole process is needed to be controlled for proper interlocks for accessing scarce data structures and pooled resources.

The simplest way to achieve this is to treat the entire operating system as a critical section and allow only one processor to execute the operating system at one time. This method is called the 'floating master' method because in spite of the presence of many processors only one operating system exists. The processor that executes the operating system has a special role and acts as a master.

As the operating system is not bound to any specific processor, therefore, it floats from one processor to another. Parallel execution of different applications is achieved by maintaining a queue of ready processors in shared memory. Processor allocation is then reduced to assigning the first ready process to the first available processor until either all processors are busy or the queue is emptied. Therefore, each idled processor fetches the next work item from the queue.

Question

Explain in your own words the various types of multiprocessor operating systems.
(**Hint**: There are basically three basic types of multiprocessor operating systems: Separate supervisor, Master-slave, and Symmetric Supervision)

8. SUMMARY

In this unit, we discussed about the concept called multiprocessing, different types of multiprocessors, and contention problems in the multiprocessor systems. We also discussed coprocessor and i/o processors. Now let us recapitulate the important concepts discussed in this unit:

- Multiprocessing is used to describe interconnected computer configurations or computers with two or more independent CPUs that have the ability to simultaneously execute several programs.
- There are mainly two types of multiprocessor configuration: tightly-coupled multiprocessors and loosely-coupled multiprocessors.
- A shared memory multiprocessor system develops the problem of contention due to memory sharing. Contention results in loss of performance of the system.
- There are essentially three types of contention in a multiprocessor system: they are memory contention, communication contention, and hot spot contention.
- A coprocessor is a computer processor that is used as a supplement to the functions of the primary processor (the CPU). A coprocessor is also known as a math processor or a numeric processor.
- Coprocessors mainly perform three functions: computation, offloading work of multiprocessor, and enhancing speed.
- An input-output processor has direct memory access capability that communicates with i/o devices.
- The communication between the devices attached to the IOP and the IOP itself is just like the program control ways of transfer.
- The i/o processor computer is also known as a channel in the IBM 370 the three types of channels include multiplexer, selector, and block- multiplexer.

9. GLOSSARY

- **Channel I/O**: Channel I/O is a general term that denotes a high-performance input/output (I/O) architecture that is executed in several forms on numerous computer architectures, particularly on mainframe computers.
- **Chip multiprocessors:** An extreme form of tightly-coupled multi-processing that consists of more than one processor placed on a single chip.
- **Communication contention:** A contention that occurs when various processors are unable to complete their access due because of the interconnection network limitations.
- **Coprocessor:** A computer processor that is used as a supplement to the functions of the primary processor (the CPU).
- **Input-Output Processor (IOP):** An external processor that communicates directly with all I/O devices and has direct memory access capabilities.
- **Multiprocessing:** A system of interconnected computer configurations or computers with two or more independent CPUs that have the ability to simultaneously execute several programs.
- **Multiprogramming:** Multiprogramming is the interleaved implementation of two or more processes by a sole CPU computer system.
- **NUMA:** Non-Uniform Memory Access
- SMP: Symmetric multiprocessing
- **UMA:** Uniform Memory Access

10. TERMINAL QUESTIONS

1. Explain the meaning of multiprocessor? What are the various types of multiprocessor configuration?
2. List the advantages and disadvantages of multiprocessing.
3. Differentiate between multiprocessing and multiprogramming.
4. Explain the concept of coprocessor. Also explain its functions.
5. Describe briefly I/O processor.
6. Discuss loosely coupled multiprocessor?
7. Describe tightly coupled multiprocessor configuration?
8. Write a short note on contention problem in multiprocessor system.

11. ANSWERS

Self-Assessment Questions

1. Multiprocessing
2. True
3. Symmetric Multiprocessing
4. False
5. Clusters
6. Linux Beowulf cluster
7. Three
8. False
9. Offloading
10. True
11. Channel
12. True

Terminal Questions

1. Multiprocessor is a system of interconnected computers' configurations or computers with two or more independent CPUs that have the ability to simultaneously execute several programs. Refer Section 2.
2. Multiprocessing improves the performance of computer systems.One disadvantage is that it is expensive. Refer to section 2.
3. Multiprocessing involves many CPU/processors whereas in multi- programming only a single CPU carries out multiple programs simultaneously. Refer Section 2.
4. A coprocessor is a computer processor that is used as a supplement to the functions of the primary processor. Refer Section 5.
5. I/O processor controls the transfer of information between the computer's main memory and the external equipments. The control unit uses the I/O processor to execute I/O instructions. Refer Section 6.
6. Every processor has its own I/O channels and memory in a loosely- coupled multiprocessor. Refer Section 3.

7. A tightly-coupled multiprocessor is a configuration in which processors shares main memory. Refer Section 3.
8. When more than one processor seeks bus access at the same time, it gives rise to contention due to memory sharing resulting into performance degradation. There are mainly three types of contention in a multiprocessing system. Refer Section 4.

References:

- Sajjan G. Shiva; Computer Design and Architecture; Marcel Dekker
- Silvia Melitta Mueller, Wolfgang J. Paul; Computer Architecture; Springer
- Joseph D. Dumas II; Computer Architecture; CRC Press
- Nicholas P. Carter; Schaum's outline of computer Architecture; Mc. Graw-Hill Professional

E-references:

- http://publib.boulder.ibm.com/infocenter/zos/basics/topic/com.ibm.zos.z concepts/zconcepts_75.html/
- http://www.ibm.com/search/csass/search?sn=mh&q=multiprocessing
- %20system&lang=en&cc=us&/
- http://siber.cankaya.edu.tr/ozdogan/OperatingSystems/ceng328/node44. html/
- http://docs.oracle.com
- www.scribd.com/doc/53304318/95/INPUT-OUTPUT-PROCESSOR-IOP
- http://vedyadhara.ignou.ac.in/wiki/images/5/5b/MediaB3U1mcs-041.pdf
- http://zone.ni.com/devzone/cda/tut/p/id/6097#toc0