BACHELOR OF COMPUTER APPLICATIONS

SEMESTER 3

DCA2103

COMPUTER ORGANIZATION

Unit 10

I/O Organization – Part 2

Table of Contents

1. INTRODUCTION

In the previous unit, you studied the need for I/O Module, External Devices, Input / Output Module, Programmed I/O, and Interrupt Driven I/O.You will find that in describing computer systems, a distinction is often made between computer architecture and computer organization. Computer architecture is related to the behavior and structure of the computer as observed by the user. It comprises the instruction set, techniques for addressing memory, and the information formats.

Computer organization is related to the manner in which the hardware components operate as well as the manner in which they are linked together to form the computer system. You must be aware that a computer is useful for the primary reason that it can take input, and process it to give output. The input-output subsystem (I/O) is hence an integral part of our study. This unit will give insight into the input & output devices, known as peripherals, how they communicate with the processor, and their model of transfer. The range of I/O devices and the large variation in their nature, speed, design, function, usage, etc. make it difficult for the operating system to handle them with any generality. The key concept in I/O software designing is device independence achieved by using uniform naming.

In this unit, you will also study the basic concept of DMA in the I/O organization and all the important concepts relating to I/O such as synchronous and asynchronous data transmission, PCI bus, etc.

1.1 Objectives:

After studying this unit, you should be able to:

- *Discuss the data transfer techniques*
- *Explain the concept of DMA*
- *Discuss about Intel 8237*
- *Discuss about Bus arbitration*
- *Explain I/O Interface*
- *Examine the synchronous and asynchronous data transfer techniques*
- *List and explain the main features of parallel I/O 8255*

- *Explain serial I/O 8251*
- *Describe the concept of PCI*
- *Explain the function of SCSI Bus*
- *Discuss about serial I/O*

2. DATA TRANSFER TECHNIQUES

In an I/O organization, there are various modes of information transfer. So let us first understand these various techniques available for data transfer.

Data transfer between the I/O devices and the central computer may be tackled in several modes. Few modes utilize the CPU as an intermediate path; while others transfer the data straight to and from the memory unit, with no intervention of CPU just as in DMA. Data transfer to and from peripherals can be performed in either of three likely modes:

1. Programmed I/O
2. Interrupt Driven I/O
3. Direct Memory Access (DMA)

Programmed I/O: The 'I/O' operations are entirely controlled by the CPU. The CPU implements programs that begin, direct and end an I/O operation. It needs a bit of special I/O hardware; however, it is quite lengthy for the CPU. This is because the CPU has to pause for slower I/O operations to finish before the CPU is able to obtain the next operation.

Interrupt-driven I/O: One more technique that suggests decreasing the waiting of CPU is interrupt-driven I/O. *Interrupt-driven* I/O, utilized by many systems for at least a few devices, permits the CPU to work on a few other processes even as waiting for the I/O device., Interrupt-driven I/O is the solution to good response times and multitasking operating systems in general-purpose applications.

The CPU gives out the I/O command to the I/O module and begins doing other work, which might be an implementation of a separate program. As soon as the I/O operation is finished I/O module intrudes the CPU to notify that the I/O operation has been completed. CPU, then, might head execution of such program.

In both programmed I/O as well as to interrupt-driven I/O, the CPU is in charge of reading data from the memory (output) as well as writing data into the memory (input). This need does not occur in DMA where the memory can be retrieved directly by the I/O module. Hence, the I/O module can store or retrieve data from/in the memory.

Self-assessment questions -1

1. _____ is used by most systems.
2. The memory can be retrieved directly by the I/O module in DMA. (True/False)

3. DIRECT MEMORY ACCESS (DMA)

In the earlier section you have already studied the two data transfer techniques i.e. programmed I/O and interrupt-driven I/O. Now we will

discuss the third technique of data transfer i.e. Direct Memory Access (DMA).

When a large quantity of data is to be transferred from the CPU, a DMA module can be utilized. In both Programmed and Interrupt driven I/O, the CPU is busy implementing input/output instructions. However, DMA permits information to be transferred fast in and out of memory with no intervention of the CPU.

In the majority of mini- and main-frame computer systems, a great deal of input(writing to the memory) and output (reading from the memory)happens between the processor and the disk system. As these systems carry huge data, so it is quite useless to perform such operations directly via the processor as it would be very time-consuming and also utilize the precious CPU time. An effective approach for such a problem is to put the data directly inside the memory or acquire the data directly from the processor with no direct intervention from the processor and that too at a very high speed. I/O performed in such a manner is generally called direct memory access or DMA. If the data to be transferred is in bulk then the DMA technique is the best choice as it increases the data transfer speed.

Figure 10.1 shows Registers of a general DMA module. You should remember that it comprises additional registers for counting the data bytes as well as data lines for feeding the address register and data count registers.

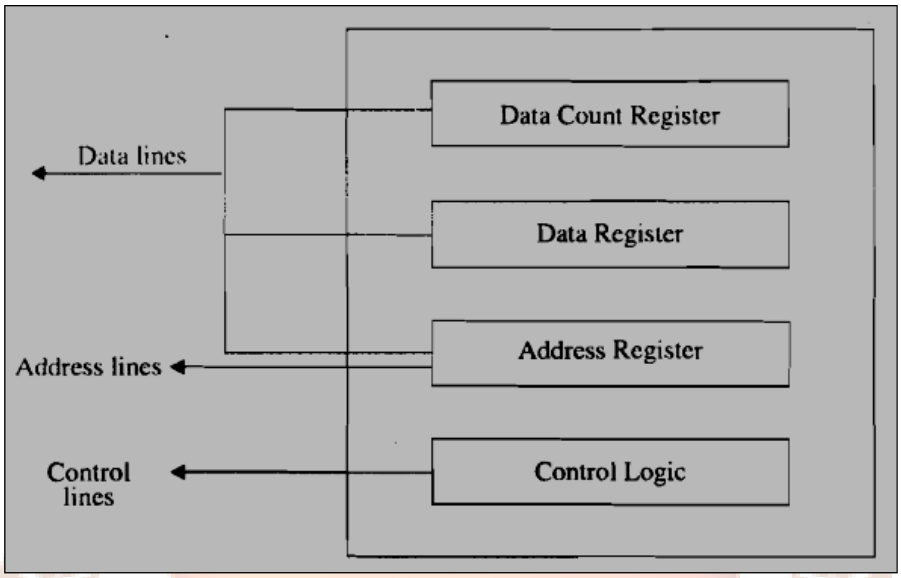

Figure 10.1: Registers on DMA Module

DMA Data transfer modes and their operations

Direct memory access data transfer can be worked in two modes: burst mode or single cycle mode. Let us study both.

1. **Burst Mode:** In burst mode, the DMA controller maintains control of the bus till the entire data has been moved to (from) memory from (to) the peripheral device. Such mode of transfer is required for quick devices where data transfer cannot be terminated until the whole transfer is completed.
2. **Single-cycle mode:** In single-cycle mode (cycle stealing), the DMA controller gives up the bus following every transfer of a single data word. This reduces the duration of time that the DMA controller prevents the CPU from monitoring the bus, however, it needs that the bus request/acknowledge sequence be carried out for every single transfer. Such overhead may result in a decline in performance.

The single-cycle mode is selected if the system is not able to tolerate higher than a few cycles of extra interrupt latency or when the peripheral devices can buffer quite a large quantity of data, making the DMA controller keep the bus busy for an extreme amount of time.

Activity 1

Find out the way data transfer from disk to memory is performed under eachof the following I/O schemes: interrupt-driven I/O, programmed I/O and DMA. Depict the steps undertaken in every case.

Self-assessment questions -2

3. There are _____ modes of data transfer to and from peripherals.
4. DMA technique is most suitable for slow devices. (True/False)

4. INTEL 8237

Let's first define Intel 8237. The 8237 is a DMA Controller that provides the memory as well as I/O with memory address information and control signals at the time of the DMA transfer. The 8237 is in reality a special-purpose microprocessor that has the job of high-speed data transfer between the I/O devices and memory. Figure 10.2 shows the pin diagram of the 8237DMA Controller.

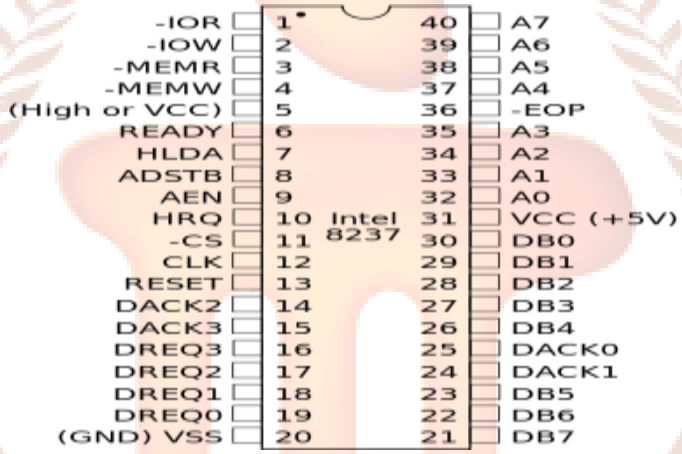

Figure 10.2: Pin Diagram of 8237

Intel 8237 was utilized like a DMA controller in the earliest IBM XT and IBM PC. Afterward, IBM-compatible personal computers consisted of chipsets that imitate the role of the 8237 in case of backward compatibility.

Features of 8237: Although the 8237 was introduced with the 8-bit 8085 processor family, it is compatible with the 8086/88 microprocessors. Some of the important features of the 8237 Intel processor are mentioned below:

i) Four independent DMA channels.
ii) Direct memory to memory transfer is possible.
iii) Independent auto initialization of all characters.
iv) Supports the software DMA requests.
v) Directly expandable to any number of DMA channels to be cascaded.
vi) Every channel can address 64k addresses with word count capabilities.
vii) The maximum data transfer rate is 1.6MB/Sec.

viii) It has the necessary logic for supporting peripheral subsystems, floppy disks, hard disks

Self-assessment questions -3

5. Intel 8237 contains _____ an independent DMA channel.
6. The maximum data transfer rate for Intel 8237 is 2.6MB/Sec. (True/False)

5. BUSES

You must remember that a bus depicts a physical link utilized to transmit a signal from one point to the other. Buses are of four types based on the signal carried by them: data, address, power, and control buses.

Data buses are used to transmit data, control buses are used to transmit control signals, address buses transmit the memory address and power buses transmit the power-supply/ground voltage. The size (number of lines) of the control, data, and address bus differ from one system to the other.

5.1 Bus arbitration

Bus arbitration is essential to solve conflicts in the condition when two or more devices wish to become the bus master simultaneously. Hence, arbitration is the process of selection of the next bus master amid several candidates.

These conflicts are capable of being resolved by the use of centralized or distributed schemes.

In centralized arbitration schemes, one arbiter is deployed to choose the next master. In the case of a decentralized arbitration scheme priority-based arbitration is utilized. Here, every potential master contains a unique arbitration number which is utilized for solving conflicts while multiple requests are presented.

5.2 Types of buses

In an asynchronous bus data transfer on the bus is monitored by a bus clock. The clock plays the part of a timing reference for every bus signal. Synchronous buses are simple and are also easy to implement. But, when linking devices with different speeds as compared to a synchronous bus, the slowest device will find out the speed of the bus.

A bus is asynchronous when data transfer on the bus depends upon the accessibility of the data and not on a clock signal.

Self-assessment questions - 4

7. In centralized arbitration schemes, a single arbiter is deployed to choose the next master. (True/False?)

6. I/O INTERFACES

You will come to know that an I/O interface is needed every time the I/O device is directed by the processor. The interface should possess essential logic to decode the device address produced by the processor Handshaking must be implemented by way of the interface utilizing proper commands (like READY, BUSY and WAIT), and the processor should be able to communicate with an I/O device via the interface.

In case varied data formats happen to be exchanged, the interface should be able to transform serial data to parallel form as well as vice-versa. There should be provision for producing interrupts and the matching type numbers for additional processing by the processor when needed.

The input-output interface offers a way for transferring information between I/O devices and internal memory. Peripherals linked to a computer need special communication connections for interfacing them along with the central processing unit. The reason behind the communication link is to solve the differences which exist between every peripheral and the central computer.

I/O Bus and Interface Modules: A communication link between several peripherals and the processor is depicted in figure 10.3.

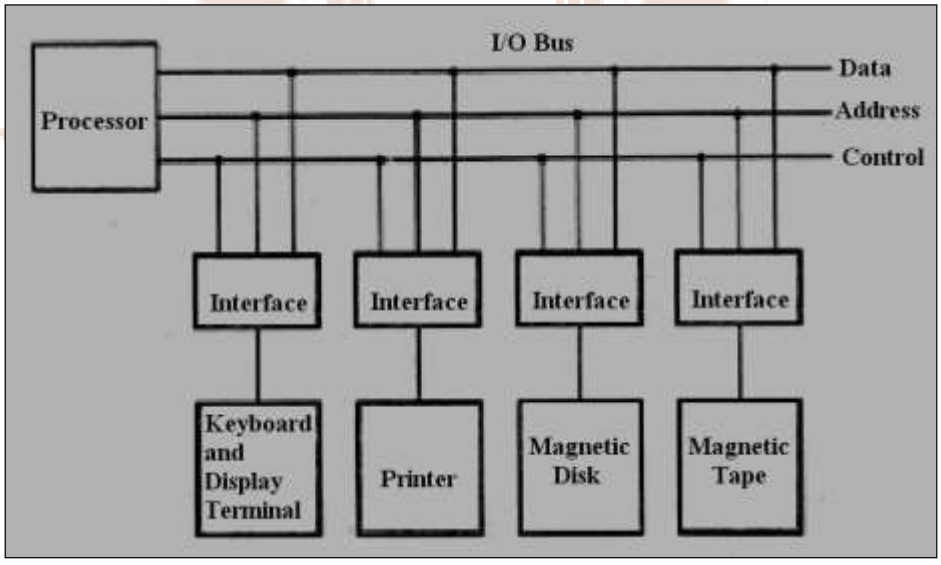

Figure 10.3: Connection of I/O Bus to Input-Output Devices

The I/O bus is comprised of address lines, control lines, and data lines.

In all general-purpose computers, the terminal, magnetic disk, and printer are utilized. The magnetic tape is used for backup storage in computers. Every peripheral device is linked with it via the interface unit. Every interface interprets the address and control acquired from the I/O bus, decodes them for the peripheral as well as offers signals for the peripheral controller. It also coordinates the data flow and controls the data transfer between the processor and peripheral. Every peripheral has its personal controller which operates the specific electromechanical device.

A controller might be housed independently or might be physically attached to the peripheral. The I/O bus from the processor is integrated into all peripheral interfaces, The processor puts a device address on the address lines in order to communicate with a particular device. Every interface integrated with the I/O bus consists of an address decoder that maintains a record of the address lines. As soon as the interface notices its address, it turns on the path between the device that it controls and the bus lines. Every peripheral whose address does not match with the address in the bus is disabled by its interface.

The address is made accessible in the address lines and the processor offers a function code in the control lines. The interface chosen reacts to the function code and advances to implement it. The function code is regarded as an I/O command and is in reality an instruction that is implemented in the interface and its integrated peripheral unit. The interpretation of the command relies upon the peripheral which the processor is addressing.

An interface might receive four types of commands as you can see in figure 10.4.

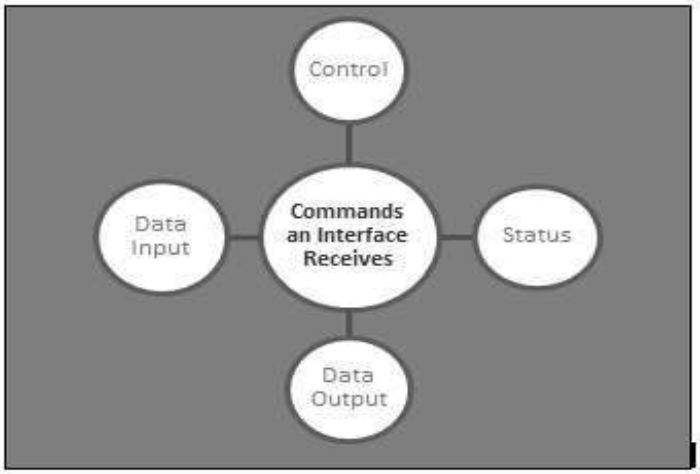

Figure 10.4: Commands Received by an I/O Interface

- **Control:** We release a control command to make the peripheral active.
- **Status:** We utilize a status command to check several status conditions in the peripheral and the interface.
- **Data Output:** A data output command makes the interface react by transferring data from the bus to one of its registers.
- **Data Input:** By providing the data input command the interface gets an item of data from the peripheral and puts it in its buffer register.

Self-assessment questions - 5

8. The data transfer rate of peripherals is normally slower compared to the transfer rate of the CPU. (True/False?)
9. We issue a _____ to activate the peripheral.

7. SYNCHRONOUS AND ASYNCHRONOUS DATA TRANSFER

You will find it interesting that asynchronous and synchronous communication represents methods through which signals are transferred in computing technology. Such signals permit computers to move data between components inside the computer or between an external network and the computer.

The majority of the operations and actions which occur in computers are carefully controlled and happen at particular times and intervals. The data transfer on the system bus might be synchronous or asynchronous.

7.1 Synchronous data transfer

In synchronous data transmission, data is transmitted through a bit-stream, that transmits a group of characters in a single stream. In this type of data transfer, the transmission speed is synchronized at both the sender and receiver with the help of a clock signal, at the time of transfer.

A particular activity that might utilize a synchronous protocol can be the transmission of files from one point to the other. As every transmission is acquired, a reaction is returned depicting success or the requirement to resend.

7.2 Asynchronous data transfer

The word asynchronous is normally used to portray communications in which data are able to be transmitted irregularly instead of in a steady stream. Asynchronous systems do not send separate information to indicate the encoding or clock information. The receiver must decide the clocking of the signal itself.

The trouble with asynchronous communications is that the receiver should have a method to differentiate between noise and valid data. In computer communications, this is normally acquired via a special start bit and stop bit at the starting and end of every piece of data. Due to this reason, asynchronous communication is at times known as start-stop transmission.

Self-assessment questions - 6

10. Asynchronous communication is sometimes called _____ transmission.
11. Transmission of files from one point to the other is an example of_____ transmission.

8. PARALLEL I/O 8255

After reading further you will know that Programmable Peripheral Interface is a useful device for interfacing peripheral devices. It is a multipart device that can be programmed by the programmer. It is able to be programmed to move data under several conditions, from simple I/O to interrupt I/O.

The Intel 8255 is a Programmable Peripheral Interface (PPI) chip that was initially created for the Intel 8085 microprocessor, and by itself is a member of a large variety of such chips, called the MCS-85 Family.

It is an IC i.e. 8255. It is used in a combination with a microprocessor for the application of complex control algorithms. It is used because of the incapability of a micro-controller to achieve the same

It is made in DIP (Dual-in-line package) 40 and PLCC (a plastic leaded chip carrier) 44 pins encapsulated versions. The 8255 is a programmable, parallel I/O device simply called Programmable Peripheral Interface (PPI).

The main features of the 8255 Programmable Peripheral Interface are:

- It has two 8 bit ports: Port A, Port B, and two 4 bit ports: C_{UPPER} and C_{LOWER}.
- It can be programmed to transfer data in 3 modes of I/O: Mode 0, Mode 1, and mode 2. PA can be set for modes 0, 1 and 2. PB for 0, 1 and PC for mode 0 and for BSR. Modes 1 and 2 are interrupt-driven modes.
- It provides 24 I/O pins that can be grouped into three 8-bit parallel ports: PORT A, PORT B, and PORT C.
  - PA0-PA7- 8-bits of port A
  - PB0-PB7- 8-bits of port B
  - PC0-PC3- 4-bits of port C lower
  - PC4-PC7- 4-bits of port C upper
- The 8-bits of port C are separated into two 4-bit ports: PORT C UPPER (PCU=PC4-PC7) and PORT C LOWER (PCL=PC0-PC3)

- The three ports are grouped into two groups A and B. PA and PCU form Group A while PB and PCL form Group B
- It is TTL compatible.

Operational modes of 8255: 8255 has two key operational modes:

1. **Input/output mode:** There are three kinds of the input/output mode i.e. Mode 0, 1, and 2.

   In mode 0, the ports can be utilized for simple input/output operations with no handshaking. It could be either utilized as I/P (input port) or O/P (output port). Mode 1 supports handshaking. Mode 2 is used for bi-directional handshaking data transfer. Mode 2 is used only for port A. When port A is programmed in mode 2 it can be used in either mode 0 or mode 1.

2. **Bit set/reset mode:** In this mode, only port B can be utilized (as an output port). Every line of port C (PC0 - PC7) is able to be set/reset by appropriately loading the command word register. There is no effect in input-output mode. The individual bits of port C have the ability to set or reset by conveying the signal OUT instruction to the control register.

Self-assessment questions - 7

12. PPI stands for _____ .
13. 8255 parallel I/O consists of three _____ bit IO ports PA, PB, PC.

9. SERIAL I/O 8251

In the case of serial communication, the interface gets a byte of data from the CPU and sends it bit by bit to the other system serially or it receives data bit by bit serially from the external system, then converts the data into bytes and sends it to CPU. Serial communication is mostly used while transmitting the data over a long distance. It transfers one bit at one time over a single line. 8251 is a programmable I/O device designed specifically for serial I/O. It is also called Universal Synchronous Asynchronous Receiver Transmitter (USART) chip. It is designed for both synchronous and asynchronous serial communication. The main features of serial I/O 8251 are:

- It supports both synchronous and asynchronous modes of data transfer.
- It contains a full-duplex double-buffered system
- It provides error detection to detect parity and framing errors.
- It's compatible with Intel processors
- Synchronous baud rate: 0-64k baud (The rate at which bits are transmitted is called baud rate. Baud rate = Bits / Second)
- Asynchronous baud rate: 0-19.2k baud
- 28 pin DIP package, TTL compatible

Self-assessment questions - 8

14. 8251 supports both synchronous and asynchronous mode of data transfer. (True/False)
15. Serial I/O 8251 contains _____ duplex double buffered system.

10. PCI

You will be surprised to know that the Peripheral Component Interconnect (PCI) bus was initially created as a local bus expansion for the ISA (Industry Standard Architecture)/EISA (Extended Industry Standard Architecture) (PC/AT) bus. The initial version of the PCI bus performed at 33MHz with a 32-bit bus (133MBps) however the recent version performs at 66MHz with a 64-bit bus. The PCI bus performs either asynchronously or synchronously along with the motherboard clock rate. While operating asynchronously, the bus will function at any frequency till the maximum (66MHz). Flow control is utilized to allow the bus to function with slower devices. The bus is un-stopped and the bus clock functions at 133 MHz.

PCI gives support to full device bus mastering. Full device bus mastering is a method that makes a controller linked to the bus to communicate straight with other devices on the bus with no going through the CPU. Basically, the I/O device has the ability to perform more complex sequences of I/O operations in the absence of CPU intervention. PCI provides bus arbitration facilities via the system chipset. PCI architecture permits bus mastering of multiple devices on the bus simultaneously, with the arbitration circuitry performing to make sure that no device on the bus (including the processor) locks out any other device.

Although, in the situation that no other device requires access to the bus, PCI will permit a bus master to move data at the maximum allowable rate. Observe that, with few initial motherboards it may be promising that not all the existing PCI bus slots will be competent for bus mastering. In case of doubt, it is advisable to confirm with the motherboard manual.

The PCI standard is a part of the Plug and Play standard created by Intel, Microsoft, and many other companies where the PCI chipset tackles the identification of cards, performing in combination with the BIOS (basic input output system) and functioning to automatically assign resources for well-matched peripheral cards.

The PCI bus utilizes its personal internal interrupt system for handling the requests from the cards on the bus. Such interrupts are frequently known as "#A", "#B", "#C", and "#D" to prevent confusion with the normal numbered system IRQs, (interrupt requests).

PCI interrupts are mapped to the normal system interrupts (usually IRQ9 to IRQ12). This forces a limit of four interrupts available for PCI devices. In case more slots are offered (or in case a USB controller is there) various PCI devices may be organised to share an IRQ.

Self-assessment questions - 9

16. The PCI bus works either synchronously or asynchronously with the motherboard clock rate. (True/False)
17. PCI supports full device bus mastering and offers bus arbitration facilities through the _____.

11. SCSI BUS

We will let you know that SCSI represents Small Computer Systems Interface. It is an ANSI standard that has turned into one of the most important I/O buses in the computer industry. The SCSI interface is a local bus type interface needed for linking multiple devices (up to eight), selected as either target (receivers) or initiators (drivers). ANSI X3.131 – 1986 is the official name of the SCSI standard. The important features of the SCSI bus are shown in table 10.1.

Table 10.1: Features of SCSI

SCSI addresses	SCSI utilizes a 3-bit addressing scheme, in which every device has designated an address varying from 0 to 7. Device 7 has the topmost priority, thus the host computer is normally designated to be device 7.
Initiator/Target	Communication happens as soon as the initiator (client), whois particularly the host computer, initiates a request, and the target (server) works on the request. The SCSI allows all devices to communicate with one another; however few devices are executed in such a manner that they are not able to start communications.
Protocols	SCSI devices can utilize either synchronous or asynchronous communication protocols. In the initial SCSI arrangement, synchronous communication permitted speeds of 5 Mb/sec. Observe that if your SCSI bus is small, asynchronous communication can be quick.
SCSI Variants	SCSI comes in four variants, SCSI-1, SCSI-2, SCSI-3, and LVD SCSI.

SCSI Bus termination: Reflected signals intrude with the "real" data on the bus and cause data corruption and signal loss. Therefore SCSI bus needs to be ended. Specific devices are utilized which make the bus look as if it is infinite in length *electrically*. Any signals sent with the bus seem to go to all devices as well as later disappear, without any reflections.

Several techniques are used for SCSI bus termination. These are forced perfect termination (FPT), Low Voltage Differential (LVD) terminations, passive termination, High Voltage Differential (HVD), and active termination.

Terminators should be present at the very ends of the bus, subsequent to all the real devices on the chain. So, there are at all times exactly two terminators per bus segment or bus. Terminators can be either internal terminators or external terminators.

Activity 2

Conduct a secondary research on various types of SCSI bus termination techniques. Find out whether your system has an external or internal terminator.

Self-assessment questions - 10

18. SCSI devices can utilise either synchronous or asynchronous communication protocols. (True/False)
19. _____is mainly found in high-end systems.

12. SERIAL I/O

Now we will study the Serial I/O interface. Electronic data communications between elements can be broadly classified into two categories: single-ended and differential. Single-ended I/O has been the the standard for years. In single-ended systems, one signal connection is made between the two ICs.

With the advancement of technology, IC communication speeds increased, therefore system and IC designers began to look for signaling methods that could support higher speed (Figure 10.5).

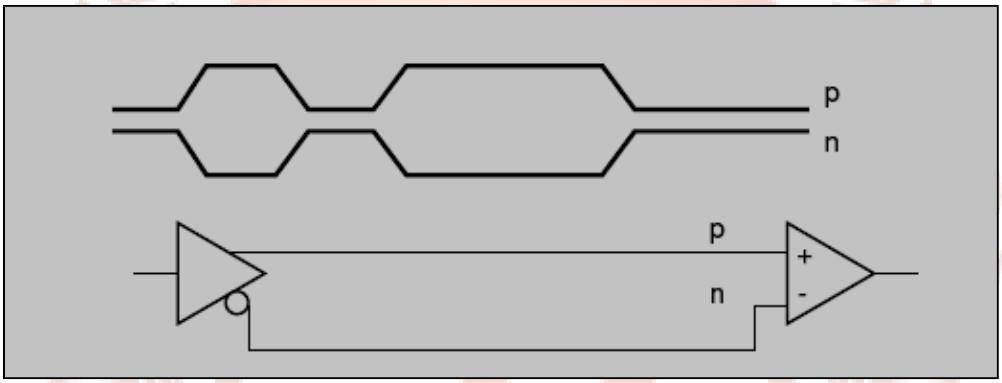

Figure 10.5: Signalling Methods

Differential signaling was a solution to this need. It has various advantages over single-ended signaling. The various advantages are given below:

1. The first advantage is the immunity from the noise in the ground plane.
2. Immunity to Crosstalk/Electromagnetic interference
3. A very high data rate is possible by the use of differential signaling.
4. The differential signaling uses a very small amount of voltage which saves power.

RS-232: RS-232 (Recommended standard-232) is a standard interface accepted by the Electronic Industries Association (EIA) for linking serial devices. We can also say that RS-232 is a long-recognized standard that explains the protocol and the physical interface for comparatively low-speed serial data communication between related devices and computers.

The Electronic Industries Association (EIA), an industry trade group, defined it initially as teletypewriter devices. In 1987, the EIA published the latest version of the standard and modified its name to EIA-232-D. Most of the people, however, still call it RS-232C, or simply RS- 232.

RS-232 is the interface which your computer utilizes to communicate with as well as exchange data with your serial devices and modem. The serial ports on the majority of the computers utilize a subset of the RS- 232C standard.

Limitations of RS-232: RS-232 has a few severe disadvantages as an electrical interface which are discussed below.

- **High noise:** A signal resting on a single line is not possible to screen efficiently for noise. Through screening of the entire cable, one can lessen the effect of external noise, however, internally produced noise continues to be a problem.
- **Requires a common ground:** Voltage levels in relation to ground signify the RS-232 signals. A wire exists for every signal, along with the ground signal (reference for voltage levels). Such an interface is beneficial for point-to-point communication at reduced speeds.

Self-assessment questions - 11

20. Serial ports driver ICs can be broadly classified into_____ categories.
21. DCE is the abbreviation for _____.

13. CASE LET: PROGRAM CONTROLLED I/O

One common I/O strategy is *program-controlled* I/O, (often called *polled* I/O). Here all I/O is performed under the control of an "I/O handling procedure,'' and input or output is initiated by this procedure.

The I/O handling procedure will require some status information (handshaking information) from the I/O device (e.g., whether the device is ready to receive data). This information is usually obtained through a second input from the device; a single bit is usually sufficient, so one input "port'' can be used to collect status or handshake information from several I/O devices. (A *port* is a name given to a connection to an I/O device; *e.g.*, to the memory location into which an I/O device is mapped). An I/O port is usually implemented as a register (possibly a set of D flip flops) which also acts as a buffer between the CPU and the actual I/O device. The word *port* is often used to refer to the buffer itself.

Typically, there will be several I/O devices connected to the processor; the processor checks the "status'' input port periodically, under program control by the I/O handling procedure. If an I/O device requires service, it will signal this need by altering its input to the "status'' port. When the I/O control

the program detects that this has occurred (by reading the status port) then the appropriate operation will be performed on the I/O device which requested the service. The outputs labeled "handshake in'' would be connected to bits in the "status'' port. The input labeled "handshake in'' would typically be generated by the appropriate decode logic when the I/O port corresponding to the device was addressed.

Program-controlled I/O has a number of advantages:

- All control is directly under the control of the program, so changes can be readily implemented.
- The order in which devices are serviced is determined by the program, this order is not necessarily fixed but can be altered by the program, as necessary. This means that the "priority'' of a device can be varied under program control. (The "priority'' of a device

determines which of a set of devices that are simultaneously ready for servicing will actually be serviced first).

- It is relatively easy to add or delete devices.

Perhaps the main disadvantage of program-controlled I/O is that a great deal of time may be spent testing the status inputs of the I/O devices when the devices do not need servicing. This "busy wait'' or "wait loop'' during which the I/O devices are polled but no I/O operations are performed is really time wasted by the processor, if there is other work that could be done at that time. Also, if a particular device has its data available for only a short time, the data may be missed because the input was not tested at the appropriate time.

Program-controlled I/O is often used for simple operations which must be performed sequentially. For example, the following may be used to control the temperature in a room:

DO forever

INPUT temperature IF (temperature <setpoint) THEN

turn heat ON

ELSE

turn heat OFF

END IF

Note here that the order of events is fixed in time, and that the program loops forever. (It is really waiting for a change in the temperature, but it is a "busy wait.'')

Question: Analyse the major advantages and disadvantages of the parallel I/O technique.

(Hint) The Parallel I/O technique offers greater control to the programmer and the major disadvantage is that it is time-consuming.

14. SUMMARY

In this unit, you have studied the basic concepts of DMA and the important concepts relating to I/O such as synchronous and asynchronous data transmission, PCI bus, etc. Let us now summarise the important concepts discussed in this unit:

- DMA approach is often used to transfer large blocks of data at high Speed, between external devices & main Memory. DMA controller permits data transfer directly between memory and I/O device, with minimal intervention of processor.
- In Asynchronous data transfer, the internal timing in every unit is separate from the other and two separate lines are used for different directions of data flow.
- Intel 8237 is a direct memory access (DMA) controller, a division of the MCS 85 microprocessor family.
- 8251 is a programmable USART chip designed for synchronous and asynchronous serial communication.
- PCI stands for Peripheral Component Interface 'PCI' Bus and it works either synchronously or asynchronously with the motherboard clock rate.
- RS-232 is the interface that your computer utilises to communicate to and exchange data with your serial devices as well as modem.

15. GLOSSARY

- **Asynchronous:** An operation is asynchronous if it is not executed in with clock.
- **DCE**: Data Communications Equipment e.g. Modem
- **Direct Memory Access (DMA):** Transferring Data directly to and from memory without the need of CPU.
- **DTE:** Data Terminal Equipment. For example, computers, printers, etc
- **Input-output interface**: Input-output interface gives a method for transferring information between internal memory and I/O devices.
- **Intel 8237:** Direct memory access (DMA) controller, a part of the MCS 85 microprocessor family.
- **Intel 8255:** It is a Programmable Peripheral Interface chip originally developed for the Intel 8085 microprocessor
- **PCI:** Peripheral Component Interface
- **RS-232:** The interface that your computer utilizes to communicate to and exchange data with your serial devices as well as a modem.

16. TERMINAL QUESTIONS

1. Explain the concept of DMA. For which type of devices is the DMA approach most useful?
2. Discuss the important characteristics of 8237.
3. What do you understand by the term I/O bus? What are its components?
4. Discuss the various types of commands that an interface may receive.
5. Describebriefly synchronous and asynchronousdata transfer techniques
6. Explain the purpose of I/O interface.
7. Describe the main features of a parallel I/O 8255
8. Briefly explain the important features of serial I/O 8251.
9. Describe briefly PCI bus and its importance.
10. Write a short note on Serial I/O.
11. Briefly describe RS 232 and its limitations.

17. ANSWERS

Self Assessment Questions

1. Interrupt-driven I/O
2. True
3. Three
4. False
5. Four
6. False
7. True
8. True
9. Control command
10. Start/stop
11. Synchronous
12. Programmable parallel I/O
13. Eight
14. True
15. Full
16. True
17. System Chipset
18. True
19. SCSI-3
20. Three
21. Data Communications Equipment

Terminal Questions

1. DMA is a sensible approach for devices that have the capability of transferring blocks of data at a very high data rate, in short bursts. Refer Section 3.
2. Intel 8237 is a direct memory access (DMA) controller. Refer to section 4.
3. The I/O bus is made of data lines, address lines, and control lines. Refer Section 5.
4. There are four types of commands that an interface may receive. They are classified as control, status, data output, and data input. Refer Section 5.

5. Synchronous communication requires that Every end of an exchange of communication respond in turn without initiating a new communication While in the asynchronous transmission data can be transmitted intermittently rather than in a steady stream. Refer Section 6.
6. I/O interface is used to communicate with the various I/O devices. Refer Section 10.6
7. The Intel 8255 is a parallel I/O Programmable Peripheral Interface chip originally developed for the Intel 8085 microprocessor. Refer Section 7.
8. 8251 is a programmable USART chip designed for synchronous and asynchronous serial communication. Refer Section8.
9. PCI stands for Peripheral Component interface. PCI is the highest performance general I/O bus currently used on PCs. Refer Section 9.
10. Electronic data communications between elements can be broadly classified into two categories: single-ended and differential. Refer Section 11.
11. RS-232 (Recommended standard-232) is a standard interface approved by the Electronic Industries Association (EIA) for connecting serial devices. Refer Section 11

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