Filter Design of Direct Matrix Converter for Synchronous Applications

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***Abstract*—Filters for switching ripple attenuation are essential at the input, and sometimes at the output for certain applications, for the deployment of matrix converters (MCs). Due to the absence of inertial elements in the MC structure and the consequent tight input–output coupling, the filter parameters significantly affect its dynamic behavior. This paper presents an exhaustive filter design method for synchronous applications of the MC in power systems. Apart from the usual considerations of ripple attenuation, voltage regulation, reactive current loading, and internal losses, this paper also addresses additional constraints which may be imposed by requirements of dynamic performance and reliable commutation. Rigorous analytical justification of each design step is provided and the sequential design process is summarized. Relevant experimental results are presented to validate the proposed design tool.**

***Index Terms*—Filter design, matrix converter (MC), synchronous applications.**

I. Introduction

RECENT YEARS have witnessed a growing interest [1]–[7] toward the deployment of the matrix converter (MC) in power systems, which are synchronous applications characterized by identical input and output frequencies. The advantage of reduced energy storage needs has inspired the use of MC as a FACTS device [1]. The use of MC for power quality improvement, reactive power control, and other power system applications has been reported in [2]–[4]. Benefits of using MC as a voltage regulator in a distribution system and as a high-performance power supply have been reported in [5]–[7], respectively. The input filter is an essential requirement of this topology for providing a local circulating path to the switching frequency current. Some of the synchronous applications require regulated output voltage and, hence, a second-order ripple filter at the output side, in addition to the input filter. The filter parameters have to be carefully selected such that their inclusion does not degrade voltage regulation, efficiency, and reactive current loading beyond an acceptable limit. Since the only inertial elements in this topology are the filter components, the filter parameters significantly affect the system dynamics.

Input filter design has been discussed in [8]–[13], where, from cost and weight considerations, the single-stage LC filter has been found to be the most appropriate topology. Although the set of filter elements (L_f, C_f) for a particular resonant frequency is infinite, Klumpner *et al.* [9] advocate a maximum C_f to ensure a minimum input displacement factor (IDF) for low loads. However, in a distribution system, most of the loads are inductive, and this restriction may be relaxed at lighter loads. An exhaustive treatment of input/output filters with focus on reducing electromagnetic interference and common-mode voltages has been provided in [14] and [15]. However, most of these have not investigated the comprehensive design of filters in the context of dynamic performance improvement or reliability of commutation hardware. The only reported approach [13], which considers both steady-state and dynamic objectives, uses a genetic algorithm to derive the parameter values as well as the filter topology. Dynamic stability criteria are based on limits detailed in [16] and [17]. Digital filters are used for measuring input voltage which are purported to improve the system stability limit. It has, however, been shown in [18] that, with a proper choice of system input and output, the derived plant has minimum phase poles for all operating points, but nonminimum phase zeros could appear, depending on input filter parameters and system operating points. Since the plant is inherently stable, imposing a general stability limit on filter design for all operating conditions [13] is unnecessary. Also, analytical justification of the filter design method is not established with any degree of rigor.

Output voltage regulation specifications restrict the inductive (series) component of the output filter. Hence, commutation based on output current direction becomes particularly difficult at zero crossing (ZC) due to the high ripple content. The detection of current direction based on switch voltage measurement introduces large delays because of the stray capacitances and large resistances used [19]–[21]. An analysis of the critical window area around the ZC of line voltages, for safe voltage-based commutation (VBC), has been provided in [22]. However, the effect of switching frequency ripple in input voltage on the demarcation of the critical areas has been ignored. In [21], it is shown that, with proper zero vector placement in space vector modulation (SVM), safe commutation can be achieved in spite of voltage measurement inaccuracies. This method is restricted to the operation with the input displacement angle within $\pm\theta^\circ$ of the voltage ZC, which is to be decided on the basis of the specific input ripple voltage measurements for a given hardware. A closed-form expression of the ripple voltage

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TABLE I
NOMINAL/RATED PARAMETERS

Base frequency (f_b)	Source voltage (per phase) (V_s)	Switching frequency (f_s)	Output current (per phase) (I_o)
50 Hz	240 V	10 kHz	10 A

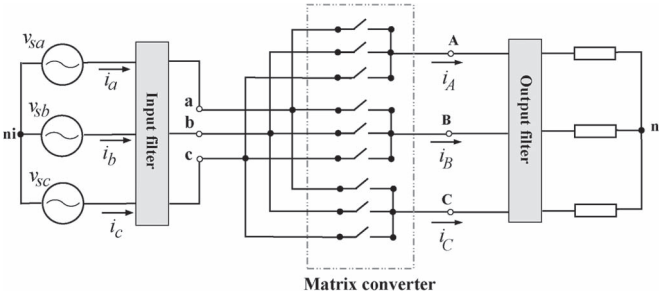

Fig. 1. Schematic of a 3 Ph MC.

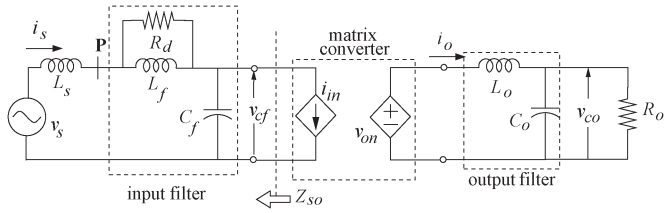

Fig. 2. Single-phase diagram including source inductance.

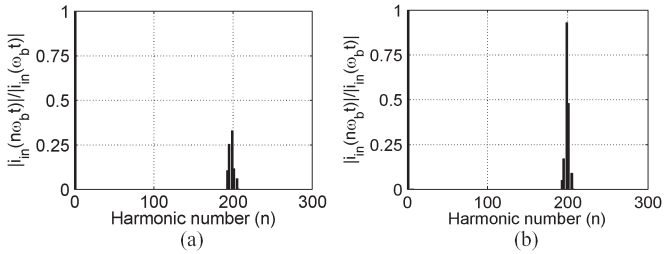

Fig. 3. $|i_{in}(n\omega_b t)|/|i_{in}(\omega_b t)|$ for (a) $m = 1$ and (b) $m = 0.5$.

would therefore provide a complete analytical design tool for this method. For wider control of IDF in applications [23], [24] requiring input reactive power control, the correct measurement of the ripple voltage is still difficult, particularly with high output current amplitude.

This paper discusses a filter design approach for the MC which integrates the steady-state performance along with the constraints imposed by the requirements of closed-loop dynamic performance and safe commutation. In the first section, the design of filters to meet certain steady-state performance specifications is detailed. Since modulation strategies for MC do not provide any separate control on the input current amplitude, an external damping resistor is included. Power loss estimation due to this inclusion is presented. Input capacitor sizing for reliable commutation is analyzed in the context of the voltage ripple and consequent problems in VBC. Then, the effect of the grid inductance has been presented. Thereafter, the output filter design is presented in the second section. In the next section, the design guidelines that emerge from the analysis have been summarized to enable a sequential design process. Finally, relevant experimental results on a 6-kVA laboratory prototype are provided for validation.

II. INPUT FILTER DESIGN

Filter parameters are chosen for the nominal/rated system parameters shown in Table I. In this analysis, an application requiring regulated 3 Ph sine-wave voltage supply has been considered which makes output ripple filters mandatory. Fig. 1 shows the schematic diagram of a 3 Ph MC. The single-phase equivalent of the overall system is shown in Fig. 2 where the Thevenin impedance of the source is modeled as an inductance L_s. The input filter damping resistor is placed across the filter inductor as the conflict between filter efficiency and damping requirements is least with this arrangement [25].

The power stage of MC appears as a current stiff sink to the supply side and as a voltage stiff supply to the load. A phase-locked loop is locked to phase a of the point of common coupling marked as **P**. L_s, which is usually small at the distribution level, is initially neglected and would be introduced later to study its impact on filter performance. The selection of filter parameters to satisfy certain criteria are sequentially described in the following sections.

A. Attenuation to Switching Ripple and Low-Order Harmonics

For $L_s = 0$, the forward gain of the input filter is defined as

$$G_{fv}(s) \triangleq \left.\frac{i_s(s)}{i_{in}(s)}\right|_{v_s} = \left.\frac{v_{cf}(s)}{v_s(s)}\right|_{i_{in}} = \frac{s\frac{L_f}{R_d}+1}{s^2 L_f C_f + s\frac{L_f}{R_d}+1}. \quad (1)$$

Denoting the corner frequency as $\omega_c : (2\pi f_c)$, the normalized form of its frequency response magnitude is

$$|G_{fv}(j\omega)| = \sqrt{\left[1+\frac{r_\omega^2}{Q^2}\right] \Big/ \left[(1-r_\omega^2)^2 + \frac{r_\omega^2}{Q^2}\right]} \quad (2)$$

which is plotted in Fig. 4. The definitions

$$r_\omega = \frac{\omega}{\omega_c}, \quad Q = R_d\sqrt{\frac{C_f}{L_f}}, \quad \omega_c = \frac{1}{\sqrt{L_f C_f}} \quad (3)$$

enable generalized analysis.

The ratio of the magnitude of the switching ripple components to the fundamental component in i_{in} varies with modulation index m [26]. Fig. 3 shows the magnitude of these component as a fraction of the fundamental obtained from simulation.

To restrict these switching ripple components from appearing in i_s, the first design criterion is set as

Spec.1 $|G_{fv}(j2\pi f_s)| \leq A_{sw}$ dB.

Also, in the deployment site of the MC, the grid voltage spectrum may contain significant low-order (h_v) harmonics. To limit the appearance of these in the filter capacitor voltage v_{cf}, the following restriction is introduced:

Spec.2 $|G_{fv}(j2\pi f_b \max.(h_v))| \leq A_{vh}$ dB.

Defining the following frequency ratios:

$$m_{fhb} = \max.(h_v) \quad \text{and} \quad m_{fsh} = \frac{\omega_s}{m_{fhb}\omega_b} \quad (4)$$

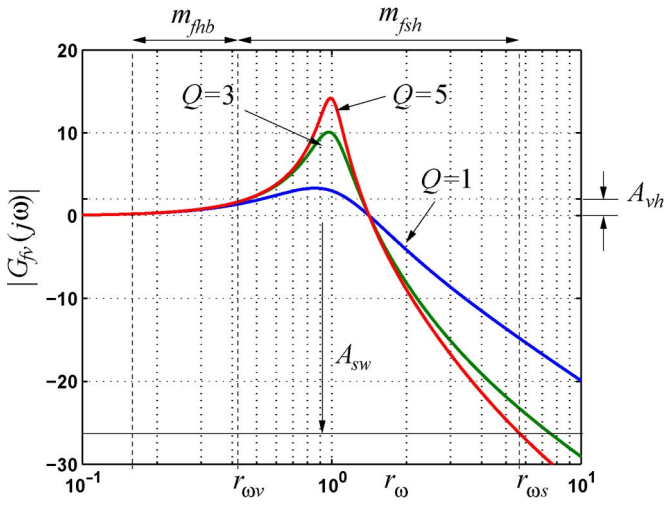

Fig. 4. $|G_{fv}(j\omega)|$(dB) with $Q = 1, 3,$ and 5.

TABLE II
Q AND f_c FROM FORWARD GAIN

A_{sw}	max.(h_v)	A_{vh}	$Q^{(1)}$	$f_{c,\max}^{(1)}$	$f_{c,\min}^{(1)}$
-26 dB	7	2 dB	3	1.35 kHz	772 Hz

it is noted that, for given switching frequency and deployment site conditions, these ratios have unique values. These are depicted in Fig. 4 by the vertical lines which are mutually stationary but could slide horizontally. Also included are the criteria defined in **Spec.1** and **Spec.2**, which are depicted as regions demarcated by stationary horizontal lines. The interval $[r_{\omega v}, r_{\omega s}]$ defines the initial choice of Q ($Q^{(1)}$) and, thereby, the acceptable range of f_c ($[f_{c,\min}^{(1)}, f_{c,\max}^{(1)}]$). For the experimental model and deployment site of MC, these selections, along with the numerical limits of **Spec.1** and **Spec.2**, are listed in Table II.

B. Voltage Regulation and Reactive Current Loading

Referring to Fig. 2, the full load regulation of MC output voltage is decided by the fundamental voltage drop in L_f. Restriction on regulation leads to the following design criterion:

Spec.3 $V_{Lf} \approx \omega_b L_f \sqrt{I_{cf}^2 + I_{in,\text{rated}}^2} \leq k_{\mathcal{R}} V_s$.

A restriction on reactive current loading is necessary for satisfying stipulations on part-load power factor, which leads to the next criterion

Spec.4 $I_{cf} \approx \omega_b C_f V_s \leq k_{\mathcal{PF}} I_{in,\text{rated}}$.

For deriving the boundary values at rated power level, analysis is done considering unity IDF operation with unity modulation index (m) [27] and resistive load unless stated otherwise. The specific inequalities in **Spec.3** and **Spec.4** obviously translate to maximum limits for L_f ($L_{f,\max}^{(1)}$) and C_f ($C_{f,\max}^{(1)}$). The rated input current is evaluated from [27]

$$I_{in,\max} = 0.866 I_o. \tag{5}$$

For the rated values in Table I, numerical limits considered for **Spec.3** and **Spec.4**, along with the maximum allowable values $L_{f,\max}^{(1)}$ and $C_{f,\max}^{(1)}$, are listed in Table III.

TABLE III
$L_{f,\max}$ AND $C_{f,\max}$ FROM REGULATION AND REACTIVE LOADING

$k_{\mathcal{PF}}$	$k_{\mathcal{R}}$	$L_{f,\max}^{(1)}$	$C_{f,\max}^{(1)}$
0.2	0.03	2.6 mH	22 μF

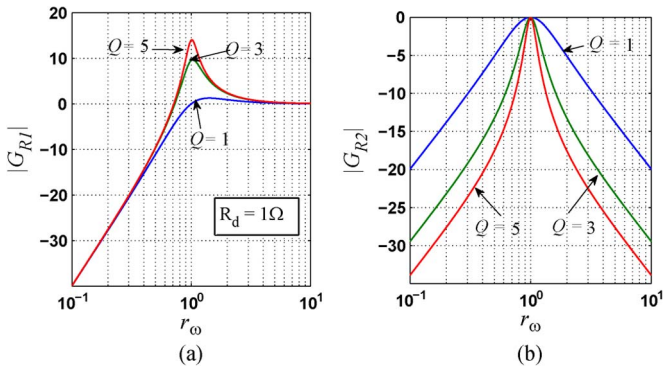

Fig. 5. (a) $|G_{R1}(j\omega)|$(dB) for $R_d = 1\ \Omega$. (b) $|G_{R2}(j\omega)|$(dB).

C. Selection of Damping Resistor R_d

Since an external damping resistor R_d is indispensable in the input filter, minimum operating efficiency requires a limit on the maximum loss associated with R_d. Denoting the current through R_d as i_{R_d}, the corresponding design criterion is

Spec.5 $3R_d \sum_{n=1}^{\infty} [i_{R_d}(jn\omega_b)]^2 < 1\%$ of rated load.

i_{R_d} can be expressed as

$$i_{R_d}(s) = G_{R1}(s) v_s(s) + G_{R2}(s) i_{in}(s) \tag{6}$$

where

$$\left| G_{R1}(s) \triangleq \frac{i_{R_d}(s)}{v_s(s)} \right|_{s=j\omega} = \frac{1}{R_d} \cdot \frac{r_\omega^2}{\sqrt{\left[(1-r_\omega^2)^2 + \frac{r_\omega^2}{Q^2}\right]}}$$

$$\left| G_{R2}(s) \triangleq \frac{i_{R_d}(s)}{i_{in}(s)} \right|_{s=j\omega} = \frac{1}{Q} \cdot \frac{r_\omega}{\sqrt{\left[(1-r_\omega^2)^2 + \frac{r_\omega^2}{Q^2}\right]}}. \tag{7}$$

The frequency responses of these transfer functions are plotted in Fig. 5(a) and (b), respectively, for $R_d = 1\ \Omega$. High Q is particularly desirable in $|G_{R2}|$ as it implies lesser ripple content in i_{R_d} and, therefore, a lower loss. However, high Q in $|G_{R1}|$ implies a higher loss due to increased low-order harmonics in i_{R_d}. The plots reveal a response similar to that encountered with the normalized form of $|G_{fv}|$ in Fig. 4. As can be expected from this similarity, $Q^{(1)}$ chosen in Section II-A is found to give an even balance between both the conflicting aspects. Therefore, $Q^{(1)}$ is finalized for filter design.

The power loss associated with R_d is

$$P_R = 3R_d \left\{ \sum_n \left(|G_{R1}(jn\omega_b)|^2 V_{s,n}^2 + |G_{R2}(jn\omega_b)|^2 I_{in,n}^2 \right) \right\} \tag{8}$$

where $V_{s,n}$ and $I_{in,n}$ are the values corresponding to the nth harmonic order. The calculation of P_R using (8) requires the

TABLE IV
HARMONICS IN i_{in} FROM SIMULATION AT $m = 1$

193^{rd}	195^{th}	199^{th}	201^{st}	205^{th}	207^{th}
10.66%	25.31%	32.58%	11.88%	5.84%	2.58%

TABLE V
$L_{f,\min}$ AND $C_{f,\min}$ FROM REGULATION, REACTIVE LOADING, AND FIXED f_c

F_1	F_2/I_o^2	$L^{(1)}_{f,\min}$	$C^{(1)}_{f,\min}$
3.44	0.001167	1.15 mH	9.7 μF

$R^{(1)}_{d,\min}$	$R^{(1)}_{d,\max}$	$R^{(2)}_{d,\min}$	$R^{(2)}_{d,\max}$
17.5 mΩ	534.16 Ω	21.7 Ω	45 Ω

prior selection of f_c for evaluating the gains $|G_{R1}(jn\omega_b)|$ and $|G_{R2}(jn\omega_b)|$. For the experimental model, f_c is selected from the allowable range provided in Table II as

$$f_c^{(1)} = 1 \text{ kHz}. \tag{9}$$

1) R_d From Loss Limit: With the harmonic analysis of MC being outside the scope of this paper, the expression for losses is derived assuming sinusoidal i_o. The harmonic components in i_{in} obtained from simulation are listed in Table IV. Using $f_c^{(1)}$ and $Q^{(1)}$, the gains defined in (7) are evaluated. Subsequently, using these gains and the harmonics listed in Table IV in (8), for the nominal parameters in Table I, P_R is obtained in the following form:

$$P_R = \frac{F_1}{R_d} + F_2 R_d \tag{10}$$

where F_1 and F_2 are functions of $|G_{R1}(j\omega_b)|$, V_s, $|G_{R2}(jn\omega_b)|$, and $I_{in,n}$. These are tabulated in Table V. Thereafter, applying the numerical limits of **Spec.5**, (10) yields two roots which define an allowable range of R_d as follows:

$$R^{(1)}_{d,\min} \le R_d \le R^{(1)}_{d,\max}. \tag{11}$$

This choice of R_d definitely satisfies **Spec.1**, **Spec.2**, and **Spec.5**. However, it is not apparent whether any value of R_d in this band and the corresponding L_f and C_f evaluated using (3) would also satisfy **Spec.3** and **Spec.4**.

2) R_d From Voltage Regulation and Reactive Loading Limits: The upper bounds $C^{(1)}_{f,\max}$ and $L^{(1)}_{f,\max}$ imply corresponding lower bounds $L^{(1)}_{f,\min}$ and $C^{(1)}_{f,\min}$ for the selected f_c in (9). These are listed in Table V.

Using (3), since

$$R_d = \left(2\pi f_c^{(1)} Q^{(1)}\right) L_f. \tag{12}$$

$L^{(1)}_{f,\max}$ and $L^{(1)}_{f,\min}$ define a new set of bounds on R_d

$$R^{(2)}_{d,\min} \le R_d \le R^{(2)}_{d,\max}. \tag{13}$$

Hence, the allowable values of R_d will be those where the two ranges obtained from (11) and (13) intersect. In the absence of intersection, the numerical limits of all or some of **Spec.3**, **Spec.4**, and **Spec.5** must be made less stringent. For the experimental model, these ranges of R_d are listed in Table V. Since these ranges intersect, (13) defines the final set for selecting R_d.

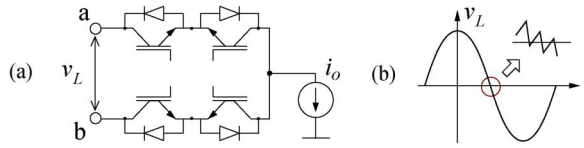

Fig. 6. Commutation between input phases a and b.

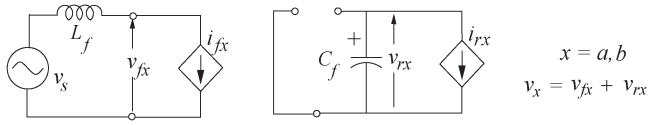

Fig. 7. Input current and voltage.

D. Lower Limit of C_f: Maximum Ripple in Input Line–Line Voltage and Consequent Problem in Commutation

Fig. 6(a) shows two input phases a and b, which are alternatively switched to an output phase. Commutation based on the polarity of input line–line voltage ($v_L = v_{ab}$) is difficult at its ZC, due to the presence of switching ripple component v_{rL}, as shown in Fig. 6(b). In the following analysis, it is assumed that only fundamental and switching frequency components are present in the input current and filter capacitor voltages. v_L can be represented as

$$v_L = \underbrace{(v_{fa} - v_{fb})}_{v_{fL}} + \underbrace{(v_{ra} - v_{rb})}_{v_{rL}} \tag{14}$$

where the subscripts f and r have been used to denote the fundamental and ripple components, respectively. Fig. 7 shows the input current and filter capacitors. It is assumed that the ripple component i_{rx} completely circulates through the filter capacitor while i_{fx} flows through the source. Hence,

$$v_{rL} = v_{ra} - v_{rb} = -\frac{1}{C_f}\int (i_{ra} - i_{rb})\, dt. \tag{15}$$

i_{rx} is synthesized from the output current envelope, which is a direct function of the load. Therefore, an arbitrarily small C_f, chosen to reduce reactive loading at low loads, leads to a corresponding high v_{rL} at high loads. With the usual delays involved, the phase error in the measurement of v_{rL} is significantly more than that of v_{fL}. The consequent inaccuracy in detecting the polarity of v_{rL} around the ZC of v_{fL} increases the chance of a commutation failure. Therefore, the estimation of maximum v_{rL} and analyzing its effect on commutation form a prerequisite for determining the lower limit of C_f. Deriving a closed-form expression for maximum v_{rL} is described in Appendix A. Incorrectly sensing the polarity of v_{fL} may lead to erroneous commutation in the following manner.

Fig. 8 shows the plot of ripple current and v_{rL} around the instant when $\hat{v}_{rL}$ reaches $\hat{v}_{rL,\max}$. This occurs during commutation from phase a to phase b. The capacitor voltages

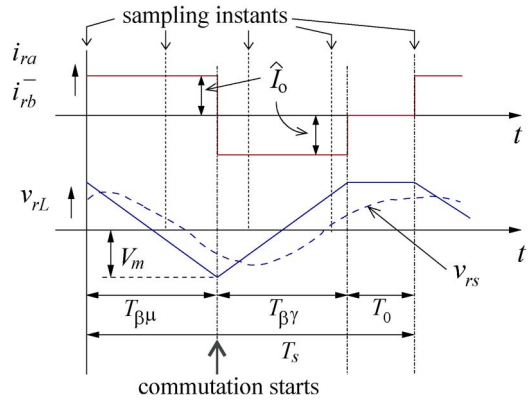

Fig. 8. Error in measuring v_{rL} around its maximum value.

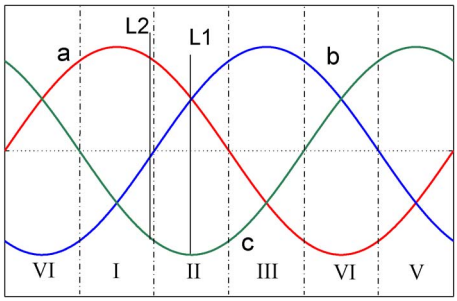

Fig. 9. Instantaneous positions of i_{fa}, i_{fb}, v_{fa}, and v_{fb} at beginning of commutation from phase a to phase b.

are sampled at frequency $4f_s$. v_{rs} is the corresponding sensed ripple voltage available for sampling. Noise filtering in voltage measurement and the antialiasing filters invariably cause delays in the sensed signal. The presented plot of v_{rs} is derived using a first-order low-pass approximation of the measurement circuit and filter.

At the sampling instant just before commutation, v_{rs} is positive, and v_{rL} is negative with a magnitude V_m. Using (43)

$$V_m \approx \frac{\sqrt{3}}{8C_f}\hat{I}_o T_s. \tag{16}$$

At the instant when commutation is about to begin, $\bar{\mathbf{I}}_{\mathbf{in}}$ is very close to the middle of sector II of the input current hexagon shown in Fig. 17(a) in Appendix A. The 3 Ph waveforms shown in Fig. 9 have been used to distinguish between the position of different variables on the basis of their instantaneous phases, at the start of commutation. The intersection of the vertical line L1 with the three waveforms therefore indicates the position of i_{fa}, i_{fb}, and i_{fc}, respectively, at the start of commutation. At the same instant, the relative position of the fundamental components of input voltages depends on the IDF. Let the intersection of the line L2 with the waveforms indicate the positions of v_{fa}, v_{fb}, and v_{fc}, respectively. Therefore, the input currents lead the voltages, a situation which can arise in applications requiring input reactive power control [23], [24]. From Fig. 9, since v_{fa} and v_{fb} have clearly distinguished instantaneous values, the commutation between these two phases is to be interpreted as an "uncritical" one [22]. For an uncritical commutation, regular two- or four-step commutation methods are suggested [21],

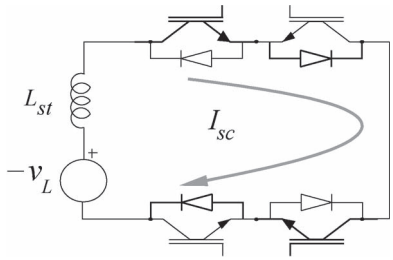

Fig. 10. Path of short circuit current.

[22]. The instantaneous values of the fundamental component of the voltages of phases a and b are

$$v_{fa} \approx \frac{\sqrt{3}}{2}\hat{V}_{cf},\ v_{fb} \approx 0 \quad \Rightarrow_{fL} = \frac{\sqrt{3}}{2}\hat{V}_{cf}. \tag{17}$$

Since v_{fL} has a substantially high magnitude and delay in sensing it is much lesser than the ripple component, it is justified to assume that its polarity is correctly detected. Also, since v_{rs} is positive, polarity of v_L is interpreted to be positive.

Now, using (16) and (17)

$$v_L = \frac{\sqrt{3}}{2}\left(\hat{V}_{cf} - \frac{\hat{I}_o T_s}{4C_f}\right). \tag{18}$$

Therefore, v_L becomes negative if

$$\hat{V}_{cf} < \frac{\hat{I}_o T_s}{4C_f} \quad \Rightarrow \quad C^{(2)}_{f,\min} = \frac{\hat{I}_o T_s}{4\hat{V}_{cf}} \approx \frac{I_o T_s}{4V_s}. \tag{19}$$

Fig. 10 shows the condition that will arise in this situation. Short circuit current i_{sc} flows over an interval T_{sc}, which comprises two turn-on and turnoff times of the insulated gate bipolar transistor (IGBT). L_{st} in Fig. 10 represents the stray inductance of the circuit. Let v_D be the total forward drop of the two IGBTs and diodes. Thereby, by denoting $\hat{I}_D$ as the maximum current rating of the devices, the criterion for the safety of the devices is obtained as

$$I_{sc,\max} = \frac{1}{L_{st}}\int_0^{T_{sc}} (-v_L - v_D)\, dt \le \hat{I}_D. \tag{20}$$

Using (18) in (20), a lower limit of C_f is obtained as

$$C^{(3)}_{f,\min} = \frac{1}{4}\hat{I}_o T_s \left\{\hat{V}_{cf} + 1.15\left(v_D + \frac{L_{st}\hat{I}_D}{T_{sc}}\right)\right\}^{-1}. \tag{21}$$

$C^{(3)}_{f,\min}$ is, of course, hardware specific. $C^{(2)}_{f,\min}$ may be used as a preliminary check before proceeding with the hardware details. If the converter is operated at unity IDF, then, for maximum v_{rL} to occur at the instant of commutation, v_{fL} has to be zero. The line voltage magnitude v_L is then equal to V_m defined in (16). Substituting $-v_L$ accordingly in (20) yields another lower limit of C_f as

$$C^{(4)}_{f,\min} = \frac{\sqrt{3}}{8}\hat{I}_o T_s \left\{v_D + \frac{L_{st}\hat{I}_D}{T_{sc}}\right\}^{-1}. \tag{22}$$

TABLE VI
$C_{f,\min}$ FOR RELIABLE VOLTAGE COMMUTATION

$C^{(2)}_{f,\min}$	$C^{(3)}_{f,\min}$	$C^{(4)}_{f,\min}$	T_{sc}	L_{st}	$\hat{I}_D$	v_D
1.04 μF	0.97 μF	14.9 μF	2 μs	260 nH	80 A	10.1 V

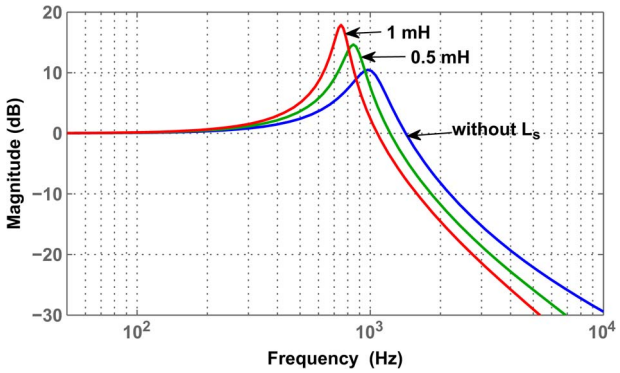

Fig. 11. Magnitude plot of $G_{fv}(s)$ for L_s of 0.5 and 1 mH.

$C^{(4)}_{f,\min}$ would be higher than both $C^{(2)}_{f,\min}$ and $C^{(3)}_{f,\min}$. For unity IDF, the commutation through a third phase [21] would allow using a smaller capacitor. However, operating with a value higher than $C^{(4)}_{f,\min}$ will ensure safe commutation for any operating condition. Moreover, this is ensured irrespective of any particular commutation method and is not dependent on the accurate ZC detection of ripple voltage.

Table VI shows $C^{(2)}_{f,\min}$, $C^{(3)}_{f,\min}$, and $C^{(4)}_{f,\min}$, calculated using tabulated device ratings and measured L_{st}.

E. Effect of L_s

With the inclusion of L_s, $G_fv(s)$ is obtained as

$$G_{fv}(s) = \frac{s\frac{L_f}{R_d}+1}{s^3\frac{L_sL_fC_f}{R_d}+s^2C_f(L_s+L_f)+s\frac{L_f}{R_d}+1}. \quad (23)$$

Under the assumption of underdamped second-order filter

$$G_{fv}(s) \approx \frac{s\frac{L_f}{R_d}+1}{\left(s\frac{L_f}{R_d}\frac{n}{n+1}+1\right)\left(\frac{s^2}{\omega_c^2}+\frac{s}{\omega_cQ_c}+1\right)} \quad (24)$$

where

$$\omega_c \approx \frac{1}{\sqrt{(n+1)L_fC_f}}, Q \approx R_d\left(\sqrt{\frac{C_f}{L_f}}\right)(1+n)^{1.5}, n = \frac{L_s}{L_f}. \quad (25)$$

Fig. 11 shows the gain plot for varying L_s. Input filter parameters are used from Table VIII. Therefore, as L_s increases, ω_c falls while Q increases. Thus, the gain to lower harmonics is bound to increase. However, the losses are going to decrease as f_s components of i_{in} now see a higher impedance parallel to C_f. Hence, knowledge of L_s is necessary before finalizing on the input filter parameters. If n defined is (25) is less than 0.5, then ω_c does not get significantly affected, and neither does the filter performance. However, a high n, apart from deteriorating the harmonic performance, further complicates the controller design as discussed subsequently.

F. Design Modifications for a Nonminimum Phase Plant

The dynamic model of 3 Ph MC in the dq reference frame has been analyzed in [18] where a condition for avoiding right half zeros (RHZs) in the plant transfer function matrix has been described. For the per-phase system depicted in Fig. 2, the input filter output impedance Z_{so} is defined as

$$Z_{so}(s) = -\frac{v_{cf}(s)}{i_{in}(s)}\bigg|_{v_s(s)=0}. \quad (26)$$

This scalar transfer function is transformed to a transfer matrix $\mathbf{Z_{so}}(s)$ in a synchronous dq reference frame as

$$\mathbf{Z_{so}}(s) = \begin{bmatrix} Z_{so11}(s) & Z_{so12}(s) \\ -Z_{so12}(s) & Z_{so11}(s) \end{bmatrix}. \quad (27)$$

For avoiding RHZs, it is necessary that

$$|Z_{so11}(j\omega_M)| < \frac{3}{2}\frac{\hat{V}_{cf}^2\cos^2\varphi_i}{P_{in}}. \quad (28)$$

$Z_{so11}(j\omega)$ has multiple phase crossovers, and ω_M is that phase crossover frequency where $|Z_{so11}(j\omega)|$ is maximum. P_{in} is the power at the input terminals of MC, and $\cos\varphi_i$ is the IDF.

Importantly, the condition defined in (28) is not confined to any specific modeling approach. The power stage of MC, along with input filters in the small signal/linearized model, is responsible for RHZs. From (28), input filter parameters are one of the factors deciding the emergence of RHZs. The violation of (28) causes four RHZs to emerge in the system, which severely complicates the controller design, particularly if the bandwidth (BW) requirement is high. Then, either the dynamic specifications have to be relaxed or the input filter has to be designed such that (28) is not violated. With reference to (28) and [18]

$$|Z_{so11}(j\omega_M)| \approx \|Z_{so11}(j\omega)\|_\infty \le \|Z_{so}(j\omega)\|_\infty. \quad (29)$$

Assuming underdamped second-order filter and ideal passive elements

$$\|Z_{so}(j\omega)\|_\infty = |Z_{so}(j\omega_c)| \approx R_d\left(1+\frac{L_s}{L_f}\right)^2. \quad (30)$$

So as L_s increases, chances of the plant migrating from minimum to nonminimum phase also increase. Under these circumstances a lower R_d or higher L_f can be chosen to ensure that (28) is satisfied and the plant remains minimum phase. Either of these options degrade the steady-state performance in different ways. Higher voltage drop across L_f lowers the maximum output voltage that can be obtained. A lower R_d on the other hand increases losses. So, for a weak grid, a tradeoff is necessary between the dynamic performance and either filter losses or full-load regulation.

The inclusion of the internal resistances (r_i) of passives at ω_M results in higher damping owing to the skin effect and, hence, lower $|Z_{so}(j\omega_M)|$ than what is represented by (30).

TABLE VII
BOUNDARY VALUES FOR PARAMETERS OF OUTPUT FILTER PARAMETERS

$f_{co,\,\max}$	$f_{co,\,\min}$	$L_{o,\,\max}$	$C_{o,\,\max}$	$L_{o,\,\min}$
2.2 kHz	777 Hz	2 mH	26.5 μF	1.6 mH

Therefore, to avoid a conservative design, using the measured value of r_i or a good design estimate of it, to calculate $|Z_{so}(j\omega_M)|$, is necessary.

III. OUTPUT FILTER

The criteria defined in **Spec.1** to **Spec.4** are also followed for output filter design. The procedure, being very similar to the earlier exercise, is therefore briefly discussed.

Denoting the resonant frequency of the output filter shown in Fig. 2 as ω_{co}, the forward gain is obtained as

$$G_{vof}(s) = \frac{v_{co}(s)}{v_{on}(s)} = \frac{1}{(s/\omega_{co})^2 + (s/Q_o\omega_{co}) + 1} \tag{31}$$

where $Q_o = R_o\sqrt{(C_o/L_o)}$.

Since v_{on} can be controlled, a virtual damping resistor can be introduced through control to emulate R_o. The selection of the values of Q_o, $f_{co,\max}$, $f_{co,\min}$, $C_{o,\max}$, and $L_{o,\max}$ is carried out in the same manner followed during the input filter design.

For the input filter, the output current decides the ripple current rating of the filter capacitors. At the output side, however, the proper sizing of L_o allows an additional freedom of using capacitors with a lower ripple current rating. This is clarified using the expression of output admittance, which is obtained as

$$Y_{mo}(s) = \frac{i_o(s)}{v_{on}(s)} = \frac{1}{R_o}\frac{1 + s\,(Q_o/\omega_{co})}{(s/\omega_{co})^2 + (s/Q_o\omega_{co}) + 1}. \tag{32}$$

Thus, for Q_o greater than 1

$$|Y_{mo}(j\omega_s)| \approx \frac{1}{\omega_s L_o}. \tag{33}$$

In SVM [27], at any instant, three output phases are connected to any two input phases. Hence, from Fig. 1, for output phase A

$$\hat{v}_{on} = \frac{2}{3}\,\hat{v}_{ab} = 1.63V_s. \tag{34}$$

The resulting peak switching ripple, found using (33) and (34), must be lower than the peak ripple current rating $(\hat{I}_{r,\mathrm{rated}})$ of C_o. Hence

Spec.6 $L_{o,\min} = (1.63V_{s,\mathrm{rated}})/(\omega_s\hat{I}_{r,\mathrm{rated}})$.

Table VII lists the described limits for output filter parameters calculated using the nominal values in Table I.

IV. SELECTION OF PARAMETER VALUES

The design guidelines from the previous sections are summarized here to facilitate a step-by-step design process. With the nominal power, fundamental and switching frequency, and percentages of different harmonics in the source voltage as design inputs, parameters are selected in the following manner.

Step 1) Selection of quality factor $Q\,(=Q^{(1)})$ from the normalized form of the input filter forward gain conforming to **Spec.1** and **Spec.2**. As discussed in Section II-C, $Q^{(1)}$ is the optimum value and, therefore, the chosen value for the design.

Step 2) Selection of f_c from the allowable range obtained using the forward gain plot, $Q^{(1)}$, **Spec.1**, and **Spec.2**

Step 3) Computation of the upper limits $L^{(1)}_{f,\max}$ and $C^{(1)}_{f,\max}$ by using **Spec.3** and **Spec.4**, respectively. Subsequently, these values, along with the selected f_c, are used to compute the corresponding $C^{(1)}_{f,\min}$ and $L^{(1)}_{f,\min}$, respectively.

Step 4) Computation of the first allowable set of R_d conforming to **Spec.5** and the second set that conforms to **Spec.3** and **Spec.4** as discussed in Section II-C2. The intersection of these two sets forms the final allowable range of R_d. If they do not intersect, then either one or both of the sets has to be expanded by relaxing the corresponding **Spec.** to obtain a region of overlap. The first set can be expanded at the expense of allowing higher losses while relaxing the upper and lower bounds of the second set implies poor regulation and higher reactive loading, respectively, than the imposed limits. In this regard, the steady-state requirements for the target application help in deciding which **Spec.** should be relaxed. This implies starting again from the step related to the redefined **Spec.**

Step 5) Computation of $C^{(4)}_{f,\min}$ for reliable voltage commutation using (19). This has to be treated as the absolute lower limit for C_f if this value is greater than $C^{(1)}_{f,\min}$.

Step 6) Selection of L_f from the interval $[L^{(1)}_{f,\min}, L^{(1)}_{f,\max}]$. Choosing C_f from the interval $[C^{(4)}_{f,\min}, L^{(1)}_{f,\max}]$ or from $[C^{(1)}_{f,\min}, L^{(1)}_{f,\max}]$ as discussed in *Step 5*. Also, finalizing the value of R_d from the range obtained from *Step 4*.

Step 7) Detecting whether the chosen input filter parameters result in a nonminimum phase plant. If it does, then the feasibility of obtaining a stable closed-loop system in compliance to the dynamic specifications has to be investigated. If a minimum phase plant is desired, then either the full-load regulation (**Spec.3**) or filter loss (**Spec.5**) has to be relaxed, and parameters have to be redesigned repeating *Steps 3* to *7*.

Step 8) Selecting Q_o, f_{co}, $C_{o,\max}$, and $L_{o,\max}$ following the same steps as their input-side counterparts.

Step 9) Selection of $L_{o,\min}$ conforming to **Spec.6**. Subsequently choosing the values of L_o and C_o, thereby completing the design process.

The filter parameters are selected following the described steps and using the boundary values listed in Tables II, III, V–VII. The parameter values chosen in this paper are shown in Table VIII, which also lists the specific volume (cm^3/kW) and weight (kg/kW) of the inductors and capacitors. Experimental results are discussed next.

TABLE VIII
INPUT AND OUTPUT FILTER PARAMETERS

Parameter	Value	Sp. volume (cm^3/kW)	Sp. weight (Kg/kW)
C_f	20 μF	19.16	0.0316
L_f	1.26 mH	101	0.38
R_d	25 Ω		
C_o	20 μF	0.93	0.00125
L_o	2 mH	91	0.38

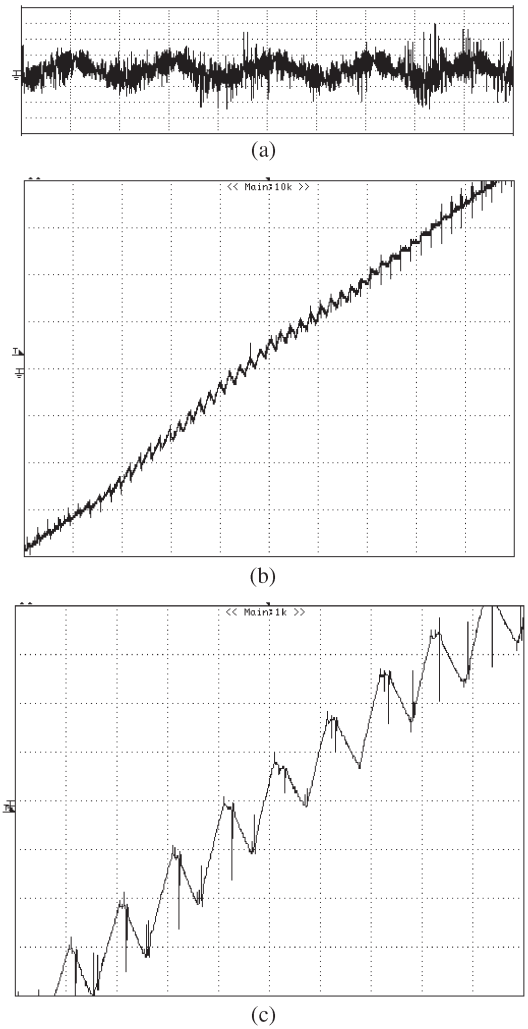

Fig. 12. (a) Voltage across R_d: 10 V/div; time: 10 ms/div. (b) v_L: 100 V/div; time: 500 μs/div. (c) v_L: 20 V/div; time: 100 μs/div.

V. RESULTS AND DISCUSSION

Experimental validation was carried out on a 6-kVA MC prototype with IGBT-based four-quadrant switches with the filter parameters listed in Table VIII. The entire control logic was realized on an FPGA platform using ALTERA EP1C12Q240C8 with a sampling frequency of 20 kHz. For commutation, the measured value of v_{cf} was sampled at 40 kHz. A regular four-step commutation strategy, as reviewed in [22], was implemented.

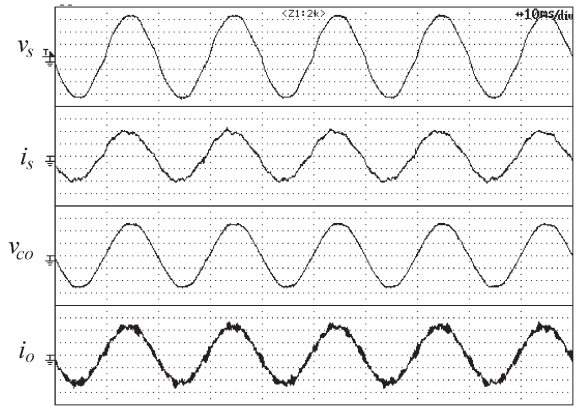

Fig. 13. Open-loop experimental results. v_s: 100 V/div, i_s: 5 A/div, v_{co}: 100 V/div, and i_o: 5 A/div. Time: 10 ms/div.

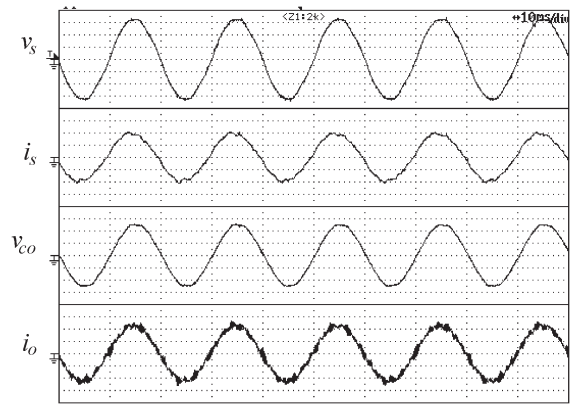

Fig. 14. Open-loop results with an L_s of 1 mH. v_s: 100 V/div, i_s: 5 A/div, v_{co}: 100 V/div, and i_o: 5 A/div. Time: 10 ms/div.

TABLE IX
MEASURED VALUES

Input power	C_f (phase - a)	C_f (phase - b)	$\hat{v}_{rL,\max}$	IDF
4.9 kW	17.9μF	14.5μF	31 V	0.982

A. Open-Loop Experimental Results

MC was operated with $m = 1$ and unity IDF with $i_o = 8.2$ A (fundamental). Figs. 12–14 show the waveforms. Experimentally measured data are listed in Table IX.

The voltage waveform across the damping resistor R_d is shown in Fig. 12(a). From the experimental data, its rms value was calculated, resulting in a power loss of 2 W which is much lower than 1% of the input power listed in Table IX. The analysis in Section II-C1 using fundamental v_s and i_o suggests a value (2.1 W) very close to the experimentally obtained value.

Referring to Appendix A and particularly (40), operating at unity IDF implies that $\hat{v}_{rL,\max}$ is expected almost at the ZC of input line–line voltage v_L. Fig. 12(b) shows v_L around ZC over 5 ms, and its zoomed view is presented in Fig. 12(c). It is evident that maximum ripple occurs around the ZC zone as expected. In the experimental setup, the measurement of the input filter capacitors with the RCL meter at 10 kHz revealed the values shown in Table IX. The values of C_f from Table IX are used to calculate v_{ra} and v_{rb} at the maximum ripple condition as detailed in Section II-D. Subsequently,

TABLE X
HARMONICS IN ONE PHASE OF v_s, i_s, AND v_{co}

Harmonic order	v_s	i_s	v_{co}
3rd	1.1%	2.65%	0.3%
5th	2.64%	2.16%	1%
7th	2%	4%	1%
9th	0.54%	2%	0.6%
11th	0.23%	0.2%	0.2%
THD	3.6%	5.9%	1.67%

TABLE XI
HARMONICS v_s, i_s, AND v_{co} WITH $L_s = 1$ mH

Harmonic order	v_s	i_s	v_{co}
3^{rd}	1.8%	3.2%	0.6%
5^{th}	1.9%	1%	1%
7^{th}	1%	2.2%	0.9%
9^{th}	0.9%	2.6%	0.6%
11^{th}	0.1%	0.65%	0.15%
15^{th}	0.1	1%	0.05
17^{th}	0.1	0.9%	0.1
THD	3.1%	5.4%	1.8%

the $\hat{v}_{rL,\max}$ magnitude is found to be 30.8 V. Numerically extracting (filtering) the switching ripple component from the experimental data reveals a maximum ripple listed in Table IX. Thus, a very close agreement is observed between the analytical and experimental observations. Experimental data also revealed an IDF of 0.982 as listed in Table IX.

Table X lists the harmonic components in phase a, where the supply voltage v_s contains significant low-order harmonics, which, in turn, get transmitted to v_{co}. Since i_s is a function of both v_s and i_o, it has a higher harmonic content. From the harmonics of v_{co} listed, it is evident that the gain criterion adopted in Sections II and III is effective in the minimal transmission of low-order harmonics from v_s to v_{co}. The switching frequency ripple in i_s was found to be slightly less than 1% of its fundamental component.

1) Performance With L_s Included: Fig. 14 shows the steady-state waveforms, at the same power level, with an externally added L_s of 1 mH. With this inclusion, using (25), ω_c reduces from 1 kHz to 746 Hz, and Q increases from 3.1 to 7.6. The harmonic contents of v_s, i_s, and v_{co} are given in Table XI. Owing to the proximity of input and output corner frequencies (746 and 796 Hz), an increase in the harmonic content of i_s close to these frequencies is observed. At the instant that this experiment was performed, the total harmonic distortion (THD) of v_s was slightly better than the previous situation. However, due to the proximity of the input and output filter corners, the harmonics of i_s around the output corner have increased, which marginally increased the THD of v_{co}. The measured value of IDF was found to be 0.984.

Fig. 15 shows the closed-loop dynamic response of one of the phases of output voltage. The error voltage in v_{cod}, m, and v_{co} are presented in the situation where, initially, a step command of 140 V is introduced and, subsequently, the reference command is reset to zero.

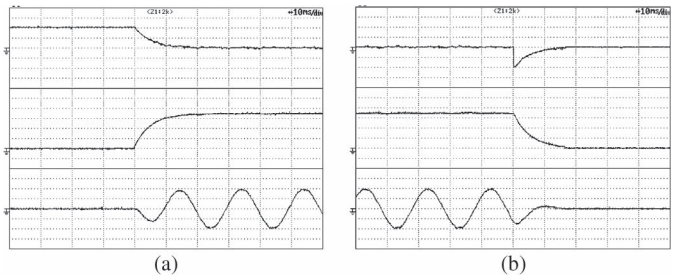

Fig. 15. Dynamic performance. (a) v_{co} reference command of 140 V. (b) v_{co} reference reset to 0 V. Upper trace: Error voltage in d-axis (116 V/div). Second trace: m (0.2/div). Bottom trace: v_{co} (100 V/div). Time: 10 ms/div.

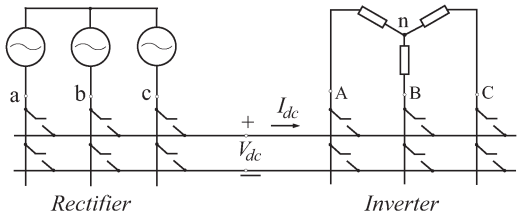

Fig. 16. Decoupled rectifier-inverter construct.

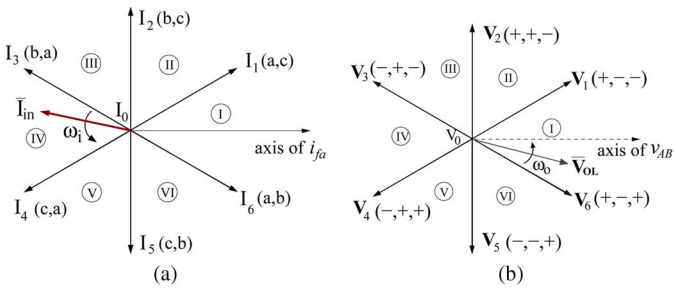

Fig. 17. (a) Input current hexagon. (b) Output voltage hexagon.

VI. CONCLUSION

An exhaustive filter design approach of 3 Ph direct MC (DMC) is presented which, in addition to meeting general requirements of a ripple filter, also addresses the design constraints imposed by dynamic specifications and commutation requirements. Ripple filter design aspects like attenuation and regulation and also MC-specific issues like the damping resistors at the input filter have been addressed. The detailed analytical derivation of the damping resistor losses and input voltage ripple is provided, and experimental results are presented to establish the validity of the analytical conclusions.

The minimum input filter capacitor required for reliable VBC has been derived based on the maximum error in ripple voltage sensing. The effect of the grid inductance has been discussed where the possibility of a compromise between the filter and controller designs has been highlighted. The output ripple filter has also been discussed, and experimental waveforms are provided to demonstrate the close agreement of the filter performance with the input specifications. The necessary tradeoffs in filter design, which may be imposed by dynamic requirements, originate from the basic power stage of a 3 Ph DMC. Therefore, the observations are equally applicable to single-phase MCs or indirect MCs which are derived from the basic MC topology.

TABLE XII
INPUT–OUTPUT CONNECTIONS IN MC FOR $\bar{I}_{in}$ IN SECTOR 2 AND $\bar{V}_{OL}$ IN SECTOR 3

		Decoupled construct					3 Ph MC					
Stationary Vectors	ON period	A	B	C	+	-	A	B	C	i_a	i_b	i_c
$\mathbf{V_2I_1}$	$d_\alpha d_\mu T_S = m\sin(60^\circ - \theta_{SV})\sin(60^\circ - \theta_{SI})T_S \rightarrow T_{\alpha\mu}$	+	+	-	a	c	a	a	c	$-i_C$	0	i_C
$\mathbf{V_2I_2}$	$d_\alpha d_\gamma T_S = m\sin(60^\circ - \theta_{SV})\sin(\theta_{SI})T_S \rightarrow T_{\alpha\gamma}$	+	+	-	b	c	b	b	c	0	$-i_C$	i_C
$\mathbf{V_3I_1}$	$d_\beta d_\mu T_S = m\sin(\theta_{SV})\sin(60^\circ - \theta_{SI})T_S \rightarrow T_{\beta\mu}$	-	+	-	a	c	c	a	c	i_B	0	$-i_B$
$\mathbf{V_3I_2}$	$d_\beta d_\gamma T_S = m\sin(\theta_{SV})\sin(\theta_{SI})T_S \rightarrow T_{\beta\gamma}$	-	+	-	b	c	c	b	c	0	i_B	$-i_B$

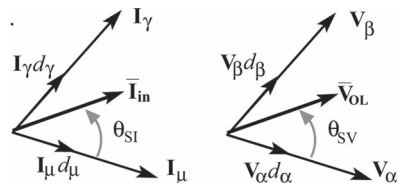

Fig. 18. θ_{SI} and θ_{SV}.

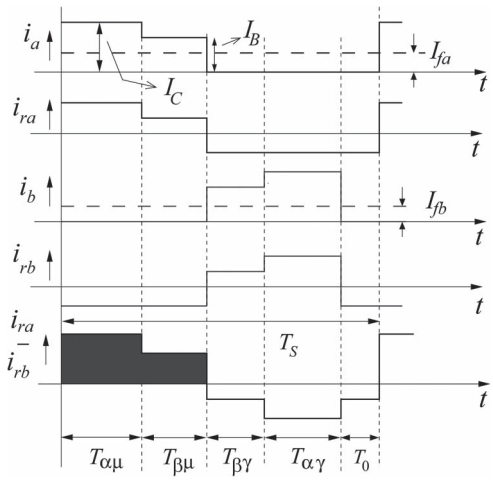

Fig. 19. Fundamental (I_{fa}, I_{fb}) and switching frequency (i_{ra}, i_{rb}) components of input currents (i_a, i_b).

APPENDIX A
MAXIMUM v_{rL} BETWEEN PHASES A AND B

Fig. 16 shows the decoupled rectifier-inverter construct of MC. The input current and output voltage stationary vectors for realizing SVM [27] are shown in Fig. 17(a) and (b). $\mathbf{I_1}$ (a, c) implies that input phases "a" and "c" are connected to the positive and negative rails of the fictitious dc link, respectively. Also, $\mathbf{V}_1(+,-,-)$ indicates that the output phase A is connected to the positive rail and both B and C are connected to the negative rail.

Considering an instant when $\bar{\mathbf{I}}_{\mathbf{in}}$ lies in sector II, requiring commutation between input phases a and b, and $\bar{\mathbf{V}}_{\mathbf{OL}}$ is in sector III, the relevant switching vector combinations and input–output connections are listed in Table III. Fig. 18 shows the rotating space vectors of each hexagon and the two bordering stationary vectors. θ_{SI} and θ_{SV} are the angles between the rotating and the trailing stationary vectors. The expression for duty cycles [27] is also indicated in Table XII. Fig. 19 shows the fundamental and switching frequency components of the input currents. The fundamental components of both input and output currents are assumed to be constant over a switching period T_s. The input currents are denoted as I_{fa} and I_{fb}, respectively. Output currents over the same period are represented as I_C and I_B. From Table XII and Figs. 9 and 19, I_{fa} and I_{fb} can be expressed as

$$I_{fa} = (I_C d_\alpha d_\mu + I_B d_\beta d_\mu) = mI_P \sin(60^\circ - \theta_{SI})$$
$$I_{fb} = (I_C d_\beta d_\gamma + I_B d_\alpha d_\gamma) = mI_P \sin\theta_{SI} \quad (35)$$

where

$$I_P = I_C \sin(60^\circ - \theta_{SV}) + I_B \sin\theta_{SV}. \quad (36)$$

From (15), the peak–peak magnitude of v_{rL}, $\hat{v}_{rL}$, is maximum when area A_P, shown shaded in Fig. 19, is maximum. A_P is evaluated as

$$A_P = \{(I_C - I_{fa} + I_{fb})d_\alpha d_\mu + (I_B - I_{fa} + I_{fb})d_\beta d_\mu\}T_s. \quad (37)$$

Substituting (35) in (37), A_P gets modified as

$$A_P = mI_P T_s \sin(60^\circ - \theta_{SI})k\,(\theta_{SI}, \theta_{SV}) \quad (38)$$

where

$$k\,(\theta_{SI}, \theta_{SV}) = \left\{1 + \sqrt{3}m\sin(\theta_{SI} - 30^\circ)\cos(\theta_{SV} - 30^\circ)\right\}. \quad (39)$$

Since θ_{SI} and θ_{SV} each vary in the closed interval $[0^\circ, 60^\circ]$ and m varies in [0, 1], it is derived that A_P reaches its maximum for

$$\theta_{SI} = 28^\circ, \theta_{SV} = 60^\circ \;\&\; m = 1. \quad (40)$$

Therefore, $\hat{v}_{rL}$ is maximum at an instant when $i_{fa} \approx i_{fb}$. Using (40), (38), and (39) in (15), maximum $\hat{v}_{rL}$ is

$$\hat{v}_{rL,\max} \approx (0.5/C_f)\hat{I}_{in}T_s. \quad (41)$$

The amplitude of the input current $\hat{I}_{in}$ in MC [27] is

$$\hat{I}_{in} = mI_P = (\sqrt{3}/2)m\hat{I}_o\cos(\varphi_{oL}) \quad (42)$$

where φ_{oL} is the load impedance angle. From (42), the maximum possible $\hat{I}_{in}$ is $(\sqrt{3}/2)\hat{I}_o$. Substituting this in (41)

$$\hat{v}_{rL,\max} \approx \frac{\sqrt{3}}{4C_f}\hat{I}_0 T_s. \quad (43)$$

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