

RGPV (DIPLOMA WING) BHOPAL			OBE CURRICULUM FOR THE COURSE			FORMAT- 3		Sheet No. 1/3	
Branch	Computer Science and Engineering					Semester		Third	
Course Code		C04	Course Name	COMPUTER ARCHITECTURE					
							Teach Hrs		Marks
Course Outcome 1		Interpret various type of micro-operations and instructions.					30		38 (10+28)
Learning Outcome 1		Understand Register transfer language and micro-operations.					10		14
Contents		<ul style="list-style-type: none">• Register transfer language, Register transfer, Bus and Memory transfer• Micro-operations,• Types of micro-operations:• Arithmetical (Binary Adder, Binary adder-subtractor, Binary Incrementor),• Logical (AND, OR, X-OR, Complement) and its Hardware implementation.• Shift (logical, circular, arithmetic)							
Learning Outcome 2		Identifythe importance of various registers.					06		05 (PT)
Contents		<ul style="list-style-type: none">• Computer registers: accumulator registers, data registers, address registers, program counter, stack pointer, Instruction register, memory data register, memory buffer register, input register, output register, temporary register.• Common Bus System using different registers.							
Learning Outcome 3		Explain Instruction cycle and types of instructions					09		14

Contents	<ul style="list-style-type: none"> • Instruction codes, Stored Program Organization, Timing and control (Hardwired control and micro programmed control), Basic computer Instruction format, Instruction cycle • Types of instructions: memory- reference, register-reference and input-output registers, Instruction set completeness 		
Learning Outcome 4	Discuss Interrupt and its types.	05	05 (PT)
Contents	<ul style="list-style-type: none"> • Input-Output and Interrupt: Input-Output Configuration, Input-Output Instructions, Program Interrupt, Interrupt cycle 		
Method of Assessment	Paper pen test		
Course Outcome 2	Outline data processing of computer system.	18	20 (06+14)
Learning Outcome 1	Express different CPU Organization and instruction formats.	06	06 (TW)
Contents	<ul style="list-style-type: none"> • CPU organization: General register organization, stack organization(reverse polish notation) • Addressing modes: Implied mode, Immediate, register, register indirect, Auto increment or auto decrement Mode, direct, indirect, relative and indexed. • Instruction format: Three address, two address, one address and Zero address 		
Learning Outcome 2	Explain Data transfer and manipulation.	12	14
Contents	<ul style="list-style-type: none"> • Data transfer and manipulation: • Data Transfer Instructions, • Data Manipulation Instructions (Arithmetic Instructions, Logical and Bit Manipulation Instructions, Shift Instructions) 		

	<ul style="list-style-type: none"> • Program Control: Status Bit Conditions, Conditional Branch Instructions, Subroutine Call and Return, program interrupts • Types of Interrupts (external Interrupts, internal interrupts and software interrupts) • Reduced instruction set computers (RISC) and compare with Complex Instruction Set Computers (CISC). 		
Method of Assessment	Paper pen test		
Course Outcome 3	Classify different methods of computer input output processing	20	18 (04+14)
Learning Outcome 1	Explain I/O interface and mode of data transfer.	08	08
Contents	<ul style="list-style-type: none"> • Input-output interface: I/O bus and Interface Modules, I/O vs memory bus, Isolated vs memory mapped I/O, Example of I/O Interface • Mode of Data transfer: Synchronous and Asynchronous, Asynchronous data transfer using Strobe Control and Handshaking, Source -initiated strobe for data transfer, Destination-initiated strobe for data transfer, Source- initiated transfer using handshaking, Destination- initiated transfer using handshaking • Asynchronous serial transfer • Mode of Data Transfer B/w computer and I/O devices 		
Learning Outcome 2	Relate various types of Priority Interrupt.	06	06
Contents	<ul style="list-style-type: none"> • Priority Interrupt, Daisy-Chaining Priority, Parallel Priority Interrupt, Priority Encoder 		
Learning Outcome 3	Draw DMA architecture.	06	04 (TW)
Contents	<ul style="list-style-type: none"> • DMA controller, DMA Transfer 		
Method of Assessment	Paper pen test		

Course Outcome 4	Illustrate various level of a memory hierarchy.	22	24 (10+14)
Learning Outcome 1	Describe Memory Hierarchy and types of cache memory	14	14
Contents	<ul style="list-style-type: none"> • Main Memory: RAM and ROM chips, Memory Address map and memory Connection to CPU. • Auxiliary memory: Magnetic disks and magnetic tapes • Cache memory: Direct, Associative and Set Associative mapping 		
Learning Outcome 2	Discuss the importance of virtual memory management.	08	10 (PT)
Contents	<ul style="list-style-type: none"> • Virtual memory: Address Space and Memory space, Address mapping using pages, Memory management hardware 		
Method of Assessment	Paper pen test		