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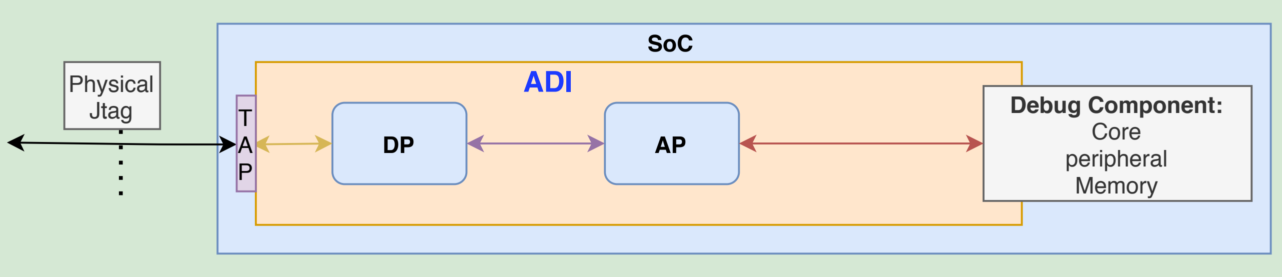


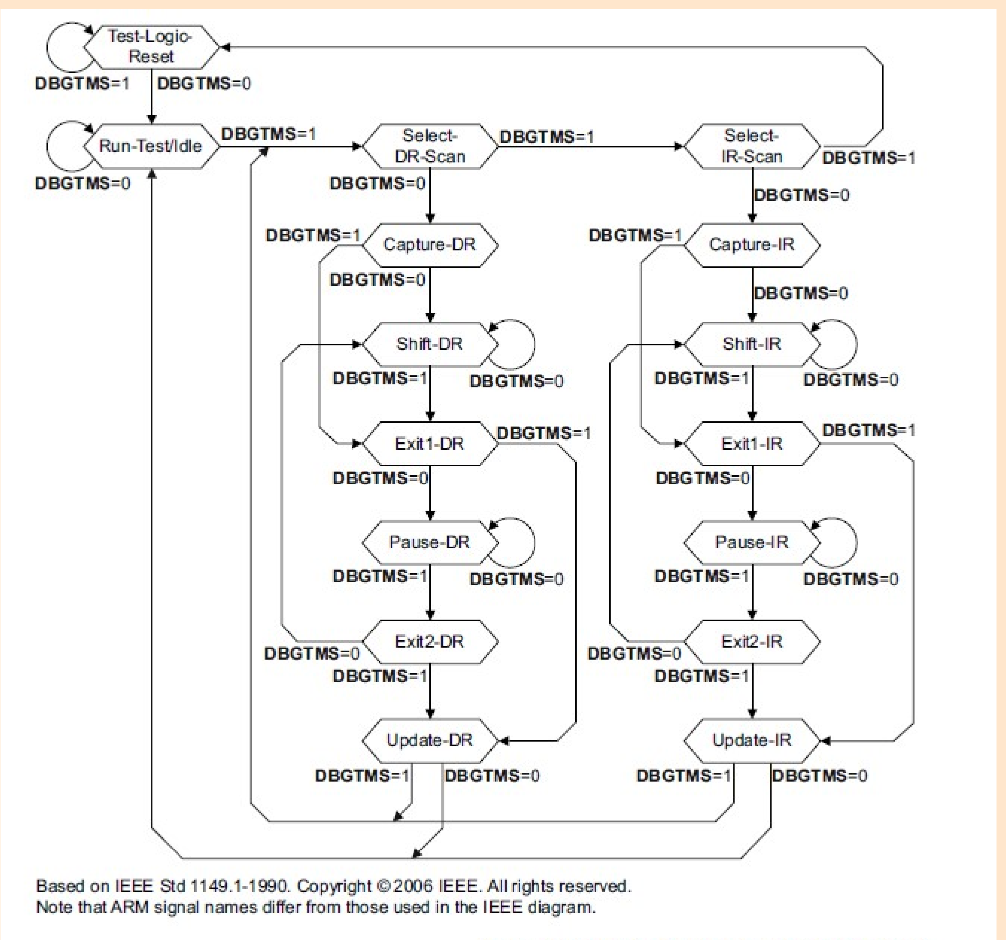


Figure B3-2 State diagram for the DBGTAPSM

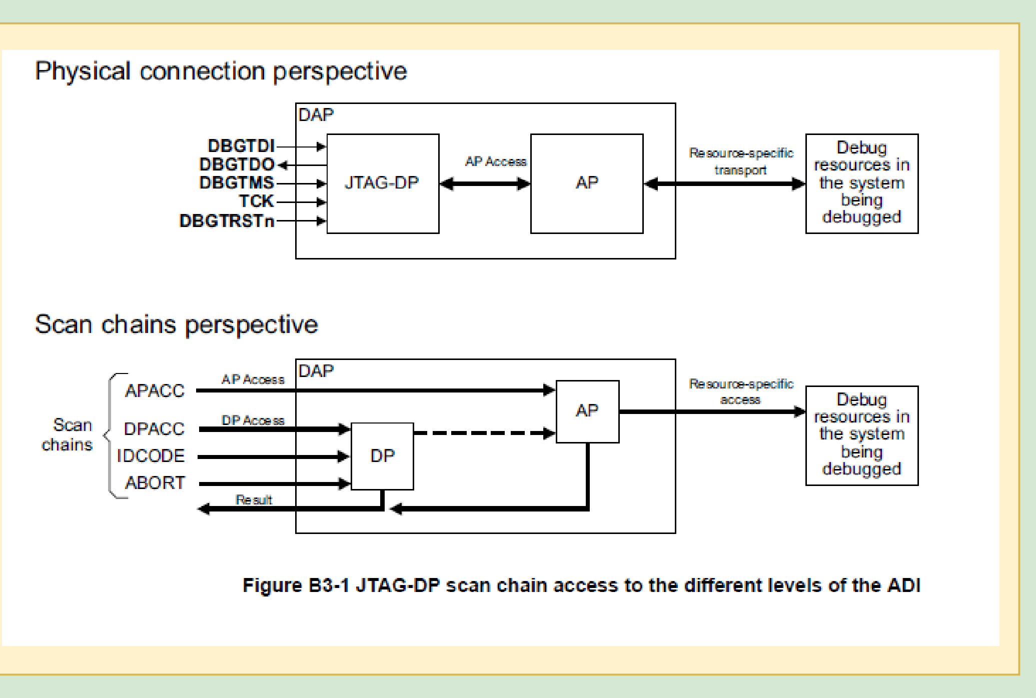
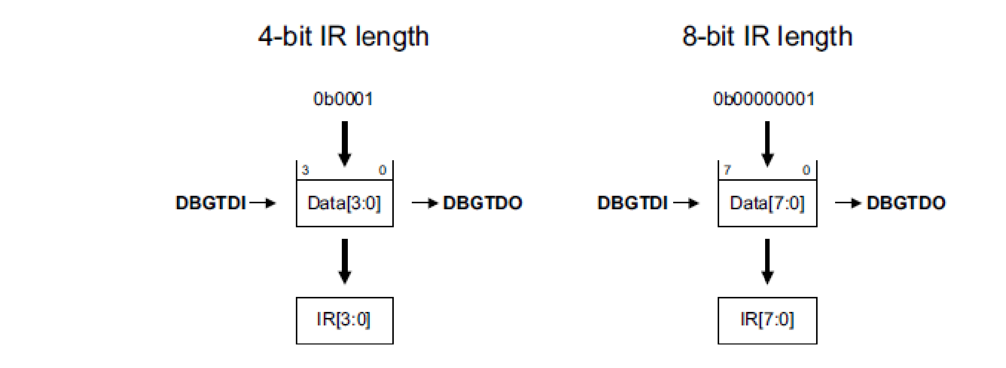


Figure B3-1 JTAG-DP scan chain access to the different levels of the ADI

Table B3-3 Standard IR instructions

4-bit IR instruction value	8-bit IR instruction value	Data register	DR scan length	Notes
0b0xxx	0b0xxxxxxx	-	-	*IMPLEMENTATION DEFINED extensions to the IR instruction set* on page B3-93.
-	0b10000000-0b11110111	-	-	Reserved.
0b1000	0b11111000	ABORT	35	-
0b1001	0b11111001	-	-	Reserved.
0b1010	0b11111010	DPACC	35	See *DPACC and APACC, JTAG-DP DP and AP Access registers* on page B3-97.
0b1011	0b11111011	APACC	35	
0b110x	0b1111110x	-	-	Reserved.
0b1110	0b11111110	IDCODE	32	-
0b1111	0b11111111	BYPASS	1	Required by JTAG specification.

The operation of the IR register is shown in the following figure:



The operation of the DPACC and APACC registers is shown in the following figure:

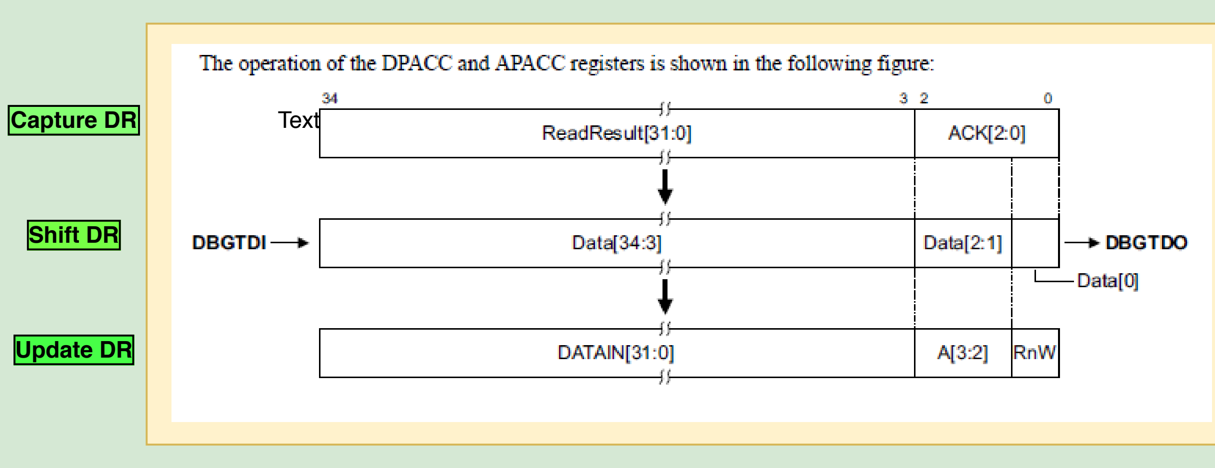
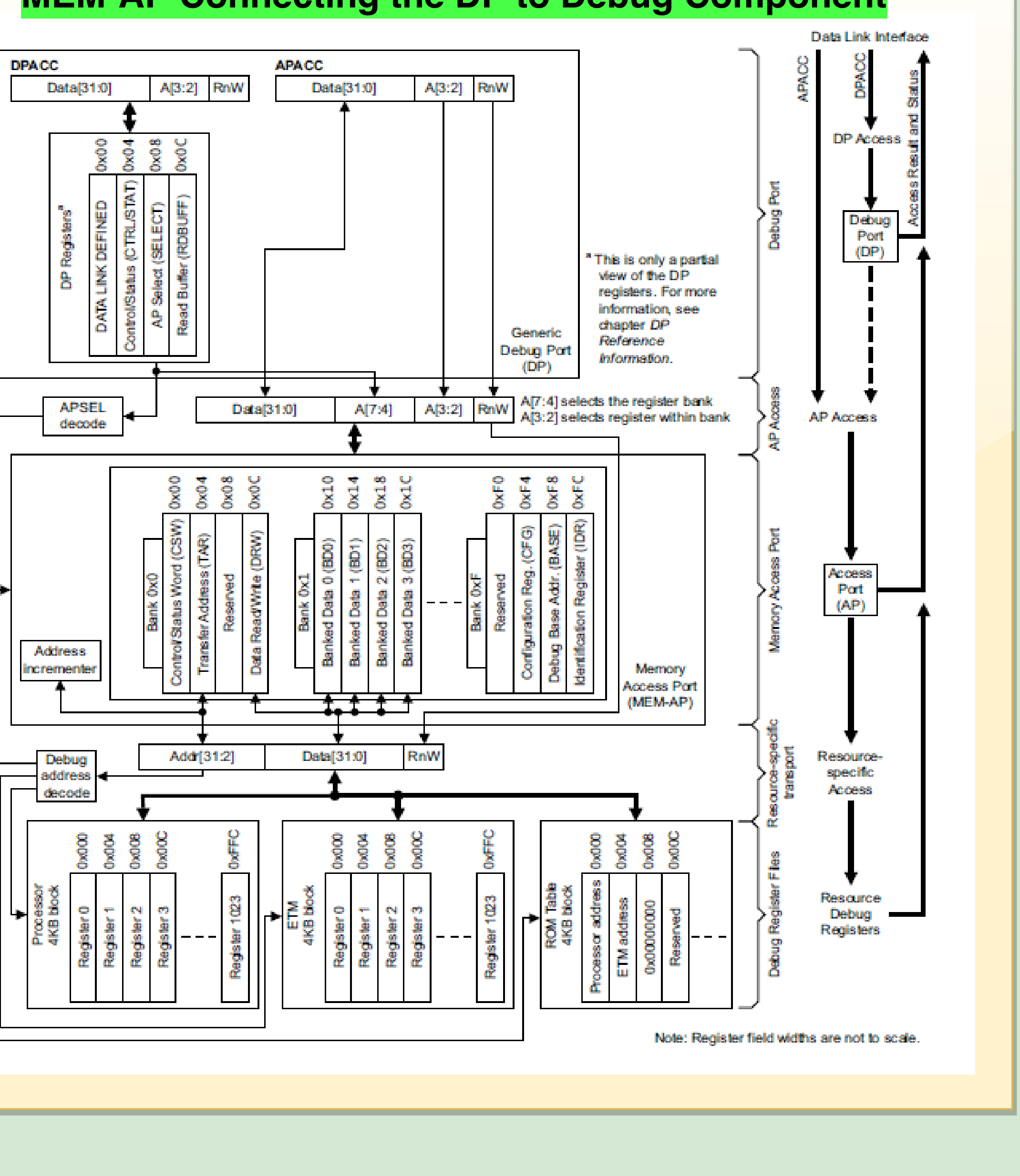


Table B3-6 DPACC and APACC ACK responses

Response	ACK[2:0] encoding	See:
OK/FAULT	0b010	*OK/FAULT response to a DPACC or APACC access*
WAIT	0b001	*WAIT response to a DPACC or APACC access* on page B3-99

MEM-AP Connecting the DP to Debug Component



Example : Access AP Register

To access Register at address 0x14 in the AP that is selected when SELECT.APSEL is 0x00 :

- **Use a DP register write to set:**

  — **SELECT.APSEL** to 0x00.
  — **SELECT.APBANKSEL** to 0x1. [0: 0x0-0xc, 1: 0x10-0x1c, 2: 0x20-0x2c ...]

- **Use an AP register access with A[3:2] = 0b01.**

Example : Access Processor Register

To Access the Processor Register 3 at addres 0x00C in Processor Register Bank is selected when Address is 0x0000000C :

1) The initial conditions are:
   Power Domain is enabled: Debug(Resouce or Component) + system
   CTRL/STAT.TRNMODE= 0b00 Normal operation. After a powerup reset, the value of this field is UNKNOWN.
   CSW.DeviceEn,
   CSW.DbgSwEnable

2) The DP SELECT register addresses a MEM-AP with a connection to the Memory Map Register Resource.

3) The AP TAR addresses the Address of the register of Resource.

4) Perform an AP write to DRW with the Data to Write/Read:
   If AP is ready, so the DP returns an OK/FAULT ACK response.
   Check CSW.TrInProg for status.
   Else Wait ACK Response:
   retry the DPACC or APACC access.

5) The TAR addresses the Address of the register of Resource, and the AP access consists of a write/read to the DRW.
   Therefore, the AP initiates a write/read to the Memory Map Register through it's connection to the Resource

6) Transfer of Write/Read completes.

NOTE:

- Implement Retry & Error Handling [ACK=WAIT,FAULT, STICKYERR , ORUNDETECT:STICKYORUN]

- Memory Read/Write transfer Status can be checked at: CSW.TrInProg
  0b0 The connection to the memory system is idle
  0b1 A transfer is in progress on the connection to the memory system.

- In case of stall access - on third write only we get ACK = WAIT

- ABORT forces an AP transaction abort.

- When an error is (Sticky)flagged, the current transaction is completed and subsequent APACC transactions are discarded until the sticky flag is cleared.

- Overrun detection: DPs support an overrun detection mode, which enables a debugger to send blocks of commands using a connection with high latency and high throughput.In overrun detection mode, the debugger must check the Sticky Overrun flag for overrun errors after each sequence of APACC transactions