ECEN 2350: Digital Logic Course Syllabus

Department of Electrical, Computer and Energy Engineering
College of Engineering and Applied Science, University of Colorado Boulder

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Instructor	Alex Fosdick	**Class Times**	MWF 11:00 - 11:50 am
Office	ECOT435	**Class Location**	Fleming 104
E-Mail	fosdick@colorado.edu	**Final Exam**	5/2 1:30pm - 4:00pm
OH	10-11am MW, TBD		

Course Overview

Prerequisites

- ECEN 1310 C-programming for ECE (or equivalent)

Class communications and Content

All communications with the professor should be made via email. The course website is https://ecee.colorado.edu/~ecen2350. However all content and grades will be posted on the D2L website https://learn.colorado.edu. Students will need to regular check their email for communications from the instructor.

Textbooks

- Fundamentals of Digital Logic with Verilog Design. Third Edition. Stephen Brown & Zvonko Vranesic, ISBN-13: 978-338054-4

Development Kits

The course will use the Altera ModelSim Software for Verilog simulations and the free version of the Altera Quartus II software for the design and implementation of digital logic.

The hardware that the course will use is the DE0, the FPGA development kit.developed by Terasic. This board can be purchased in the E-store. This is the same board that will be used in ECEN3350.

Course Objectives

For students to:

1. To understand how logic circuits are used to solve engineering problems.
2. To understand how logic circuits are analyzed, designed, verified, and tested.
3. To understand the relationship between abstract logic characterizations and the practical electrical implementations.

Learning outcomes

After taking this course students will be able to recognize and use the following concepts, ideas, and/or tools:

1. **Logic level models**, including Boolean algebra, finite state machines, and hardware description languages.
2. **Logic gates, memory**, including CMOS gates, flip-flops, arrays, and programmable logic.
3. **Design tools**, both manual and computerized, for design and test of logic circuits.
4. **Design criteria**, including area, speed, power consumption, and testability.

Topics

1. Boolean algebra
2. Logic Gates and networks
3. The Verilog HDL (Hardware Description Language)
4. Combinational logic circuit synthesis and optimization
5. Number representation and arithmetic circuits
6. CMOS technology and programmable logic
7. Flip-flops, registers and coutners
8. Finite state machines
9. Synchronous sequential circuits
10. Digital system design
11. Asynchronous sequential circuits
12. Testing and testability of logic circuits

Schedule

Week #	Dates	Schedule Notes
1	M: 1/11 S: 1/17	**Mon. 1/11:** Read Section 1.5, Digital Representation of Information and watch the screencast Digital Representation of Numbers and Letters. If you don't have the book yet, here is a scan of Chapter 1 **Wed. 1/13:** Watch the screencasts Decimal To Binary And Hexadecimal and Decimal Fraction to Binary Conversion. **Fri. 1/15:** Read Sections 2.1-2.4, Variables, Functions, Inversion, Truth Tables, Logic Gates and Networks and watch the screencasts Logic Functions: AND, OR, NOT and Analysis and Synthesis of Logic Networks. If you don't have the book yet, here is a scan of Chapter 2
2	M: 1/18 S: 1/24	**1/18 - MLK Day (No classes)** **1/20 - Last day to add class MyCUInfo** **Mon. 1/18:** *** Martin Luther King Jr. Day ***

		Wed. 1/20: Section 2.5, Boolean Algebra, Venn Diagrams. Related screencasts: Boolean Algebra Iand Boolean Algebra II and Boolean Identity Proofs and Boolean Algebra Example. **Fri. 1/22:** Sections 2.6-2.7, Synthesis Using AND, OR, NOT Gates, NAND and NOR Logic Networks. Related screencasts: Synthesis Using AND, OR, NOT Gates and NAND, NOR, Logic Networks and NAND/NOR Only Example.
3	M: 1/25 S: 1/31	1/27 - Last Day to Drop course (No Tuition/Fee charges) **Mon. 1/25:** Section 2.8, Design Examples. Related screencast: Logic Building Block Examples. **Wed. 1/27:** Sections 2.9-2.10, Introduction to CAD Tools, Introduction to Verilog. Related screencasts: Introduction to Verilog Part 1 and Introduction to Verilog Part 2. Download the Altera Software (Modelsim and Quartus II) and install it on your computer. It will be needed for the next homeworks. Also get the Terasic DE0 board (available at the e-store of the ECEE Department). **Fri. 1/29:** Section 2.11, Minimization and Karnaugh Maps. Related screencast: Minimization and Karnaugh Maps.
4	M: 2/1 S: 2/7	**Mon. 2/1:** Section 2.12-2.13, Strategy for Minimization, Minimization of Product-of-Sums Forms. Related screencasts: Strategy for Minimization and Prime Implicants and More. **Wed. 2/3:** TBD Related screencasts Intro to Verilog and ModelSim, Part1, Intro to Verilog and ModelSim, Part2, and Intro to Verilog and ModelSim, Part3. Watching these videos should also help you with Project 1. **Fri. 2/5 ***** Quiz 1 *****.** Closed book, closed notes, one sheet (8.5"x11", both sides, with your own notes) allowed. No calculators or cell phones. Covers Section 1.5, binary and hexadecimal representation of integers and fractions, and Chapter 2 in the book. For practice you can use some of the examples in Section 2.17 in the book, the problems from Chapter 2 which have a star next to them (solutions are at the end of the book), and the homework problems and their solutions.
5	M: 2/8 S: 2/14	**Mon. 2/8:** Section 2.14, Incompletely Specified Functions. Related screencast: Incompletely Specified Functions. **Wed. 2/10:** Sections 2.15, 3.1, Multiple-Output Circuits, Positional Number Representation. Related screencast: Number Representation. **Fri. 2/12:** Section 3.2, Addition of Unsigned Numbers. Related screencast: Addition of Unsigned Numbers.
6	M: 2/15	**Mon. 2/15:** Section 3.3, Signed Numbers. Related screencast: Signed Numbers, Part 1.

	S: 2/21	**Wed. 2/17:** Section 3.3, Signed Numbers. Related screencast: Signed Numbers, Part 2. **Fri. 2/19:** Section 3.4, Fast Adders. Related screencasts: Fast Adders, Part 1 and Fast Adders, Part 2.
7	M: 2/22 S: 2/28	**Mon. 2/22:** Section 3.5, Design of Arithmetic Circuits Using CAD Tools. Related screencast:Arithmetic Circuits in Verilog, Part 1. **Wed. 2/24:** Section 3.5, Design of Arithmetic Circuits Using CAD Tools. Click here for the Verilog Code Worksheet that we used in class. Related screencast: Arithmetic Circuits in Verilog, Part 2. **Fri. 2/26 ***** Quiz 2 *****.** Closed book, closed notes, one sheet (8.5"x11", both sides, with your own notes) allowed. No calculators or cell phones. Covers Section 1.5, binary and hexadecimal representation of integers and fractions, Chapter 2, and Sections 3.1-3.5 in the book. For practice you can use some of the examples in Sections 2.17 and 3.8 in the book, the problems from Chapters 2 and 3 which have a star next to them (solutions are at the end of the book), and the homework problems and their solutions.
8	M: 2/29 S: 3/6	**3/2 - Summer Registration Starts for continuing students, Fall schedule available** **Mon. 2/29:** Section 3.7, Other Number Representations: Binary Coded Decimal (BCD). Related screencasts: BCD Adder in Verilog. **Wed. 3/2:** Section 3.7, Other Number Representations: IEEE Floating Point Numbers. Related screencasts: Other Number Representations. **Fri. 3/4:** Section 4.1, Multiplexers, Verilog Worksheet.
9	M: 3/7 S: 3/13	**Mon. 3/7:** Appendix B.1, B.8, Transistor Switches, Practical Aspects. **Wed. 3/9:** Appendix B.3, B.8.8, CMOS Logic Gates, Transmission Gates. Related screencast: From Transistors to Gates. **Fri. 3/11:** Section 4.1, Multiplexers, Multiplexer Synthesis Using Shannon's Expansion. Related screencast: Multiplexers.
10	M: 3/14 S: 3/20	**Mon. 3/14:** Sections 4.2, 4.3, Decoders, Encoders. Related screencasts: Decoders, and Encoders. **Wed. 3/16:** Section 4.6, Verilog for Combinational Circuits. Related screencast: Verilog for Combinational Circuits. **Fri. 3/18: ***** Quiz 3 *****.** Closed book, closed notes, one sheet (8.5"x11", both sides, with your own notes) allowed. No calculators, cell phones, or smart watches. Covers Section 1.5, binary and hexadecimal representation of integers and fractions, Chapters 2, 3 (except Section 3.6), 4, and Appendix B (only Sections B.1-B.3 and B.8) in the book. For practice you can use some of the examples in Sections 2.17, 3.8, 4.8, and B.12 in the book, the problems

		from Chapters 2, 3, 4, and Appendix B which have a star next to them (solutions are at the end of the book), and the homework problems and their solutions.
11	M: 3/21 S: 3/27	3/21-3/25 - Spring Break **(No Classes)**
12	M: 3/28 S: 4/3	**3/28 - Fall registration starts for continuing students** **Mon. 3/28:** Section 4.6, Verilog for Combinational Circuits. Related screencast: Verilog for Combinational Circuits. **Wed. 3/30:** Section 5.1, Basic Latch. Related screencast: Latches. **Fri. 4/1:** Sections 5.2-5.3, Gated SR Latch, Gated D Latch. Related screencast: Latches.
13	M: 4/4 S: 4/10	**Mon. 4/4:** Sections 5.4-5.5, Edge-Triggered D Flip-Flops, T Flip-Flop. Related screencast: Edge-Triggered Flip-Flops. **Wed. 4/6:** Sections 5.6-5.8, JK Flip-Flop, Summary of Terminology, Registers. Related screencast:Different Types of Flip-Flops. **Fri. 4/8:** Section 5.9, Asynchronous Counters. Related screencast: Registers and Counters.
14	M: 4/11 S: 4/17	**Mon. 4/11:** Section 5.9, Synchronous Counters. Related screencast: Synchronous Counters. **Wed. 4/13:** Sections 5.10-5.12, Reset Synchronization, Other Types of Counters, Using Storage Elements with CAD Tools. Related screencasts: Other Types of Counters, and Verilog for Storage Elements, Part 1, and Verilog for Storage Elements, Part 2. **Fri. 4/15: ***** Quiz 4 *****.** Closed book, closed notes, one sheet (8.5"x11", both sides, with your own notes) allowed. No calculators, cell phones, or smart watches. Covers Section 1.5, binary and hexadecimal representation of integers and fractions, Chapters 2, 3 (except Section 3.6), 4, Appendix B (only Sections B.1-B.3 and B.8), and Chapter 5 (up to and including Section 5.11) in the book. For practice you can use some of the examples in Sections 2.17, 3.8, 4.8, B.12, and 5.17 in the book, the problems from Chapters 2, 3, 4, Appendix B, and Chapter 5 which have a star next to them (solutions are at the end of the book), and the homework problems and their solutions.
15	M: 4/18 S: 4/24	**Mon. 4/18:** Section 5.13, Using Verilog Constructs for Registers and Counters. Related screencast:Verilog for Registers and Counters. **Wed. 4/20:** Section 6.1, Basic Design Steps (Synchronous Sequential Circuits). Related screencast:FSM: Basic Design Steps, Part 1, and FSM: Basic Design Steps, Part 2, **Fri. 4/22:** Sections 6.2 and 6.3, State-Assignment Problem, Mealy State Model. Related screencasts: State Assignment Problem and Mealy State Model.
16	M: 4/25 S: 5/1	**4/29 - Last day of Classes**

		Mon. 4/25: Sections 6.4 and 6.5, Design of Finite State Machines Using CAD Tools, Serial Adder Example. Related screencast: Finite State Machines in Verilog. **Wed. 4/27:** Sections 6.6 and 6.7, State Minimization, Design of a Counter Using the Sequential Circuit Approach. Related screencasts: State Minimization, Part 1 and State Minimization, Part 2and Counter Design Using FSM Approach. **Fri. 4/29:** Sections 6.8, 6.9 and 6.10, FSM as an Arbiter Circuit, Analysis of Synchronous Sequential Circuits, Algorithmic State Machine (ASM) Charts. Related screencast: Algorithmic State Machine (ASM) Charts.
17	M: 5/2 S: 5/8	**5/1 - 5/5 - Final Exams Week** **5/2 1:30 am - 4:00 pm Final Exam**

Evaluation and Grading Procedure

Grading

Grading breakdown can be seen in the table below.

Homework: 10% (Weekly, due Mondays)
Clicker Questions: 10%
Projects: 20%
Quizzes (4x): 10% (each)
Final Exam: 20%

Reading

Reading selections have been posted with each week's lecture. Students are expected to keep up on the reading material from the course textbook.

Homework

Expect weekly homework assignments covering material from the text and lecture. Students may collaborate together on homework, but each student must turn an individual paper with problem solutions. All homework and reports must be legibly written or typed. All homework assignments must be turned in at the start of the class or, if submitted electronically, prior to the class period they are due.

Projects

For each project you are asked to solve a specific problem, implement your solution in Verilog, observe the results on the DE0 board, and then draw conclusions and improve and embellish your solution as necessary. You have to document your strategy for solving the problem, the Verilog code, and the results that you observed in a short report. You submit your project by uploading your report and the zipped Verilog project files (including the .sof file and all .v files) to the dropbox on D2L for the corresponding project. The projects are individual efforts, but feel free to discuss ideas with other students in the class. **Submissions with identical Verilog code and/or identical reports will not be accepted**.

Late Homework/Project Policy

No Late Homework. Assignments need to be turned it at the beginning of class when due, or submitted online by the due date. Save all your assignments and verify your score with scores that are posted on the D2L site. Any questions regarding score need to occur as soon as possible after assignment will be handed back. End of the semester regrades will not be accepted. Please alert me to any conflicts (travels, religious observances, family events) you have with exams or turning in homework ASAP. If I don't hear from you, I can't help you. This does not mean the day before the assignment.

Examinations

There will be scheduled quizzes roughly every couple of weeks over material since the last quiz. There will be a final examination that is cumulative. These assessments are to be done using individual effort alone.

Make-up Exam Policy

No make-up exams are given except for medical or other similar hardships where advanced arrangements are made with the instructor; or in case of non-selective medical emergencies with physician's note or documentation. Otherwise, failure to take the exam at the scheduled time will result in a zero grade in the exam. Students are responsible for checking final exam times within the first few weeks of the semester to reschedule them. More information can be read at http://www.colorado.edu/policies/final-examination-policy.

Attendance and Participation

Attendance at every class is expected. It is the student's responsibility to obtain materials handed out in a lecture which the student missed. Students are expected to keep up with the course material. If you get confused or start to fall behind, attend office hours or schedule an appointment with the professor as soon as possible. If you must miss a lecture, please let the instructor know in advance, if possible. Students are expected to participate in class discussions of course topics. Students must obtain an iclicker to participate in class questions and polls, which is available from http://www.colorado.edu/oit/services/teaching-learning-tools/cuclickers. In addition, students are expected to assist other students in understanding course material and assignments.
Students are expected to complete assignments on time. Project assignments will be accepted late, but the grade earned on the assignment will be reduced. Expectations for Out-of-Class Study: Beyond the time required to attend each class meeting, students enrolled in this course should expect to spend at least an additional 3 hours per week of their own time in course-related activities, including reading required materials, completing assignments, preparing for exams, etc.

University Policies

In general all university policies can be looked up at the follow link:
http://www.colorado.edu/policies

Honor Code and Academic Integrity

All students enrolled in a University of Colorado Boulder course are responsible for knowing and adhering to the academic integrity policy of the institution (http://www.colorado.edu/policies/academic-integrity-policy). Violations of the policy may include: plagiarism, cheating, fabrication, lying, bribery,

threat, unauthorized access, clicker fraud, resubmission, and aiding academic dishonesty. Credit must be clearly given for code or designs legally borrowed from others. Submission of project work performed previously or concurrently for a different course constitutes cheating, if instructor consent is not obtained prior to submission. When in doubt, ask the instructor for clarification. All incidents of academic misconduct will be reported to the Honor Code Council (honor@colorado.edu; 303-735-2273). Students who are found responsible of violating the academic integrity policy will be subject to nonacademic sanctions from the Honor Code Council as well as academic sanctions from the faculty member. Additional information regarding the academic integrity policy can be found at http://honorcode.colorado.edu.

Accommodations and Disability Services

If you qualify for accommodations because of a disability, please submit to your professor a letter from Disability Services in a timely manner so that your needs may be addressed. Disability Services (303.492.8671, dsinfo@colorado.edu) determines accommodations based on documented disabilities. If you have a temporary medical condition or injury, see Temporary medical conditions (http://www.colorado.edu/disabilityservices/students/temporary-medical-conditions) under Quick Links at Disability Services website (http://disabilityservices.colorado.edu/) and discuss your needs with your professor.

Religious Observances

Every effort will be made to reasonably and fairly deal with students who have serious religious observances that conflict with mandatory lectures, scheduled exams, assignments, etc. Please notify your professor well in advance, so that there is time to make adequate arrangements. See campus policy regarding religious for details. Info can be found at the links below.
http://www.colorado.edu/policies/observance-religious-holidays-and-absences-classes-andor-exams

Discrimination and Harassment

The University of Colorado Boulder (CU-Boulder) is committed to maintaining a positive learning, working, and living environment. CU-Boulder will not tolerate acts of sexual misconduct, discrimination, harassment or related retaliation against or by any employee or student. CU's Sexual Misconduct Policy prohibits sexual assault, sexual exploitation, sexual harassment, intimate partner abuse (dating or domestic violence), stalking or related retaliation. CU-Boulder's Discrimination and Harassment Policy prohibits discrimination, harassment or related retaliation based on race, color, national origin, sex, pregnancy, age, disability, creed, religion, sexual orientation, gender identity, gender expression, veteran status, political affiliation or political philosophy. Individuals who believe they have been subject to misconduct under either policy should contact the Office of Institutional Equity and Compliance (OIEC) at 303-492-2127. Information about the OIEC, the above referenced policies, and the campus resources available to assist individuals regarding sexual misconduct, discrimination, harassment or related retaliation can be found at the OIEC website (http://www.colorado.edu/institutionalequity/).

Classroom Behavior

Students and faculty each have responsibility for maintaining an appropriate learning environment. Those who fail to adhere to such behavioral standards may be subject to discipline. Professional courtesy and sensitivity are especially important with respect to individuals and topics dealing with

differences of race, color, culture, religion, creed, politics, veteran's status, sexual orientation, gender, gender identity and gender expression, age, disability, and nationalities. Class rosters are provided to the instructor with the student's legal name. I will gladly honor your request to address you by an alternate name or gender pronoun. Please advise me of this preference early in the semester so that I may make appropriate changes to my records. For more information, Information regarding campus policies can be read at the urls below.
http://www.colorado.edu/policies/student-classroom-and-course-related-behavior
http://www.colorado.edu/osc/sites/default/files/attached-files/osc_handbook_2015-16.pdf.
http://www.colorado.edu/institutionalequity/
http://www.colorado.edu/policies/discrimination-and-harassment-policy-and-procedures