**AM04 MICROPROCESSOR**

**Description**

The AM04 is a RISC microprocessor based on the MIPS 1 ISA rev 3.2. It implements a subset of the full MIPS 1 ISA and is designed around a 32-bit architecture. The AM04 is a working synthesisable MIPS-compatible CPU, that uses a memory-mapped bus, allowing it to access system memory and various peripherals. The AM04 can be integrated on any FPGA or ASIC having been tested on Cyclone IV E.

**AM04 Architecture**

The AM04 defines a 32-bit word, a 16-bit half word and an 8bit byte. The byte ordering is Little-Endian format.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 31 24 | 23 16 | 15 8 | 7 0 | Word Address |
| Byte-F | Byte-E | Byte-D | Byte-C | C |
| Byte-B | Byte-A | Byte-9 | Byte-8 | 8 |
| Byte-7 | Byte-6 | Byte-5 | Byte-4 | 4 |
| Byte-3 | Byte-2 | Byte-1 | Byte-0 | 0 |

**Figure 1** Little Endian Byte Alignment

**Processor Resources**

The AM04 provides thirty-two 32-bit wide registers referred to as GPRs (General Purpose Registers). The AM04 also contains 3 special registers: the program counter (*PC*), the results of multiply / divide *Hi* and *Lo*. Furthermore, the AM04 also utilises an ALU for arithmetic calculations, comparisons, and operations.

The program counter provides the address of the next instruction. The *Hi* register stores the result of the most significant 32 bits in a multiply instruction, and the remainder in a divide instruction. The *Lo* register stores the result of the least significant 32 bits in a multiply instruction, and the quotient in a divide instruction.

The ALU can perform the following operations: unsigned