4-bit Comparator Design and Implementation

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1 Introduction

1.1 Objective of Project

- To Design a 4-bit comparator circuit using Verilog HDL.
- Implement the circuit using gate level modelling.
- Verify the functionality of the design using simulation tools.
- Use Xilinx Vivado software to compile the Verilog code and generate a bit stream file.
- Deploy the bit stream on an Artix-7™ Field Programmable Gate Array (FPGA) from Xilinx.
- Verify the functionality of the circuit on the FPGA by comparing 4-bit BCD numbers.
- Ensure that the circuit can detect the three conditions: A equals B (AEB), A less than B (ALB), and A greater than B (AGB).
- Demonstrate the usefulness of the circuit as a component in digital systems and its potential applications.

1.2 Description of Project

The project involves the design and implementation of a 4-bit comparator using Verilog HDL and Xilinx Vivado software. The aim of the project is to create a circuit that can compare two 4-bit numbers A and B, which are represented in binary-coded decimal (BCD) format, and output whether A is equal to, less than, or greater than B. The design is implemented using gate level modelling, which involves the use of logic gates to construct the circuit.

Verilog HDL is a hardware description language that is widely used for designing digital circuits. The Vivado software from Xilinx is a popular tool for designing and programming FPGAs. The software provides a graphical user interface (GUI) that allows designers to create and edit designs using a block diagram approach. Vivado also includes a simulator for testing and verifying the design before it is implemented on the FPGA.

Once the design is complete, the next step is to create a bit stream that can be deployed on an Artix-7™ Field Programmable Gate Array (FPGA) from Xilinx. The Xilinx part number used for this project is XC7A100T-1CSG324C. The FPGA is a programmable integrated circuit that can be configured to perform a specific function, in this case, the 4-bit comparator circuit.

To deploy the bit stream on the FPGA, the Verilog code is compiled using the Vivado software, which generates a bit stream file that can be loaded onto the FPGA. The design is synthesized, implemented, and then programmed onto the device. The synthesized design is mapped onto the specific logic cells and interconnect resources available on the FPGA, and then the resulting configuration file is loaded onto the device.

Once the design is deployed on the FPGA, it can be used to compare 4-bit BCD numbers. The circuit is capable of detecting three conditions: A equals B (AEB), A less than B (ALB), and A greater than B (AGB). The output of the circuit indicates which of these conditions is true, based on the inputs A and B.

Overall, the project demonstrates the use of Verilog HDL, gate level modelling, and FPGA programming using Xilinx Vivado to implement a digital circuit that performs a specific function. The resulting 4-bit comparator circuit is a useful component in many digital systems and can be used in a wide range of applications.

2 Designing of 4-bit comparator

2.1 Designing of 4-bit comparator.

4-bit comparator is intended to compare two 4-bit binary numbers, the circuit will have eight inputs and three outputs. The inputs will be the two 4-bit binary numbers, labelled A and B, and each bit of the numbers will be labelled A3-A0 and B3-B0, respectively. The outputs will be three bits that indicate the relationship between the two numbers, labelled AGT, ALT, and AEQ, which stand for A greater than B, A less than B, and A equal to B, respectively.

The 4-bit comparator can be constructed using four 1-bit comparators, each of which will compare one bit of the two input numbers. The output of each 1-bit comparator will be connected to the inputs of a combinational logic circuit that will determine the overall relationship between the two numbers.

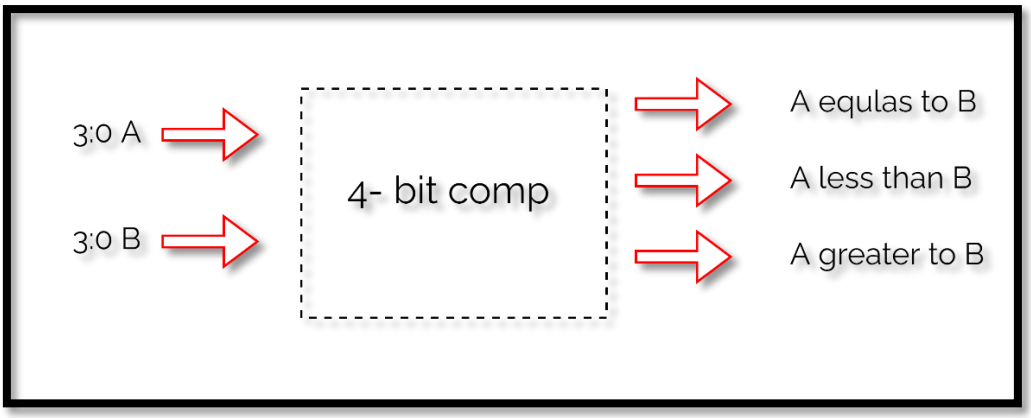

Figure 1:4-bit Comparator

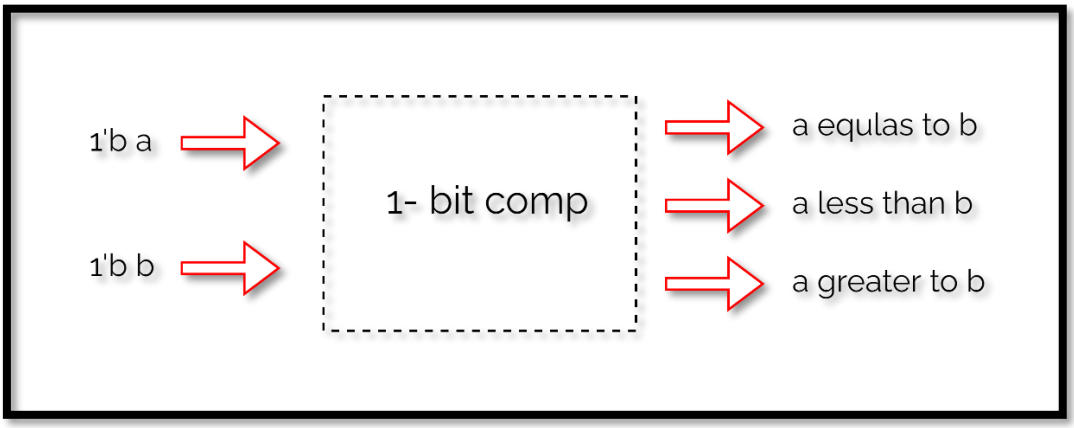

Figure 2:1-bit Comparator

2.2 RTL Schematic

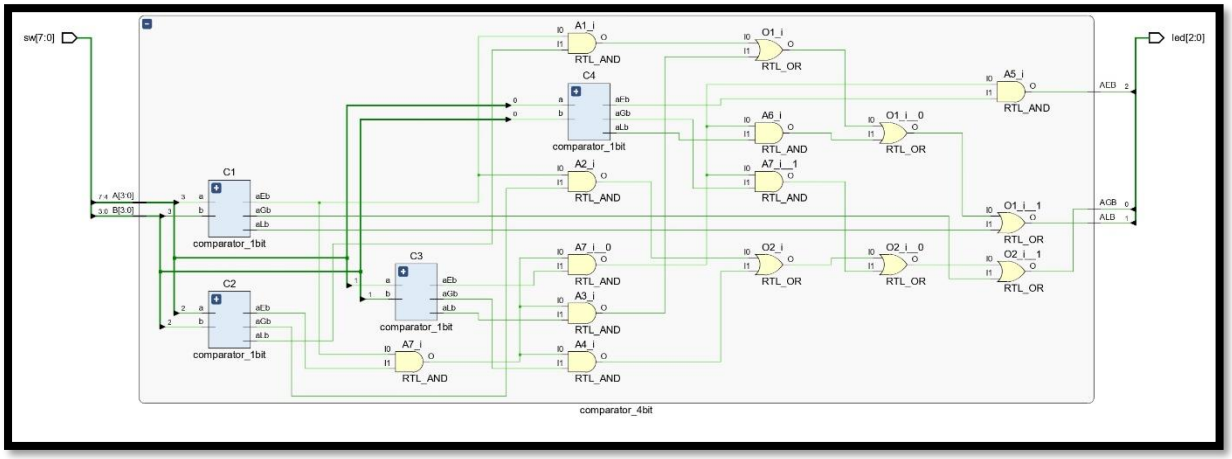

Figure 3:4-bit comparator RTL diagram

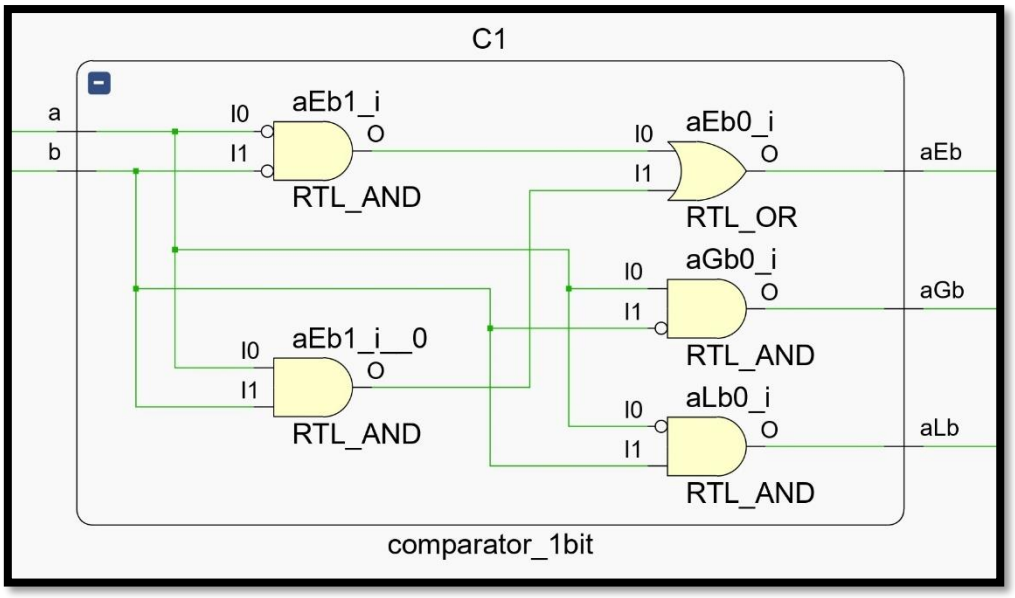

Figure 4:1-bit comparator

2.3 Verilog code

```
module comparator_1bit(aEb,aLb,aGb,a,b);
output reg aEb,aLb,aGb;
input a,b;
always@(a,b)
begin
aEb=(~a&~b)|(a&b);
aLb=(~a&b);
aGb=(a&~b);
end
endmodule
```

```
module comparator_4bit(AEB,ALB,AGB,A,B);
output AEB,ALB,AGB;
input [3:0]A;
input [3:0]B;
wire [1:18]w;
comparator_1bit C1(w[1],w[17],w[18],A[3],B[3]);
comparator_1bit C2(w[2],w[3],w[4],A[2],B[2]);
comparator_1bit C3(w[5],w[6],w[7],A[1],B[1]);
comparator_1bit C4(w[8],w[9],w[10],A[0],B[0]);
and A1(w[11],w[1],w[3]);
and A2(w[12],w[1],w[4]);
and A3(w[13],w[1],w[2],w[6]);
and A4(w[14],w[1],w[2],w[7]);
and A5(AEB,w[1],w[2],w[5],w[8]);
and A6(w[15],w[1],w[2],w[5],w[9]);
and A7(w[16],w[1],w[2],w[5],w[10]);
or O1(ALB,w[11],w[13],w[15],w[17]);
or O2(AGB,w[12],w[14],w[16],w[18]);
endmodule


module top_comparator_4bit(led,sw);
output [2:0]led;
input [7:0]sw;
//comparator_4bit(AEB,ALB,AGB,A,B);
comparator_4bit
uut(led[2],led[1],led[0],sw[7:4],sw[3:0]);
endmodule
```

3 Hardware Deployment

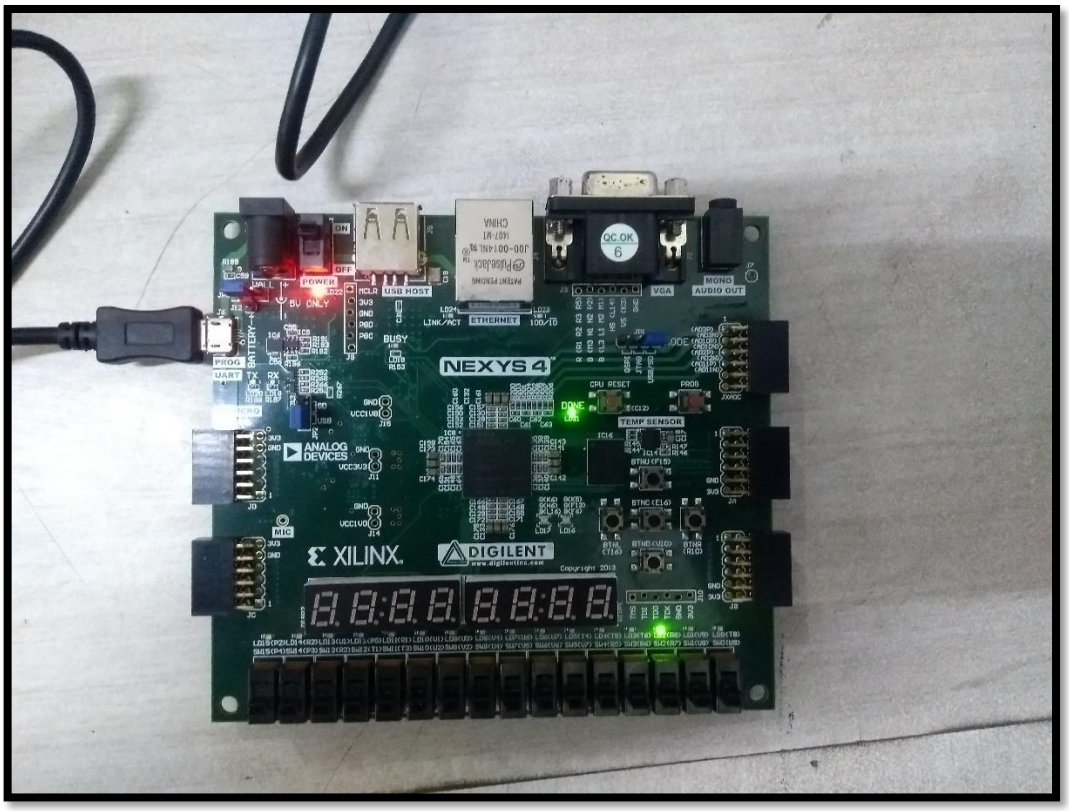

Figure 5:A equals to B

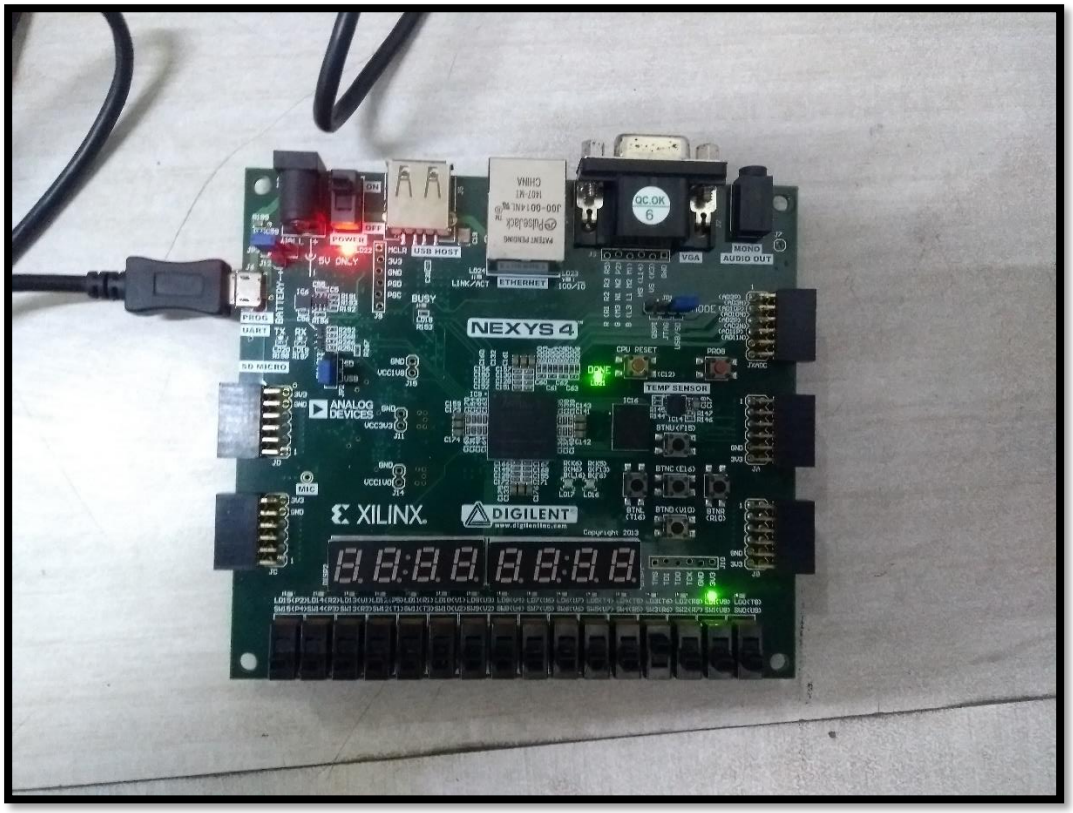

Figure 6:A less than B

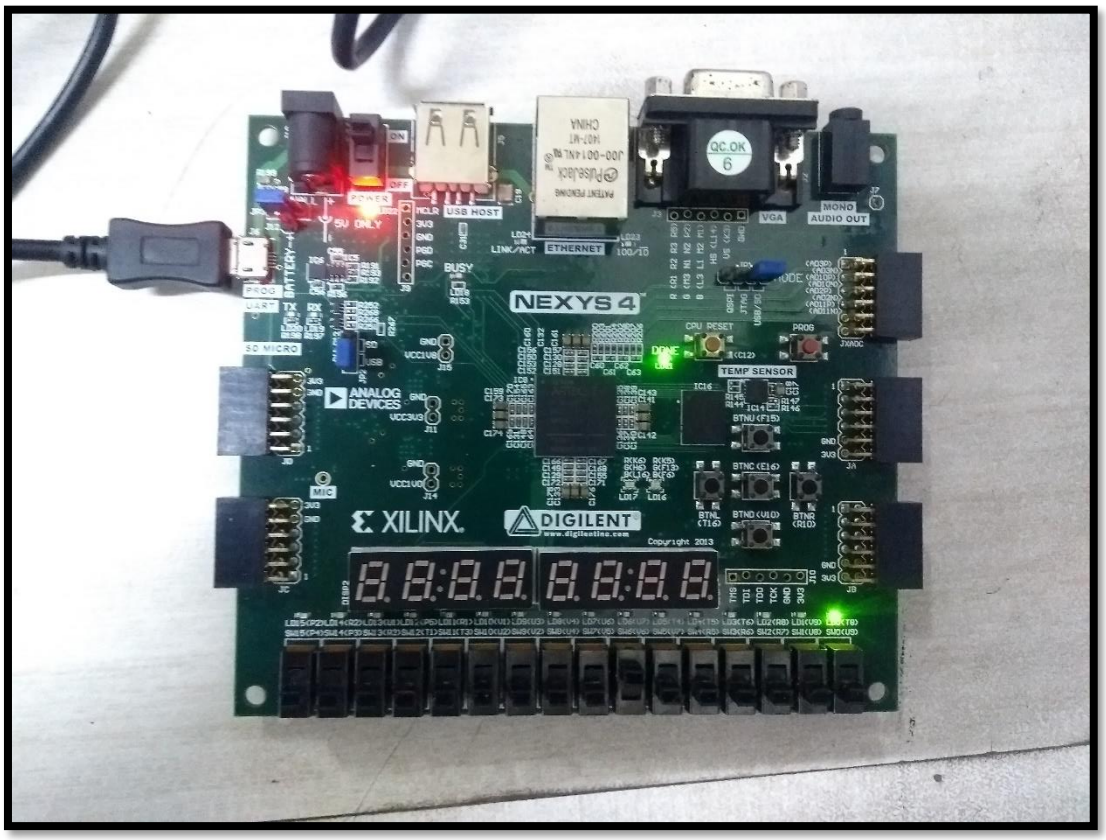

Figure 7:A greater than B

4 Conclusion

In conclusion, the project successfully demonstrated the design and implementation of a 4-bit comparator circuit using Verilog HDL and Xilinx Vivado software. The circuit was designed to compare two 4-bit numbers represented in BCD format and output whether A is equal to, less than, or greater than B.

The gate level modeling approach was used to construct the circuit using logic gates, and the Xilinx Artix-7 FPGA was used to deploy the bit stream generated from the Verilog code. The resulting circuit is capable of detecting the three comparison conditions: A equals B, A less than B, and A greater than B.

The project provided a practical demonstration of the use of Verilog HDL and FPGA programming for digital circuit design. The skills and knowledge gained from this project can be applied in a wide range of digital systems and applications. The project also demonstrated the importance of testing and verifying the design using the Vivado simulator before deploying the circuit on the FPGA.

Overall, the project was a success and achieved its objectives of designing and implementing a 4-bit comparator circuit using Verilog HDL and Xilinx Vivado software.