Design of Differential Voltage Sense Amplifier with CMOS 45nm Technology

Jay Baswaraj Khaple

School of Electronics and Electrical Engineering

Lovely Professional University

Phagwara, India.

Registration no.12011859.

Abstract—In this report a CMOS based differential voltage sense amplifier is presented which operates at 1v power supply and with 45nm technology node. This sense amplifier provides a gain of 10.45db with maximum delay of 13.36ps. The average total power consumption is 8.812uW.

Keywords—Gain, delay, average total power.

I. Introduction

The growing gap between the processor and embedded memory speed is a major setback in the overall performance of electronic system. Since the sense amplifier (SA) forms an integral part of the read circuitry in both volatile memories, such as SRAM, and non-volatile memories (NVMs), such as FLASH, its performance has a significant effect on the overall performance of memory. Access time, offset, power and area are the four important performance metrics of SA. The memory access time and input-offset of SA greatly affect the speed of the entire memory and therefore to patch up the gap between processor and memory speed, the SA is required to be fast and efficient. As one SA is employed for each bitline in the memory array, it is required to be compact in size and should have low power consumption. Furthermore, scaling in technology makes it difficult to control the fabrication process leading to variation in process parameters causing unpredictability in the performance of SAs. Therefore, it is very important to keep this aspect in mind while designing and estimating the performance metrics of the SA. (Arora, 2015)

In modern computer memory, a SA is one of the elements which make up the circuitry on a semiconductor memory chip (integrated circuit); the term itself dates to the era of magnetic core memory. A SA is part of the read circuitry that is used when data is read from the memory; its role is to sense the low power signals from a bitline that represents a data bit (1 or 0) stored in a memory cell and amplify the small voltage swing to recognizable logic levels so the data can be interpreted properly by logic outside the memory. (contributors, 2022)

II. Operations

A. Memory chip operation

The data in a semiconductor memory chip is stored in tiny circuits called memory cells. Sense Amplifiers are primarily applied in Volatile memory cells. The memory cells are either SRAM or DRAM cells which are laid out in rows and columns on the chip. Each line is attached to each cell in the row. The lines which run along the rows are called wordlines which are activated by putting a voltage on it. The lines which run along the columns are called bit-line and two such complementary bitlines are attached to a sense amplifier at the edge of the array. Number of sense amplifiers are of that of the “bitline” on the chip. Each cell lies at the intersection of a particular wordline and bitline, which can be used to “address” it. The data in the cells is read or written by the same bit-lines which run along the top of the rows and columns. (contributors, 2022)

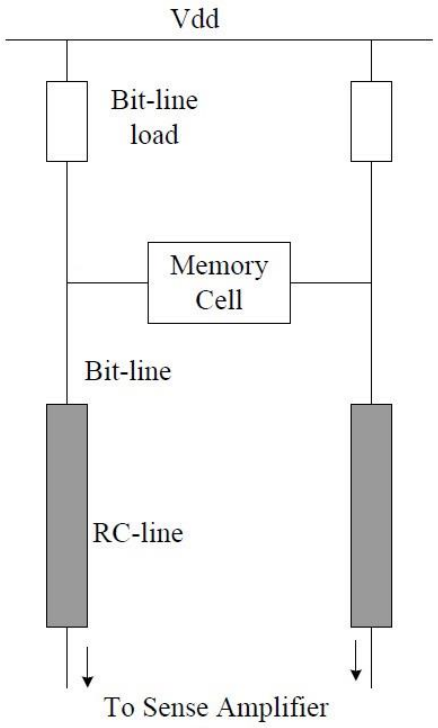

Figure 1: Memory with bitlines

Source: File:Sense Amp position.jpg - https://en.wikipedia.org

B. SRAM operation

To read a bit from a particular memory cell, the wordline along the cell's row is turned on, activating all the cells in the row. The stored value (Logic 0 or 1) from the cell then comes to the Bit-lines associated with it. The sense amplifier at the end of the two complementary bit-lines amplify the small voltages to a normal logic level. The bit from the desired cell is then latched from the cell's sense amplifier into a buffer and put on the output bus.

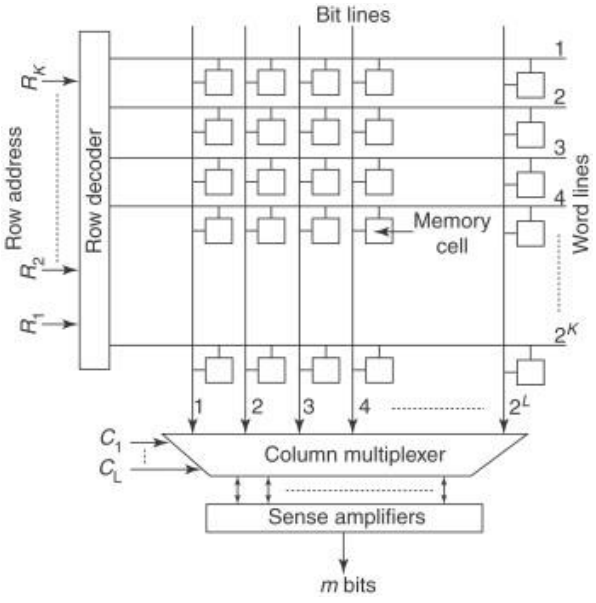

Figure 2: Memory cell array overview

C. DRAM operation

The sense amplifier operation in DRAM is quite like the SRAM, but it performs an additional function. The data in DRAM chips is stored as electric charge in tiny capacitors in the memory cells. The read operation depletes the charge in a cell, destroying the data, so after the data is read out the sense amplifier must immediately write it back in the cell by applying a voltage to it, recharging the capacitor. This is called memory refresh.

III. Differential Voltage Sense Amplifier

The basic MOS differential voltage sense amplifier circuit contains all elements required for differential sensing. A differential amplifier takes small signal differential inputs and amplifies them to a large signal single ended output. The effectiveness of a differential amplifier is characterized by its ability to reject common noise and amplify true difference between the signals. Because of rather slow operational speed provided at considerable power dissipation and inherently high offset basic differential voltage amplifier is not applied in memories. (Garg & Tonk, 2015)

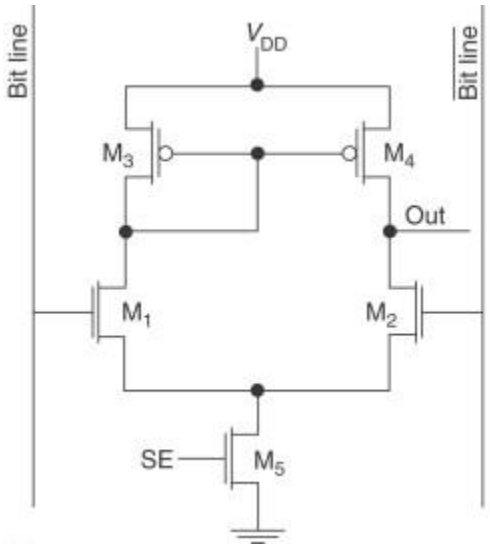

Figure 3: Differential Voltage Sense Amplifier

IV. Design of Basic Differential Voltage Sense Amplifier

Implementation of basic differential amplifier is done with the help 'Cadence Virtuoso' EDA tool, which is one the widely used tool in industry. Figure 4 shows the entire design of basic differential voltage sense amplifier which consist of a differential amplifier with bitline (BL) and bitline bar (BL') as the differential inputs along with the sense enable (SE). Whenever the SE pin is high the differential voltage sense amplifier will detect the small voltage input and amplify it into normal voltage and will give desired output in logic 1 and 0.

In addition to differential voltage sense amplifier in figure 4, there is a buffer, which is designed using two inverters connected in cascade, for storing the desired output and to do analysis on it.

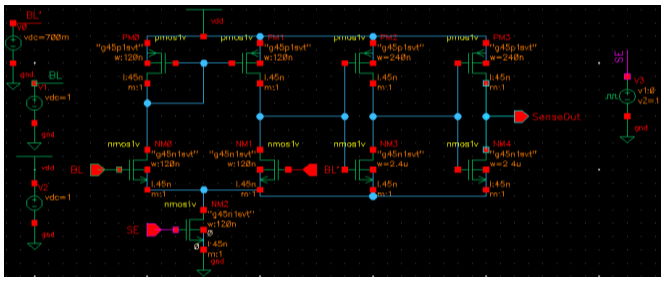

Figure 4:Design of Differential Voltage Sense Amplifier

As it is shown it the figure 4, differential inputs are as 1 V and 0.7 V, with Vdd=1 V. There will be two cases according to the input combination given to BL and BL'. Figure 5 and figure 6 shows the exact result generated on the bases of following input combinations.

a) Case 1: when BL = 1 V; BL'=0.7 V i.e. when Bl>BL' then sense-out => logic high.

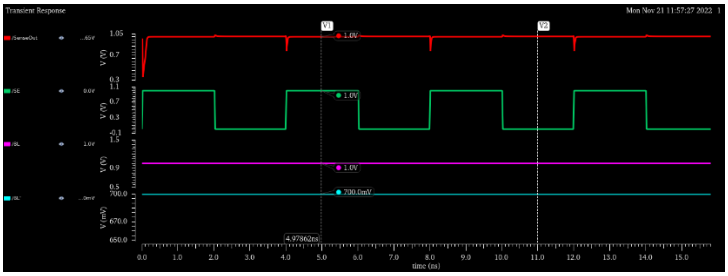

Figure 5:Sense-out when BL>BL'

b) Case 2: when BL = 0.7 V; BL'=1 V i.e. when Bl<BL' then sense-out => logic low.

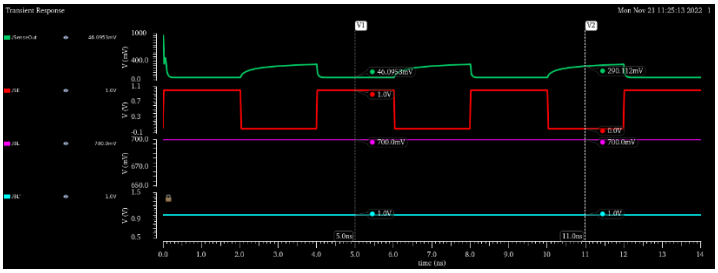

Figure 6:Sense-out when BL<BL'

There is no change in the sense-out when the sense enable is logic low, as a result sense-out stores the previous value irrespective of the inputs.

Table 1

	MOSFET Parameters	
Device	Length(L)	Width (W)
PM0	45 nm	120 nm
PM1	45 nm	120 nm
PM2	45 nm	240 nm
PM3	45 nm	240 nm
NM0	45 nm	120 nm
NM1	45 nm	120 nm
NM2	45 nm	120 nm
NM3	45 nm	2.4 um
NM4	45 nm	2.4 um

Table 1 consists of all MOSFET parameters used in the design of sense amplifier.

V. Analysis of Basic Differential Voltage Sense Amplifier

a. Power analysis

For the above design average total power's analysis is done using the EDA tool and shown in figure 7

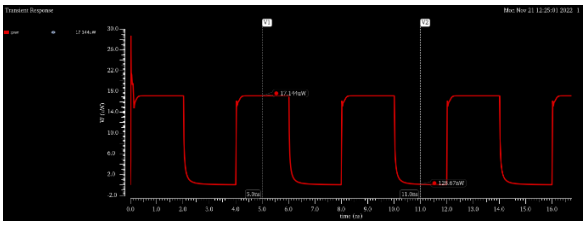

Figure 7: Power Plot when BL>BL'

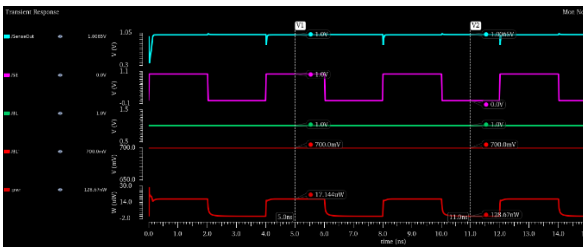

Figure 8: Power Plot when BL>BL'

After taking the average of the Power plot with the help of inbuilt calculator in cadence, the average total Power = **8.812uW**.

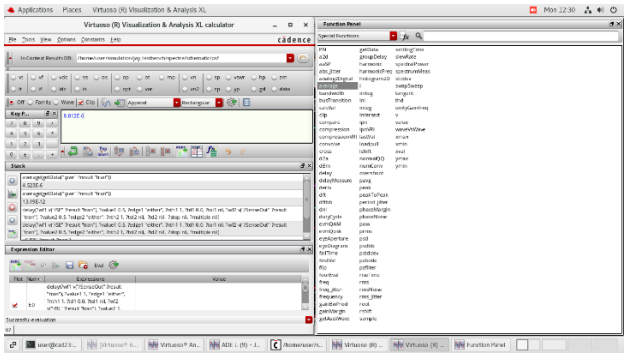

Figure 9:Average total power when BL>BL'

Similarly, the average total power plot is obtained when BL<BL'.

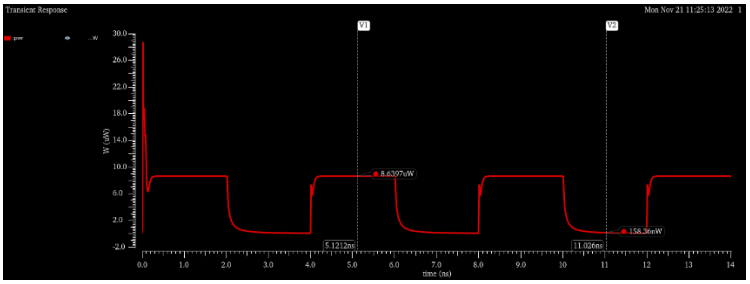

Figure 10:Power Plot when BL<BL'

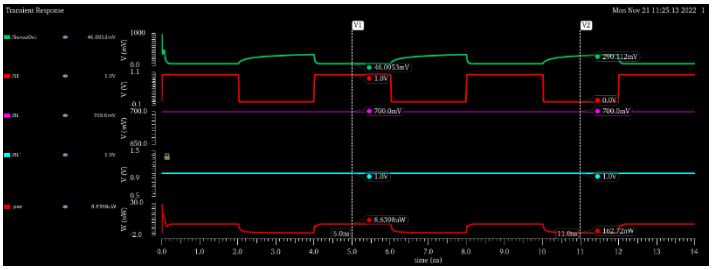

Figure 11:Power Plot when BL<BL'

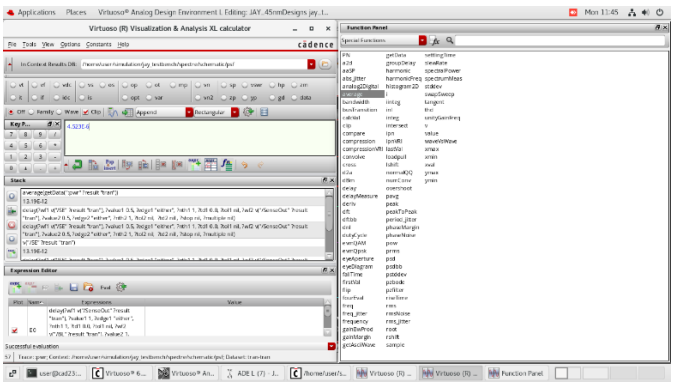

Figure 12:Average Power Plot BL<BL'

b. Delay analysis

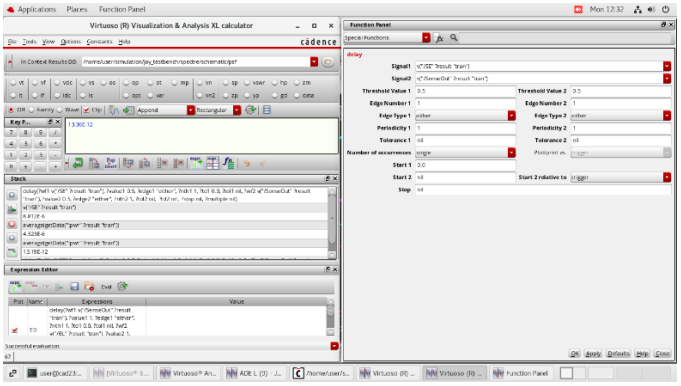

Figure 13:Delay from SE to Sense-out

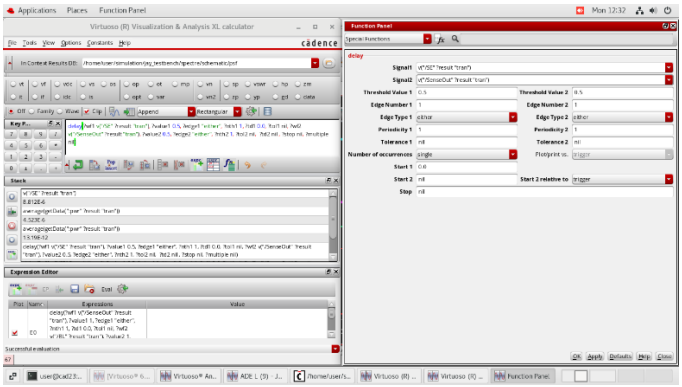

Figure 14:Delay equation

As show in the figure 13 the maximum delay of this sense amplifier is **13.36 ps.**

VI. Conclusion

In this design, we have satisfied all the parameters in the requirement and specially we achieved low power consumption and least delay. By comparison we found that the simulation result is a little different from out theoretical design due to some unavoidable conditions. But after all, our calculation has represented the real situation and offered great help in the design of the Basic Differential Voltage Sense Amplifier.

VII. References

Aggarwal, A., shukla, A., & Chauh, A. (2017). 6T SRAM Architecture & Implementation at CMOS 45nm. *Department of Electronics & Communication Engineering* (p. 56). Phagwara : Lovely Professional University.

Arora, D. (2015). *Design and Analysis of Sense Amplifier Topologies for Volatile and NonVolatile Memories.* New Delhi: Indraprastha Institute of Information Technology.

contributors, W. (2022, October 6). Sense amplifier. *Wikipedia, The Free Encyclopedia.*, p. 1. Retrieved from https://en.wikipedia.org/w/index.php?title=Sense_amplifier&oldid=1114466019

Garg, M. R., & Tonk, A. (2015). A Study of Different Types of Voltage & Current Sense Amplifiers used in SRAM. *International Journal of Advanced Research in Computer and Communication Engineering* (p. 6). Faridabad,India: IJARCCE.