MINGJIE LIU

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PhD Student ◇ Department of Eletrical and Computer Engineering

RESEARCH INTERESTS

Machine learning for design automation and analog design automation.

EDUCATION

The University of Texas at Austin, TX, USA *Aug. 2018 – Current*
PhD Student, Electrical and Computer Engineering
Advisor: David Z. Pan

University of Michigan, Ann Arbor, MI, USA *Sep. 2016 – May 2018*
MS in Electrical and Computer Engineering
GPA: 4.0/4.0

Peking University, Beijing, CN *Sep. 2012 – June 2016*
BS in Microelectronics, BE in Economics
GPA: 89.9/100 (cummulative) 91.7/100 (major)

EXPERIENCE

The University of Texas at Austin, TX, USA *Sep. 2018 – Current*
Research Assitant at UTDA Lab

- Analog layout automation tool: MAGICAL
- Bayesian optimization assisted analog layout generation
- Analog placement quality prediction with convolutional neural networks
- Graph heuristics and learning for analog symmetry constraint detection
- Guided analog routing with Autoencoders

Nvidia Corporation, TX, USA *June 2020 – Sep. 2020*
Research Intern

- Parasitic-aware transistor sizing with Bayesian optimization
- Layout parasitic prediction with graph neural networks

Micron Technology, CA, USA *May. 2017 – Aug. 2017*
Design Engineer Intern

- Output buffer design
- Custom logic path timing optimization

RELATED COURSES

The University of Texas at Austin

- EE382M: VLSI CAD and Optimization
- EE382M: VLSI Phys Design Automation
- EE381V: Reinforcement Learning
- EE381V: Combinatorial Optimization
- ORI391Q: Integer Programming

University of Michigan, Ann Arbor

- EECS545: Machine Learning
- EECS511: A/D Interfaces
- EECS522: Analog Integrated Circuits
- EECS413: Monolithic Amplifier Circuits
- EECS427: VLSI Design I
- EECS470: Computer Architecture

SKILLS

- Experience with machine learning frameworks, such as Tensorflow and PyTorch
- Experience with Bayesian optimization and reinforcement learning
- Understanding of EDA algorithms
- Experience with commercial EDA software
- Familiar with analog circuit and sytem designs, including data converters and PLLs

AWARDS AND HONORS

Best Paper Award	ASPDAC	2020
Best Paper Award Nomination	ASPDAC	2020
Graduate School Fellowship	The University of Texas at Austin	2018
Graduation of Honor	Peking University	2016
Fangzheng Scholarship	Peking University	2015
Samsung Scholarship	Peking University	2014
EECS Departmental Fellowship (No. 8508)	Peking University	2013

PUBLICATIONS

First Authored Papers

I7 Hao Chen*, **Mingjie Liu***, Xiyuan Tang*, Keren Zhu*, Nan Sun and David Z. Pan, "MAGICAL 1.0: An Open-Source Fully-Automated AMS Layout Synthesis Framework Verified With a 40-nm 1GS/s $\Delta\Sigma$ ADC", IEEE Custom Integrated Circuits Conference (CICC), April 25-30, 2021. *indicates equal contributions

I6 **Mingjie Liu**, Walker Turner, George Kokai, Brucek Khailany, David Z. Pan and Haoxing Ren, "Parasitic-Aware Analog Circuit Sizing with Graph Neural Networks and Bayesian Optimization", IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE), Feb. 01-05, 2021.

I5 **Mingjie Liu**, Keren Zhu, Xiyuan Tang, Biying Xu, Wei Shi, Nan Sun and David Z. Pan, "Closing the Design Loop: Bayesian Optimization Assisted Hierarchical Analog Layout Synthesis", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, July 19-23, 2020.

I4 **Mingjie Liu***, Keren Zhu*, Jiaqi Gu, Linxiao Shen, Xiyuan Tang, Nan Sun and David Z. Pan, "Towards Decrypting the Art of Analog Layout: Placement Quality Prediction via Transfer Learning", IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE), Grenoble, France, Mar. 09-13, 2020. *indicates equal contributions

I3 **Mingjie Liu**, Wuxi Li, Keren Zhu, Biying Xu, Yibo Lin, Linxiao Shen, Xiyuan Tang, Nan Sun and David Z. Pan, "S3DET: Detecting System Symmetry Constraints for Analog Circuits with Graph Similarity", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Beijing, China, January 13-16, 2020. **Best Paper Nomination**

I2 Hao Chen*, **Mingjie Liu***, Xiyuan Tang*, Keren Zhu*, Nan Sun and David Z. Pan, "Challenges and Opportunities Toward Fully Automated Analog Layout Design", Journal of Semiconductors, 2020. *indicates equal contributions

I1 Hao Chen*, **Mingjie Liu***, Biying Xu*, Keren Zhu*, Xiyuan Tang, Shaolan Li, Yibo Lin, Nan Sun and David Z. Pan, "MAGICAL: An Open-Source Fully Automated Analog IC Layout System from Netlist to GDSII", IEEE Design & Test, 2020. *indicates equal contributions

Conference Papers

C12 Zixuan Jiang, Jiaqi Gu, **Mingjie Liu**, Keren Zhu, and David Z. Pan, "Optimizer Fusion: Efficient Training with Better Locality and Parallelism", International Conference on Learning Representations (ICLR), Workshop on Hardware Aware Efficient Training (HAET), May 07, 2021.

C11 Xiaohan Gao, **Mingjie Liu**, David Z. Pan and Yibo Lin, "Interactive Analog Layout Editing with Instant Placement Legalization", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, July 11-15, 2021.

C10 Hao Chen, Keren Zhu, **Mingjie Liu**, Xiyuan Tang, Nan Sun, and David Z. Pan, "Universal Symmetry Constraint Extraction for Analog and Mixed-Signal Circuits with Graph Neural Networks", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, July 11-15, 2021.

C9 Jiaqi Gu, Chenghao Feng, Zheng Zhao, Zhoufeng Ying, **Mingjie Liu**, Ray T. Chen and David Z. Pan, "SqueezeLight: Towards Scalable Optical Neural Networks with Multi-Operand Ring Resonators", IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE), Feb. 01-05, 2021.

C8 Keren Zhu, **Mingjie Liu**, Hao Chen, Zheng Zhao and David Z. Pan, "Exploring Logic Optimizations with Reinforcement Learning and Graph Convolutional Network", 2nd ACM/IEEE Workshop on Machine Learning for CAD (MLCAD), November 16-20, 2020.

C7 Xiaohan Gao, Chenhui Deng, **Mingjie Liu**, Zhiru Zhang, David Z. Pan and Yibo Lin, "Layout Symmetry Annotation for Analog Circuits with Graph Neural Networks", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Tokyo, Japan, January 18-21, 2021.

C6 Hao Chen, Keren Zhu, **Mingjie Liu**, Xiyuan Tang, Nan Sun and David Z. Pan, "Toward Silicon-Proven Detailed Routing for Analog and Mixed-Signal Circuits", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), November 02-05, 2020.

C5 Keren Zhu, Hao Chen, **Mingjie Liu**, Xiyuan Tang, Nan Sun and David Z. Pan, "Effective Analog/Mixed-Signal Circuit Placement Considering System Signal Flow", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), November 02-05, 2020.

C4 Zixuan Jiang, Keren Zhu, **Mingjie Liu**, Jiaqi Gu and David Z. Pan, "An Efficient Training Framework for Reversible Neural Architectures", European Conference on Computer Vision (ECCV), Glasgow, United Kingdom, August 23-27, 2020.

C3 Jiaqi Gu, Zheng Zhao, Chenghao Feng, **Mingjie Liu**, Ray T. Chen, David Z. Pan, "Towards Area-Efficient Optical Neural Networks: An FFT-based Architecture", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Beijing, China, January 13-16, 2020. **Best Paper Award**

C2 Biying Xu, Keren Zhu, **Mingjie Liu**, Yibo Lin, Shaolan Li, Xiyuan Tang, Nan Sun, and David Z. Pan, "MAGICAL: Toward Fully Automated Analog IC Layout Leveraging Human and Machine Intelligence", IEEE International Conference on Computer-Aided Design (ICCAD), Westminster, CO, USA, November 4-7, 2019. Invited Paper

C1 Keren Zhu, **Mingjie Liu**, Yibo Lin, Biying Xu, Shaolan Li, Xiyuan Tang, Nan Sun and David Z. Pan, "GeniusRoute: A New Routing Paradigm Using Generative Neural Network Guidance for Analog Circuits", IEEE International Conference on Computer-Aided Design (ICCAD), Westminster, CO, USA, November 4-7, 2019.

Journal Papers

J1 Jiaqi Gu, Zheng Zhao, Chenghao Feng, Zhoufeng Ying, **Mingjie Liu**, Ray T. Chen and David Z. Pan, "Towards Hardware-Efficient Optical Neural Networks: Beyond FFT Architecture via Joint Learnability", IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems (TCAD), September, 2020.

COURSE PROJECTS

Multidisciplinary Design Project with Texas Instruments *Sep. 2017 – May 2018*

- X-band radar front end design with TI chips
- Matched filter signal processing backend for improved SNR

Course Project for A/D Interface *Jan. 2018 – May 2018*

- Third order continuous time $\Delta\Sigma$ ADC with chopping and FIR noise filtering

Course Project for Computer Architecture *Jan. 2017 – May 2017*

- 64-bit P6 based 2-way superscaler RISC processor design in synthesizable verilog

Course Project for VLSI Design I *Sep. 2016 – Jan. 2017*

- 16-bit 300MHz custom designed RISC processor core
- Custom designed 0.37V 8T SRAM with leakage compensation