Closing the Design Loop: Bayesian Optimization Assisted Hierarchical Analog Layout Synthesis

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Speaker Bio

- Mingjie Liu
- The University of Texas at Austin

Mingjie Liu Mingjie Liu received his B.S degree from Peking University and M.S. degree from the University of Michigan, Ann Arbor in 2016 and 2018, respectively. He is currently pursuing his Ph.D. degree in Electrical and Computer Engineering at The University of Texas at Austin. His current research interests include applied machine learning for design automation, and physical design automation for analog and mixed-signal integrated circuits.

Analog Design and Challenges

- The world is analog
- Increased demands of analog IC
  - Communication
  - Automotive
  - Healthcare
  - Advanced computing

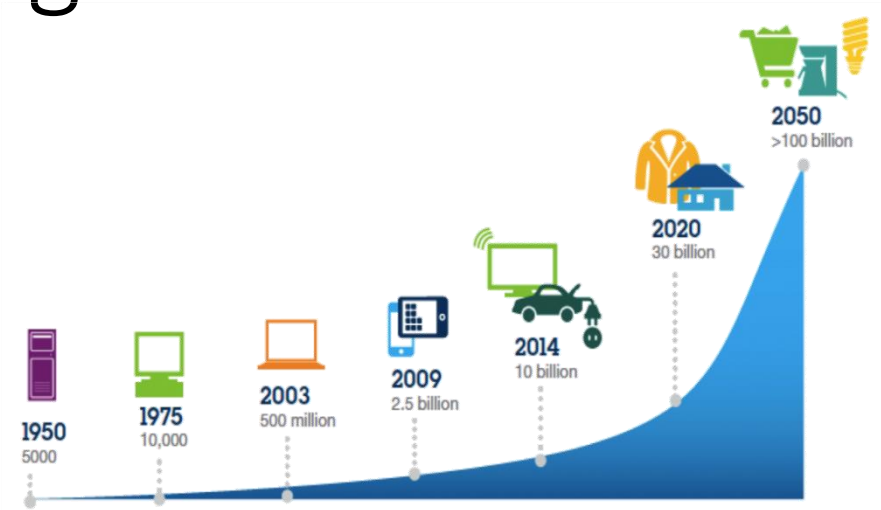
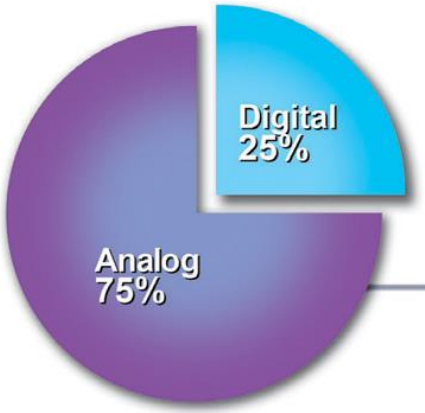
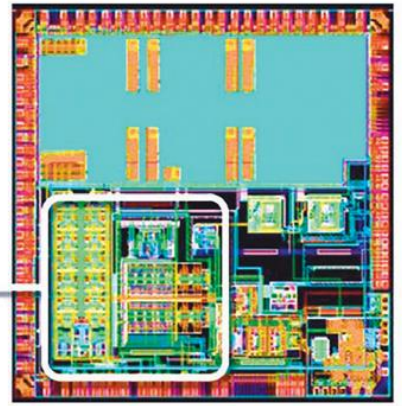


Image Sources: IBM, Ansys, public technology

- Heavily manual with limited automation



Design Efforts

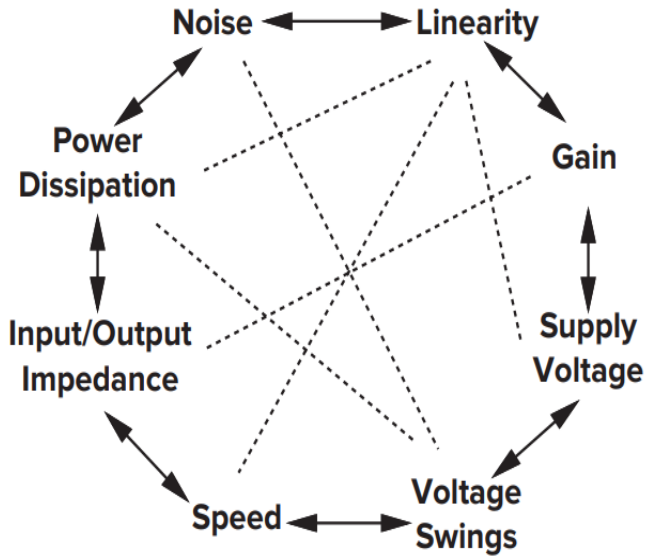


Mixed-Signal SoC

Image Sources: IBS and Dr. Handel Jones, 2012

Analog Layout Design and Challenges

- Analog IC layout design is still heavily manual
  - Compared with digital
  - Time-consuming and error-prone
  - Complex design rules
- Difficulties for automated analog layout
  - Sensitive layout effects
  - Complex performance trade-offs
  - No governing optimization targets



Courtesy [Razavi, Design of Analog IC]

Analog Layout Design and Challenges

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  - Time-consuming and error-prone
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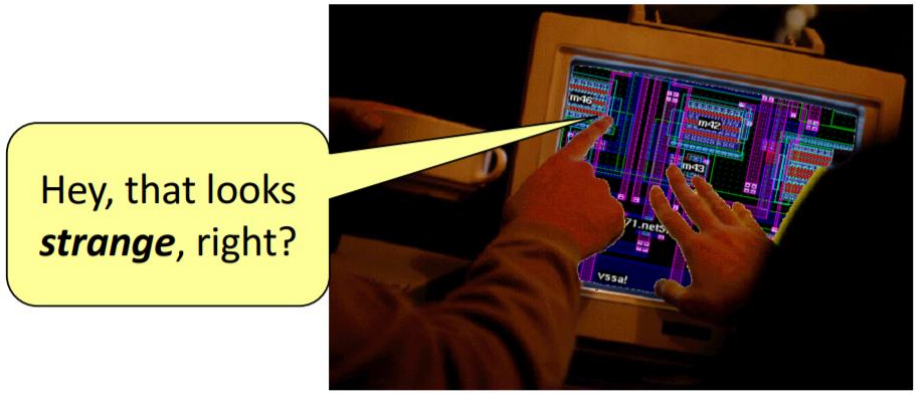
- Difficulties for automated analog layout
  - Sensitive layout effects
  - Complex performance trade-offs
  - No governing optimization targets
- As a result analog layout rely on
  - Human experience
  - Heuristic constraints
  - Aesthetic engineering



Courtesy [Rutenbar, TCACE'16]

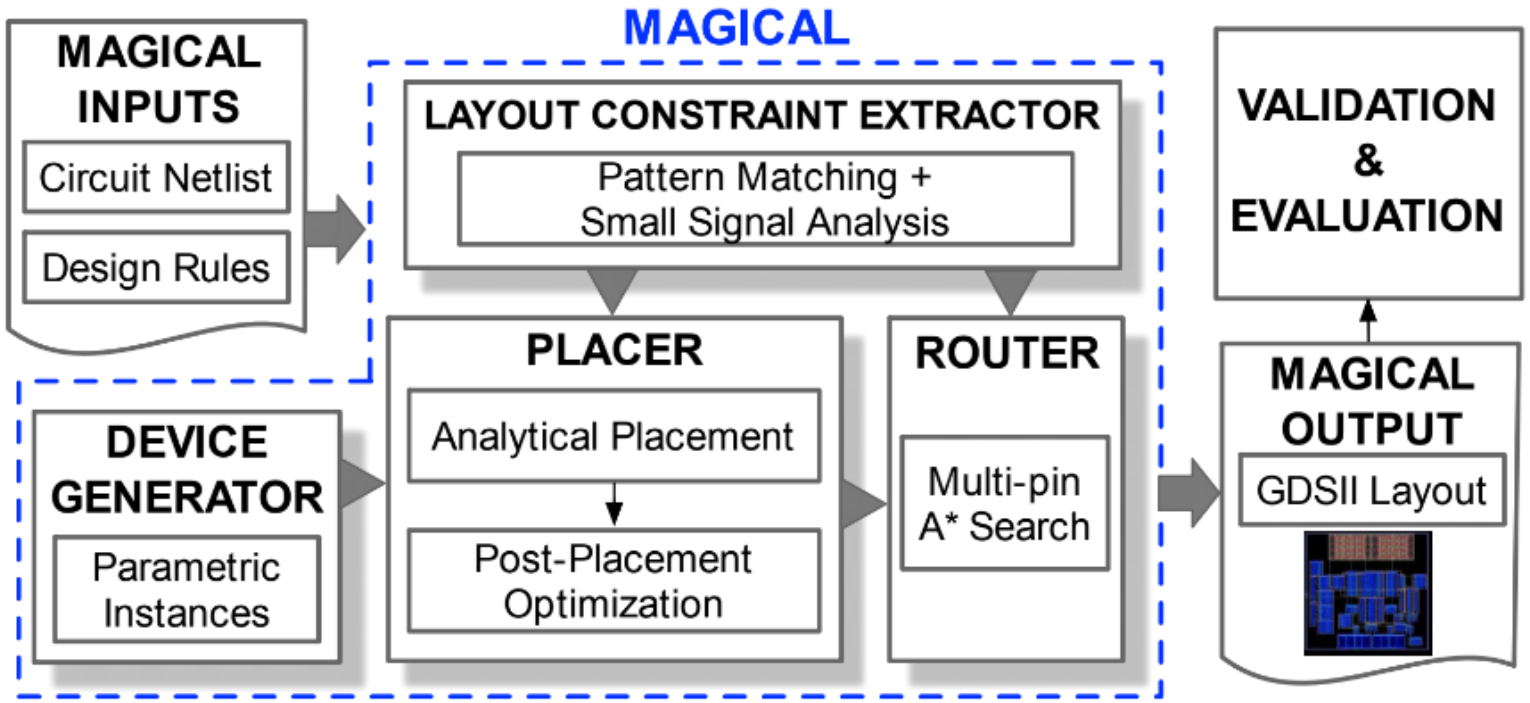
Prior Analog Layout Synthesis Tools

- Procedural layout generators [Crossley+, ICCAD'13]
  - Require manual efforts
  - Encode placement location, routing topology etc.
  - Efficient design reuse and technology migration
- Optimization-based layout tools [Meyer+, JSSC'93] [Cohn+, JSSC'91] [Kunal+, DAC'19]
  - Require heuristic constraints: symmetry, proximity, etc.
  - Constraints are design specific
- Performance-driven layout approach [Ou+, DAC'15] [Lampaert+, JSSC'95]
  - Derive layout effects analytically or with sensitivity analysis
  - Not accurate and difficult to model in advanced nodes

Our Contributions

- Ideally, we want to achieve
  - Little to no human in-the-loop
  - Sign-off quality layouts meeting various performance metrics
  - Scalable to handle system level designs
- Our Contributions:
  - Fully automated layout generation from netlist to GDSII layout
  - Bayesian optimization leveraging simulation results
  - Hierarchical analog layout synthesizer capable of handling system level designs
  - Open-sourced

Fully Automated Layout Generation



- Core layout generation engine with MAGICAL
- Allow customizable inputs: symmetry constraints, placement net weighting, routing net sequence etc.

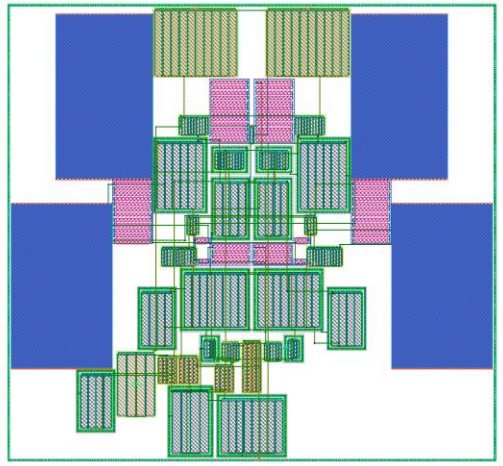
"MAGICAL: Toward Fully Automated Analog IC Layout Leveraging Human and Machine Intelligence," ICCAD'19

Fully Automated Layout Generation

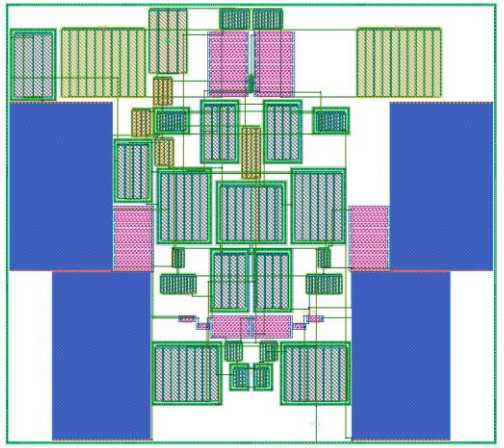
- Allow customizable inputs and tunable parameters
- Extended symmetric constraints for system designs
- Global placement parameters:
  - Net weighting for wirelength optimization
  - Area and wirelength trade-off parameter
- Routing considerations:
  - Net sequence in routing
  - Wire width and spacing

Fully Automated Layout Generation

- Allow customizable inputs and tunable parameters
- Parameters could lead to different layout implementations and significant differences in circuit performance
- E.g. Net weighting in wirelength optimization



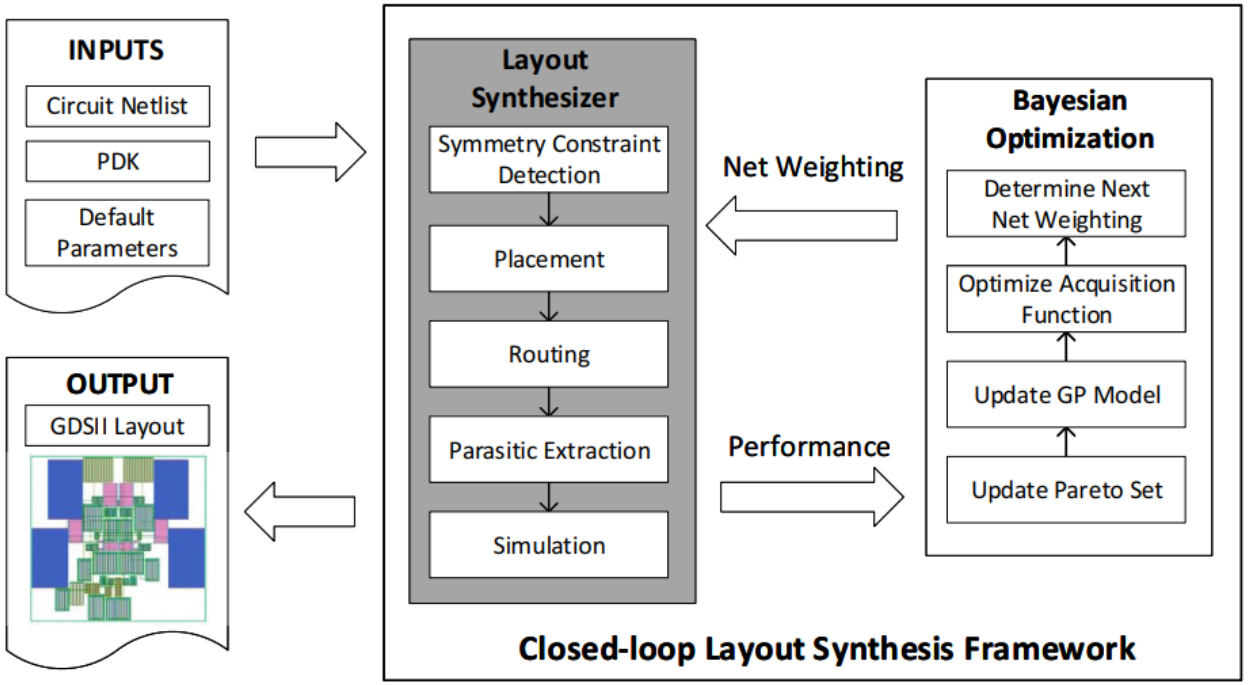
Offset (mV)	~ 0
CMRR (dB)	110



Offset （mV)	5.0
CMRR (dB)	76.3

Closed-loop Layout Synthesis

- Leverage simulation results
- Automated and efficient parameter tuning
- Multi-objective Bayesian optimization
  - Search for performance Pareto fonts
  - Flexible performance trade-offs by designer



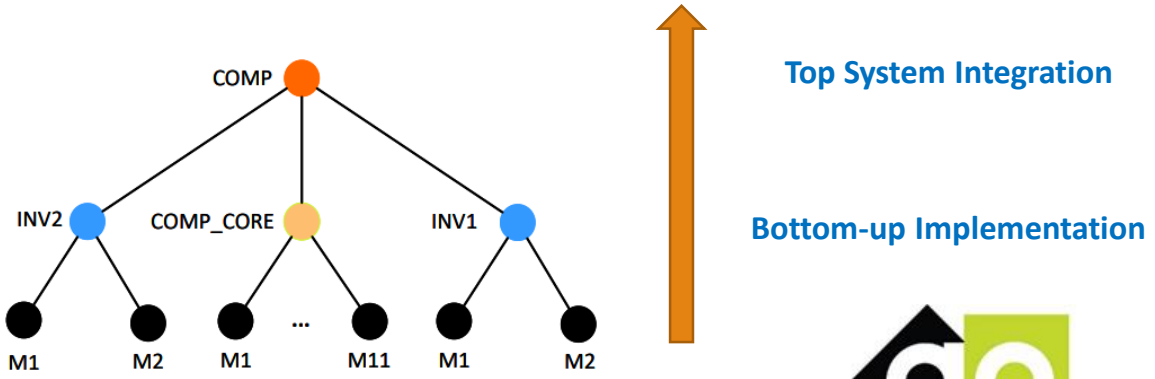
Hierarchical Design Methodology

- Extract design hierarchy from input netlist
- Bottom-up design implementation
  - Divide and conquer
  - Guarantee building block performance
  - System level integration
- Practical issues:
  - Long simulation time for system designs
  - Manual tune parameters for system integration

Input Netlist

```
subcircuit COMP_CORE
  ...
subcircuit INV
  ...
subcircuit COMP
  COMP_CORE  ... COMP_CORE
  INV1 ... INV
  INV2 ... INV
```

Extracted Design Hierarchy



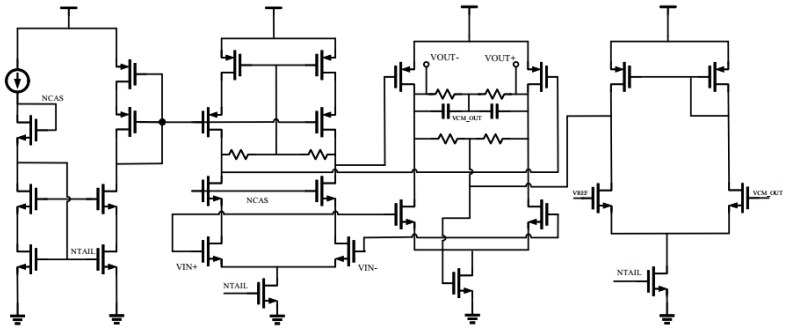
Runtime Comparison

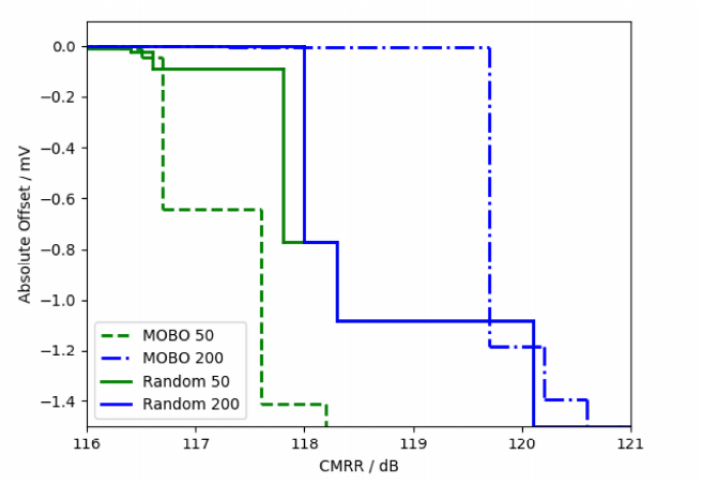
	Layout	Extraction	Simulation
Amplifier	18s	34s	26s
CTDSM	1m14s	41s	1h59m25s

Experimental Results

- Automated parameter tuning on amplifier design
- Offer performance guarantee
- Effective on layout centric performance

Amplifier Design





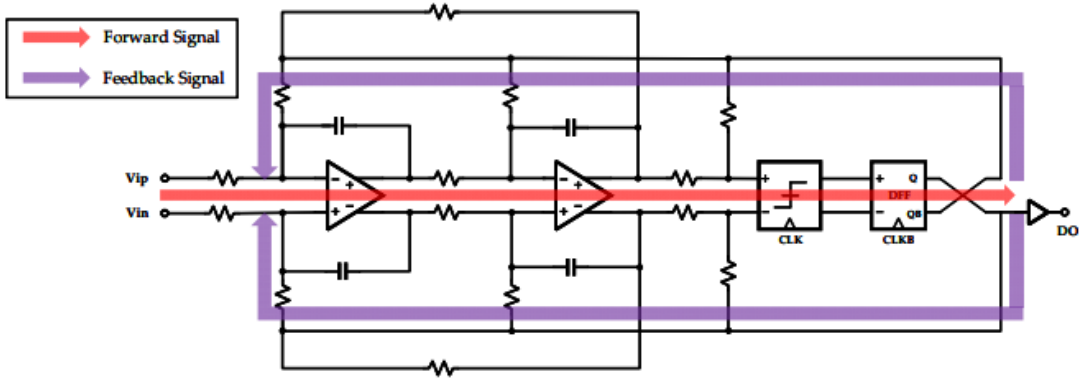
CMRR vs Offset

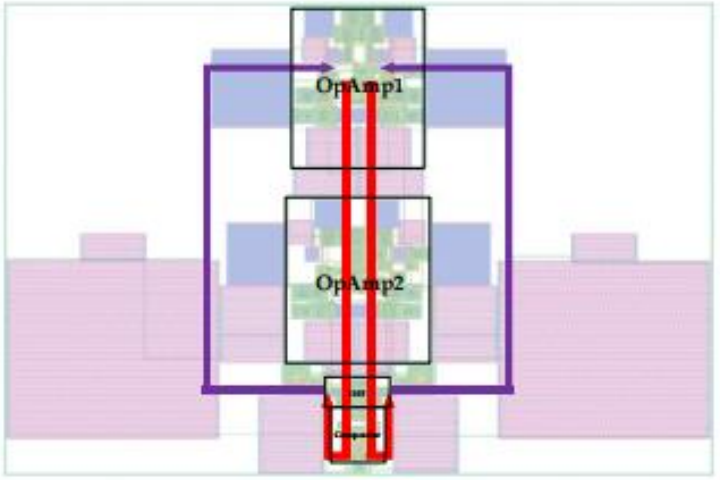
Performance Results

	Schematic	Optimized Layout	One-shot Layout
Gain (dB)	54.0	54.1	32.8
GBW (MHz)	487	344	335
Phase Margin	50.6°	67.7°	14.5°
CMRR (dB)	–	119.7	56.4
Offset (mV)	–	0.007	4.8

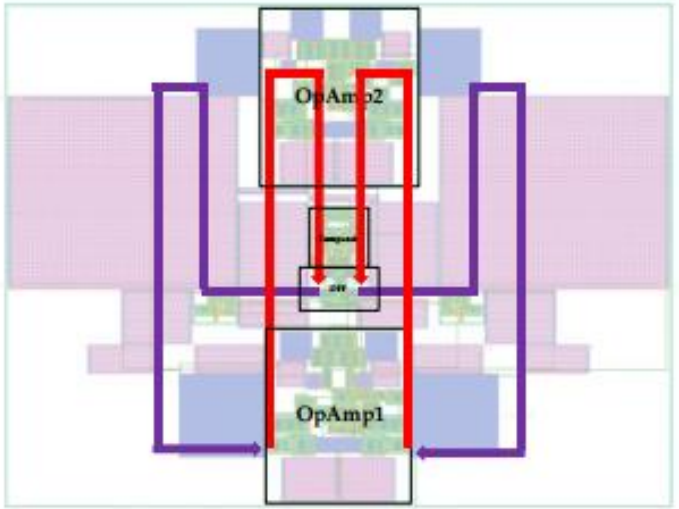
Experimental Results

2nd Order CTDSM Design





Regular signal flow



Irregular signal flow

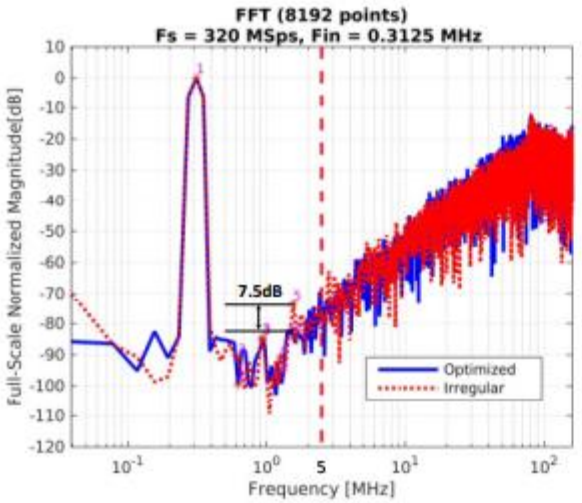
- Handling system level design:
  - 177 devices with 3 analog blocks
  - Optimize and guarantee building block performance with MOBO
  - Tune parameters to optimized regular “signal flow” through heuristics
- Considerations:
  - Upweight nets on forward signal path
  - Prioritize clock routing with increased net spacing to mitigate clock coupling

Experimental Results

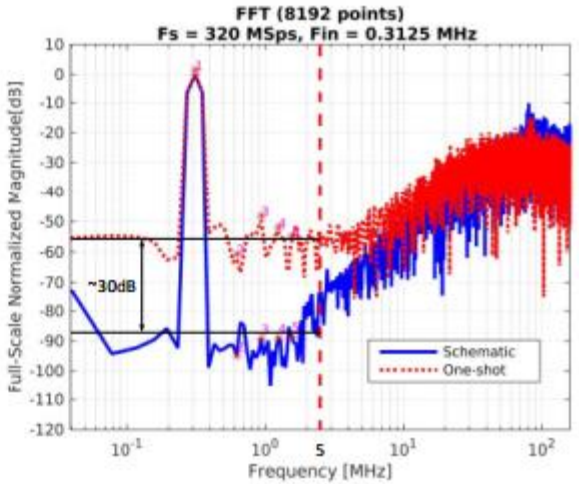
- Handling system level design:
  - Optimized layout achieves near schematic performance
  - Need to guarantee building block circuit performance

- Optimized: Manual tuning in system integration, automated synthesis in building blocks
- Irregular: Default parameter in system integration, automated synthesis in building blocks
- One-shot: Default parameters and no automated synthesis in building blocks

Simulated Spectrums



Optimized vs Irregular



Schematic vs One-shot

Performance Results

	Schematic	One-shot	Irregular	Optimized
Supply (V)	1.2			
F_s (MHz)	320			
BW (MHz)	5			
SNDR (dB)	67.8	39.6	65.2	65.9
SFDR (dB)	84.7	48.5	73.0	80.5
Power (mW)	0.84	0.91	0.86	0.86
Area (um^2)	–	8094	8188	9450

Conclusions

- **Performance-driven:** Utilize post layout simulation results
- **Automated**: Efficient parameter tuning with Bayesian optimization
- **Scalable**: Leverage design hierarchy for system level designs
- **Open-sourced**: ***https://github.com/magical-eda/MAGICAL***

Questions