Mingjie Liu

The University of Texas at Austin, Austin, TX, 78712
jay_liu@utexas.edu
https://jayl940712.github.io/

Education Information

Ph.D. in Electrical and Computer Engineering - The University of Texas at Austin

- In Progress

- VLSI CAD and Optimization A
- Integer Programming A

M.S. in Electrical and Computer Engineering - University of Michigan

- GPA: 4.0/4.0

- Machine Learning A+
- VLSI Design I A
- Computer Architecture A
- A/D Interfaces A

B.S. in Microelectronics - Peking University

- GPA: 89.8/100(cumulative) 91.7/100 (major)

Relevant Skills

- Hand on experience with machine learning platforms, such as TensorFlow and PyTorch
- Understanding of Bayesian optimization and reinforcement learning
- Understanding of EDA algorithms in placement and routing
- Experience with using commercial EDA software: digital and analog
- Knowledge of circuit analysis and signal processing
- Familiar with analog circuit and system designs, including data converters and PLLs

Work Experience

Research Assistant at UTDA, The University of Texas at Austin Sep 2018 - Present

- Analog layout design automation tool: MAGICAL
- Bayesian optimization assisted hierarchical analog layout generation
- Analog placement quality prediction with convolutional neural networks
- Graph heuristic algorithms for analog placement constraint generation
- Guided analog routing with generative neural networks

Research Intern, Nvidia Corporation June 2020 - Sep 2020

- Parasitic-aware transistor sizing with Bayesian optimization
- Layout parasitic prediction with graph neural networks

Design Engineer Intern, Micron Technology May 2017 - Aug 2017

- Output buffer design and delay optimization for critical logic paths

Course Projects

Multidisciplinary Design Project with Texas Instruments Sep 2017 - May 2018

- X-band radar front end design with state-of-the-art RF chips from TI
- Matched filter signal processing back end for improved SNR performance

Course Project for A/D Interfaces Jan 2018 - May 2018

- Third order continuous time ΔΣ ADC with chopping and FIR noise filtering

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Course Projects

Course Project for Computer Architecture — Jan 2017 – May 2017

- 64-bit P6 based 2-way superscalar RISC processor design in synthesizable Verilog

Course Project for VLSI Design I — Sep 2016 - Jan 2017

- 16-bit 300MHz fully custom designed RISC processor
- Custom designed 0.37V 8T SRAM with leakage compensation

Teaching Experience

- Graduate Teaching Assistant, The University of Texas at Austin — Fall 2018
  - EE 411 Circuit Theory
- Graduate Teaching Assistant, University of Michigan — Fall 2017
  - EECS 427 VLSI Design I

Scholarships and Awards

- The University of Texas Graduate School Fellowship — 2018
- Graduation of Honor: College Graduate Excellence Award of Beijing — 2016
- Fangzheng Scholarship — 2015
- Samsung Scholarship — 2014
- EECS Departmental Fellowship (No. 8508) — 2013

Publications

Mingjie Liu, Walker Turner, George Kokai, Brucek Khailany, David Z. Pan and Haoxing Ren, "Parasitic-Aware Analog Circuit Sizing with Graph Neural Networks and Bayesian Optimization," IEEE Design, Automation & Test in Europe (DATE) Conference, Feb. 1-5, 2021.

Mingjie Liu, Keren Zhu, Xiyuan Tang, Biying Xu, Wei Shi, Nan Sun and David Z. Pan, "Closing the Design Loop: Bayesian Optimization Assisted Hierarchical Analog Layout Synthesis," ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, July 19-23, 2020.

Mingjie Liu*, Keren Zhu*, Jiaqi Gu, Linxiao Shen, Xiyuan Tang, Nan Sun and David Z. Pan, " Towards Decrypting the Art of Analog Layout: Placement Quality Prediction via Transfer Learning, " IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE), Grenoble, France, Mar. 09-13, 2020

Mingjie Liu, Wuxi Li, Keren Zhu, Biying Xu, Yibo Lin, Linxiao Shen, Xiyuan Tang, Nan Sun and David Z. Pan, "S3DET: Detecting System Symmetry Constraints for Analog Circuits with Graph Similarity, " IEEE/ACM Asian and South Pacific Design Automation Conference (ASPDAC), Beijing, China, Jan. 13-16, 2020 (**Best Paper Nomination**)

Hao Chen*, **Mingjie Liu***, Xiyuan Tang*, Keren Zhu*, Nan Sun and David Z. Pan, "Challenges and Opportunities Toward Fully Automated Analog Layout Design," Journal of Semiconductors, 2020

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Publications

Hao Chen*, **Mingjie Liu***, Biying Xu*, Keren Zhu*, Xiyuan Tang, Shaolan Li, Yibo Lin, Nan Sun and David Z. Pan, "MAGICAL: An Open-Source Fully Automated Analog IC Layout System from Netlist to GDSII," IEEE Design & Test, 2020

Jiaqi Gu, Chenghao Feng, Zheng Zhao, Zhoufeng Ying, **Mingjie Liu**, Ray T. Chen and David Z. Pan, "SqueezeLight: Towards Scalable Optical Neural Networks with Multi-Operand Ring Resonators," IEEE Design, Automation & Test in Europe (DATE) Conference, Feb. 1-5, 2021.

Xiaohan Gao, Chenhui Deng, **Mingjie Liu**, Zhiru Zhang, David Z. Pan and Yibo Lin, "Layout Symmetry Annotation for Analog Circuits with Graph Neural Networks," IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Tokyo, Japan, Jan 18-21, 2021.

Jiaqi Gu, Zheng Zhao, Chenghao Feng, Zhoufeng Ying, **Mingjie Liu**, Ray T. Chen and David Z. Pan, "Towards Hardware-Efficient Optical Neural Networks: Beyond FFT Architecture via Joint Learnability," IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems (TCAD), September, 2020

Keren Zhu, **Mingjie Liu**, Hao Chen, Zheng Zhao and David Z. Pan, "Exploring Logic Optimizations with Reinforcement Learning and Graph Convolutional Network," ACM/IEEE Workshop on Machine Learning for CAD (MLCAD), November 16-20, 2020.

Hao Chen, Keren Zhu, **Mingjie Liu**, Xiyuan Tang, Nan Sun and David Z. Pan, "Toward Silicon-Proven Detailed Routing for Analog and Mixed-Signal Circuits," IEEE/ACM International Conference on Computer-Aided Design (ICCAD), November 02-05, 2020.

Keren Zhu, Hao Chen, **Mingjie Liu**, Xiyuan Tang, Nan Sun and David Z. Pan, "Effective Analog/Mixed-Signal Circuit Placement Considering System Signal Flow," IEEE/ACM International Conference on Computer-Aided Design (ICCAD), November 02-05, 2020.

Zixuan Jiang, Keren Zhu, **Mingjie Liu**, Jiaqi Gu and David Z. Pan, "An Efficient Training Framework for Reversible Neural Architectures," European Conference on Computer Vision (ECCV), Glasgow, United Kingdom, August 23-27, 2020.

Jiaqi Gu, Zheng Zhao, Chenghao Feng, **Mingjie Liu**, Ray T. Chen, David Z. Pan, "Towards Area-Efficient Optical Neural Networks: An FFT-based Architecture, " IEEE/ACM Asian and South Pacific Design Automation Conference (ASPDAC), Beijing, China, Jan. 13-16, 2020 (**Best Paper Award**)

Keren Zhu, **Mingjie Liu**, Yibo Lin, Biying Xu, Shaolan Li, Xiyuan Tang, Nan Sun and David Z. Pan, "GeniusRoute: A New Analog Routing Paradigm Using Generative Neural Network Guidance, " IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Westminster, CO, Nov. 4-7, 2019

Biying Xu, Keren Zhu, **Mingjie Liu**, Yibo Lin, Shaolan Li, Xiyuan Tang, Nan Sun and David Z. Pan, "MAGICAL: Toward Fully Automated Analog IC Layout Leveraging Human and Machine Intelligence " IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Westminster, CO, Nov. 4-7, 2019 **(Invited Paper)**