DESIGN, AUTOMATION & TEST IN EUROPE
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Parasitic-Aware Analog Circuit Sizing with Graph Neural Networks and Bayesian Optimization

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Outline

- Background and Prior Work
- Parasitic Prediction with Machine Learning
- Parasitic-Aware Sizing with Bayesian Optimization
  - Improved Surrogate Modeling
  - Uncertainty Estimates with Dropouts
- Experimental Results
- Conclusions

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- **Background and Prior Work**
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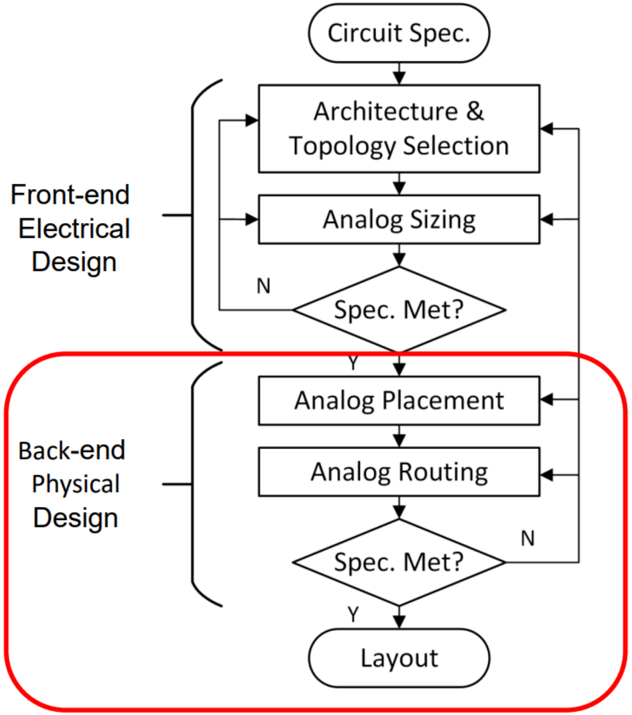
Background and Prior Work

- **Analog design still heavily manual**
  - **Large degree of freedom**
  - **Design specific performance**
- **Iterative optimization between schematic sizing and layout**
  - **Estimate parasitic to avoid "surprises"**
  - **Critical parasitic effect performance**
- **Parasitic becomes difficult to estimate**



Background and Prior Work

- **Numerous methods for automated sizing**
  - **Model first, then optimize**
  - **Model free black-box optimization**
  - **Sample efficient black-box optimization**

Better Model Fidelity
Better Sample Efficiency

- **Parasitic-aware sizing**
  - **Generate layout in optimization loop**
  - **Estimate parasitic after placement**

Rajan et al. DATE’04, Habel et al. TCAD’11
Hakhamaneshi et al ICCAD’19, Settaluri et al. DATE’20

Lourenco et al. DATE’15

- **Require some-level of layout generation**

Background and Prior Work

- **In this work:**
  - **Parasitic-aware sizing framework based on Bayesian optimization**
  - **Replace in-the-loop layout generation with Graph Neural Network (GNN) based parasitic prediction**
  - **Better performance surrogate model with parasitic features**
  - **Leverage dropout as an efficient uncertainty prediction**
  - **Improved runtime and optimization convergence**

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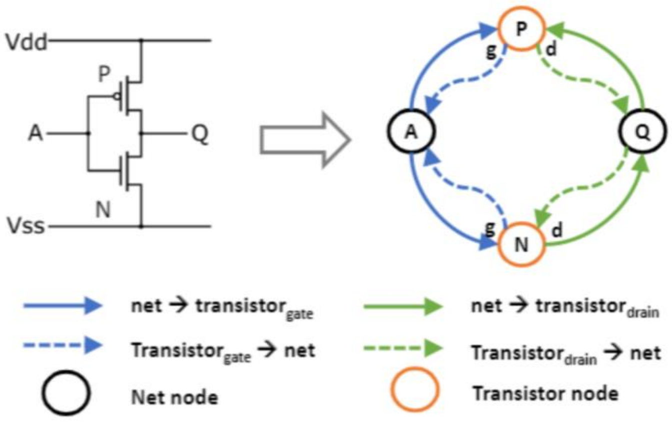
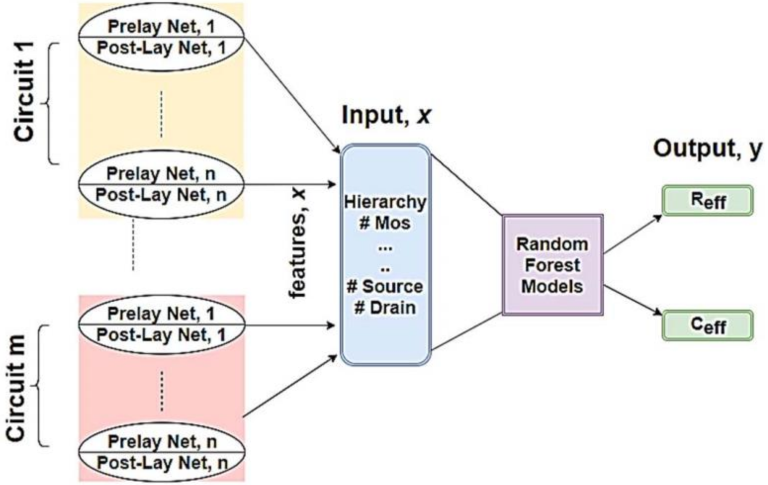
Parasitic Prediction with Machine Learning

- **Predicting layout parasitic directly from schematic**
  - **Graph neural networks (ParaGraph)**
  - **Random forests (MLParest)**



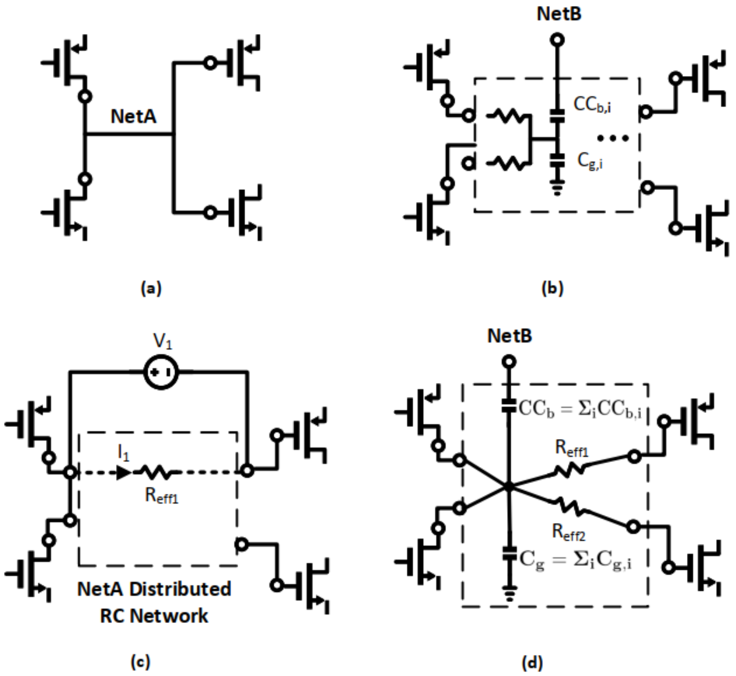
ParaGraph: Ren et al. DAC'20



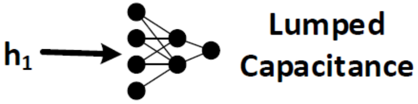
MLParest: Shook et al. DAC'20

Parasitic Prediction with Machine Learning

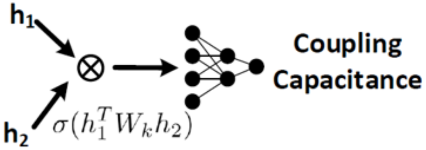
- **Our work extend ParaGraph:** Ren et al. DAC'20
  - C only → R+C+CC
- **R+C+CC data labeling**
  - Effective resistance from DC simulations
  - Lump to C and CC



- **C prediction**



- **R/CC prediction**



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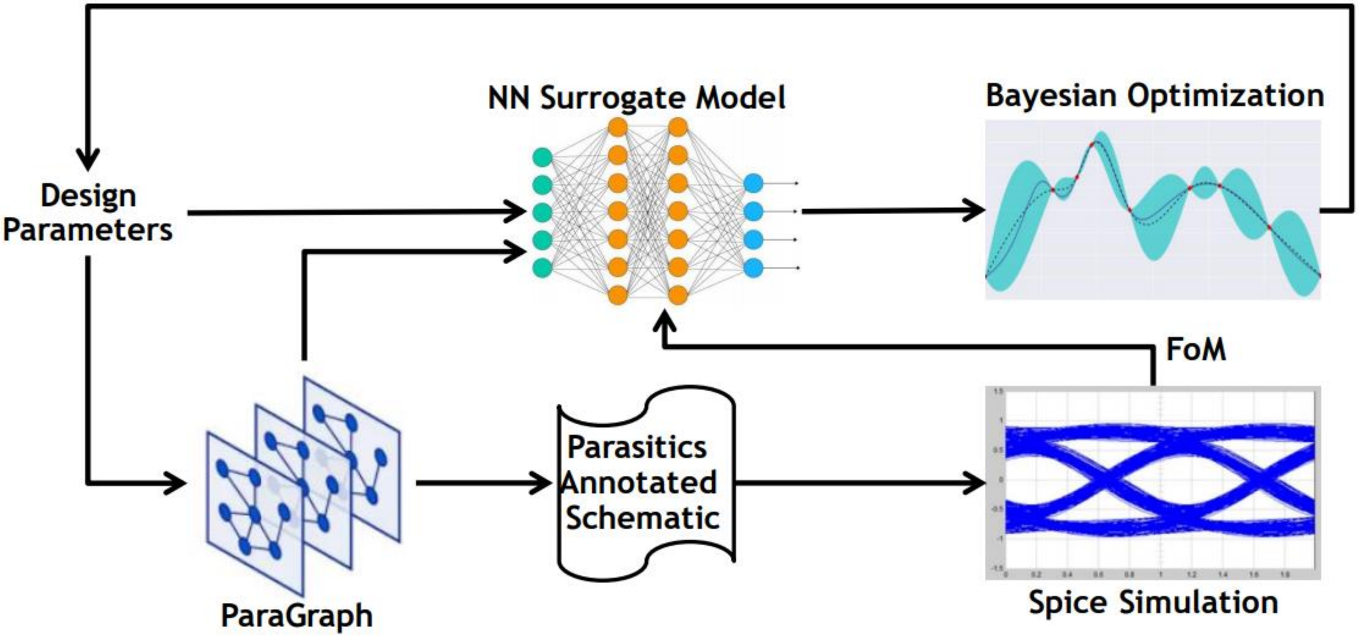
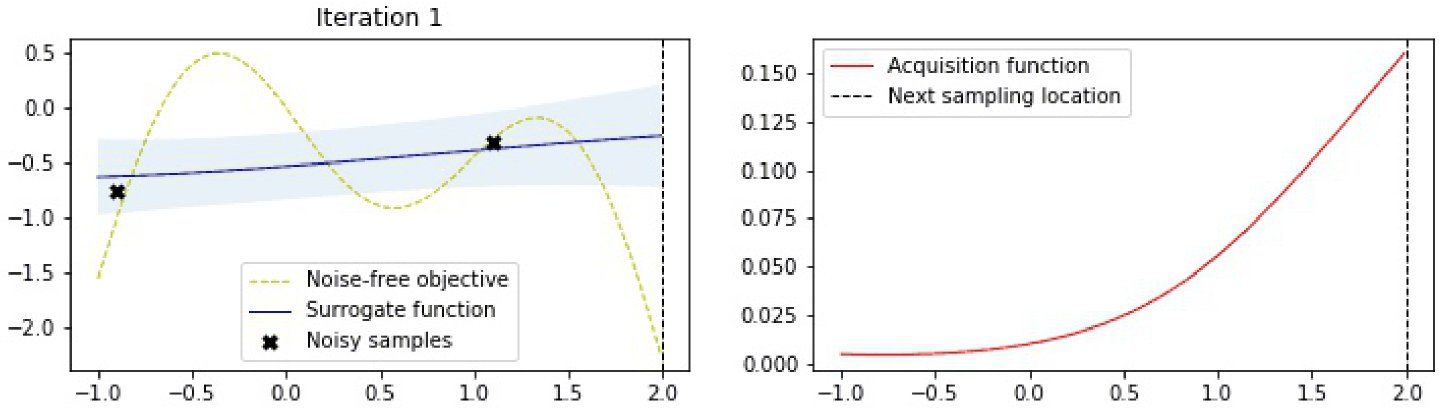
Parasitic-Aware Sizing with Bayesian Optimization



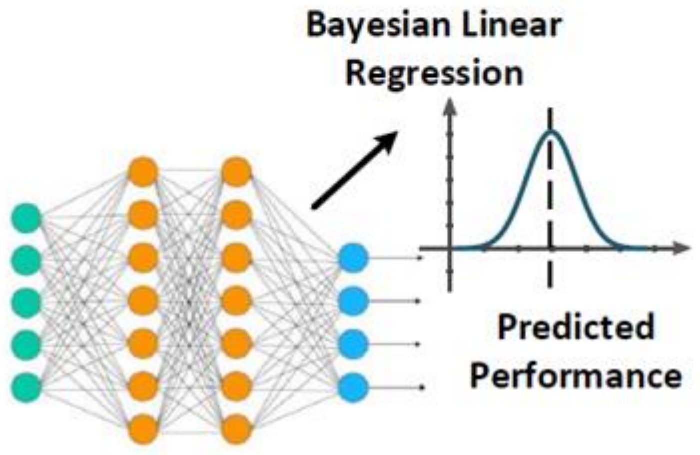
Bayesian Optimization

- **Problem formulation: constrained single-objective**
- **Bayesian optimization**
  - **Gaussian process regression: predict both mean and uncertainty**
  - **Acquisition function: determine where next to evaluate (balance exploration and exploitation)**



Improved Surrogate Modeling

- Gaussian Process Regression
  - Non-parametric probabilistic model
  - Poor scalability $O(N^3)$ training
- Scalable Bayesian Optimization
  - Neural networks as trainable kernel function
  - Replace FC layer with Bayesian linear regression (BLR)
  - Better scalability $O(N)$ training



Snoek et al. PMLR’15, Zhang et al. DATE’19

Improved Surrogate Modeling

- **Use neural networks**
  - **For scalability**
  - **Additional parasitic features from ParaGraph**
- **Method:**
  - **ParaGraph is pre-trained with abundant data**
  - **Circuit graph is fixed, node input attributes (contains sizing) change**
  - **Obtain node embedding matrix** $H = \{h_1 \cdots h_n\} \in \mathbb{R}^{n \times d}$
  - **Get graph embedding**
    - **Average:**

$$g = \frac{1}{n} \sum_i^n h_i$$

Weighted:

$$z_i = \sigma(w^T h_i)$$

$$w_i = softmax(z_i) = \frac{exp(z_i)}{\sum_1^n exp(z_i)}$$

$$g = \frac{1}{n} \sum_1^n w_i \cdot h_i,$$

Improved Surrogate Modeling

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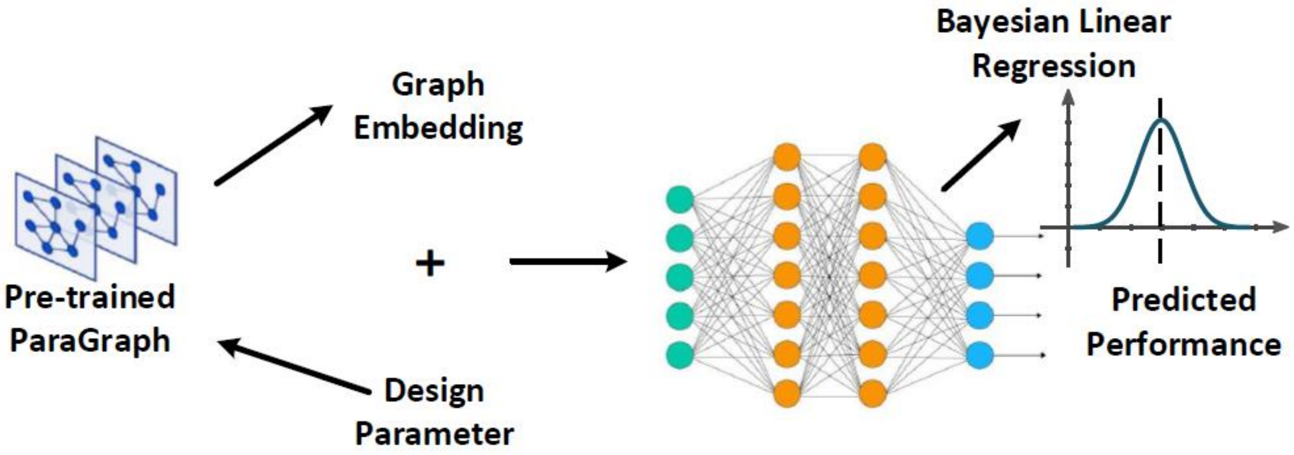

Uncertainty Estimates with Dropout

- **Replace BLR with dropouts:**
  - **Train model with dropout**
  - **Retain model in training mode and batch inference**
  - **Obtain statistical mean and variance (uncertainty)**
- **Pros: Easy to implement and works!**
- **Cons: Difficult to obtain gradients of acquisition function**
- **Solution: Maximize acquisition function with non-gradient methods (particle swarm optimization)**
- **More details in paper.**

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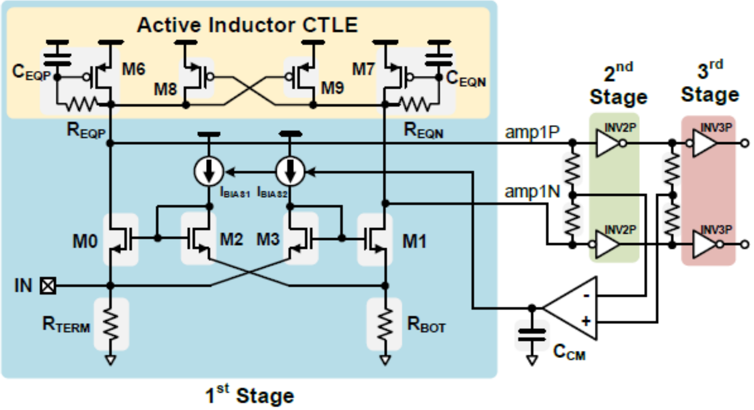

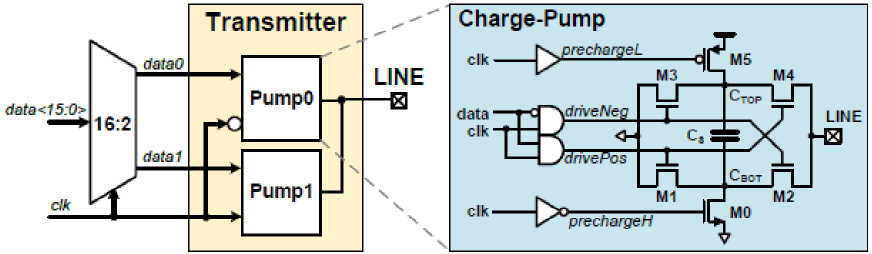

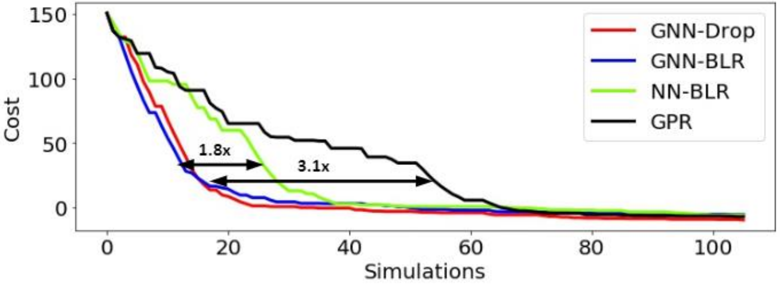

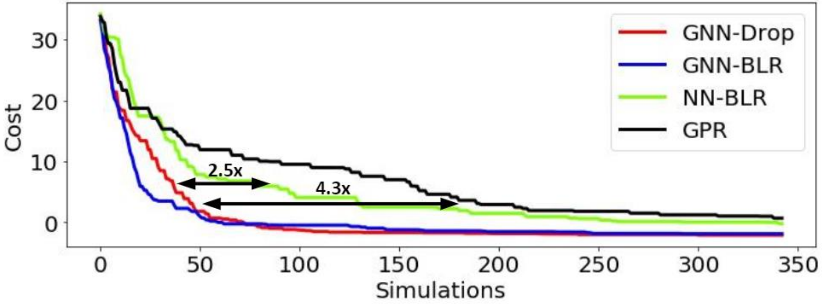

Experimental Results

- **Extended C+CC parasitic estimation reduces simulation errors by 41.3% compared with C only model**
- **Improved surrogate performance model outperforms Gaussian process regression (GPR) by more than 20%**
- **Our method improves convergence by 2.1x speedup compared with NN-BLR and 3.7x speedup compared with GPR**
- **More details in the paper**

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Conclusions

- **Conclusions:**
  - **Parasitic-aware sizing without layout generation**
  - **Extend parasitic estimation to R+C+CC**
  - **Improved surrogate model with parasitic graph embedding**
  - **Leverage dropouts for uncertainty prediction with Bayesian optimization**

Thank You