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Effective Analog/Mixed-Signal Circuit Placement Considering System Signal Flow

Keren Zhu, Hao Chen, Mingjie Liu, Xiyuan Tang, Nan Sun and David Z. Pan
ECE Department
The University of Texas at Austin
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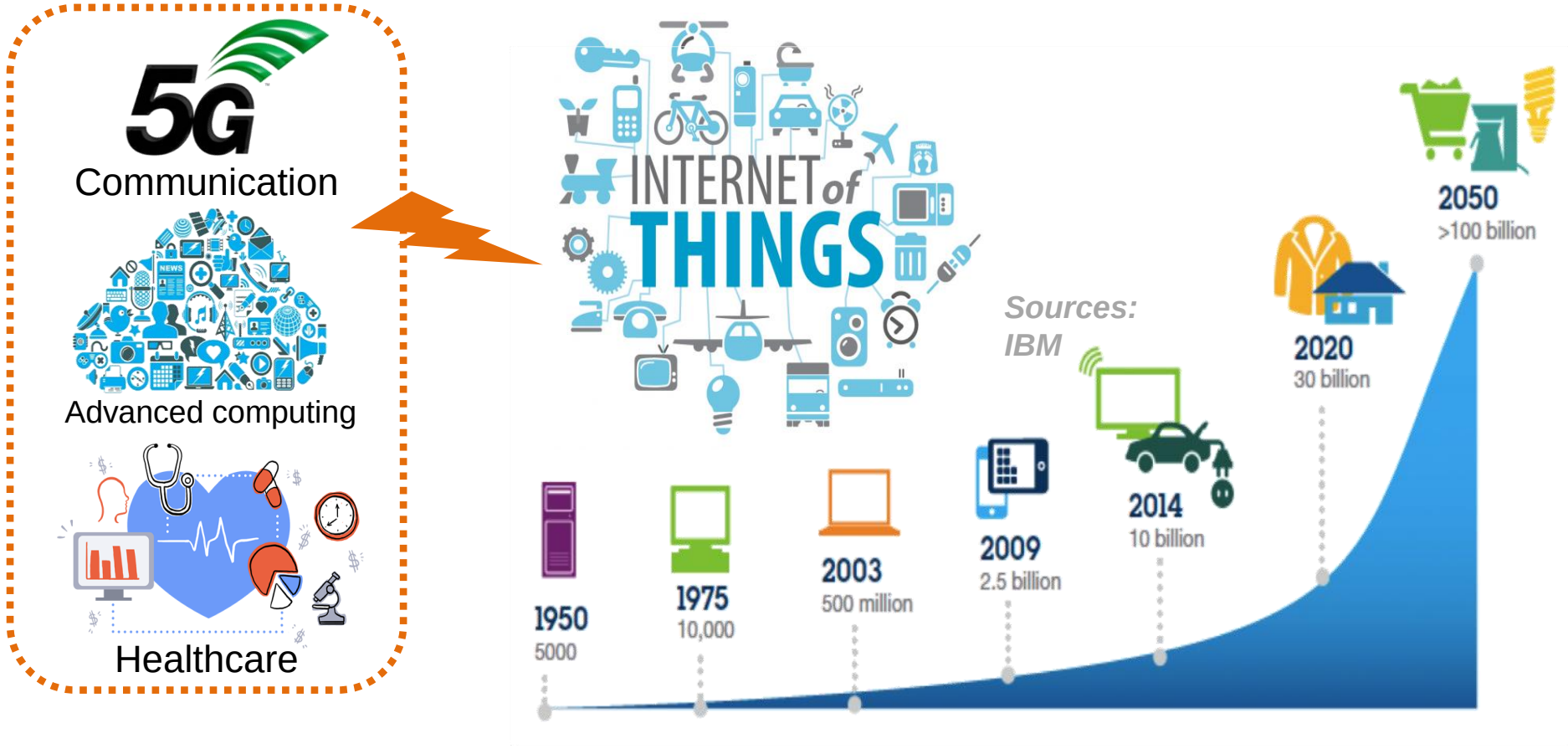
Speaker – Keren Zhu

- Keren Zhu is a Ph.D. student at ECE Department at UT Austin under supervision of Prof. David Z. Pan.
- Keren Zhu's research interests include general topics in VLSI physical design with a focus on analog layout automation.

Background: Automating AMS Layouts

- There are high demand for analog and mixed signal (AMS) circuits
- Drawing AMS layouts are still manual and cost time

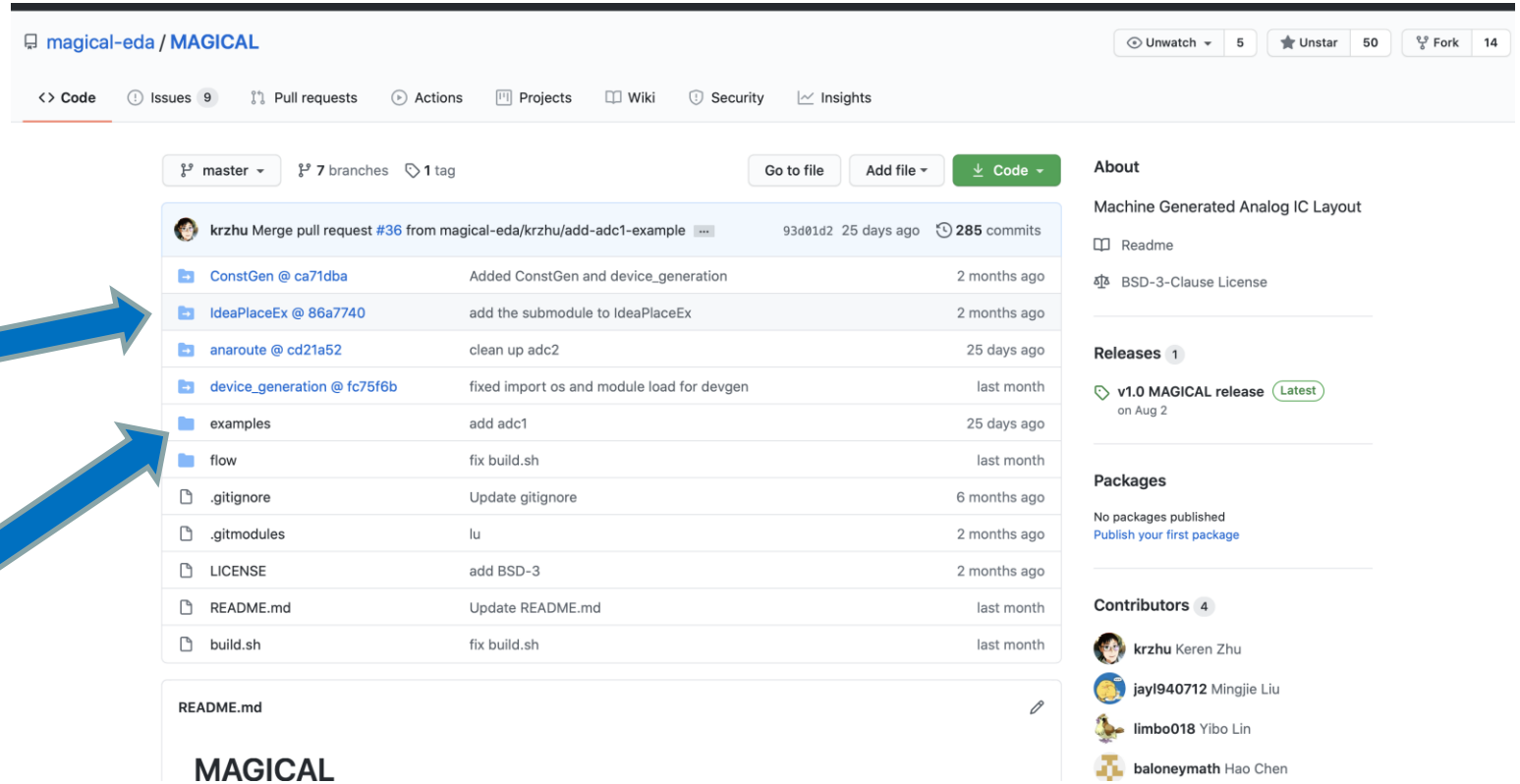


Background: MAGICAL

- This work is part of MAGICAL https://github.com/magical-eda/MAGICAL
- Machine Generated Analog IC Layout

Placer codes

Benchmark netlists
(sanitized)

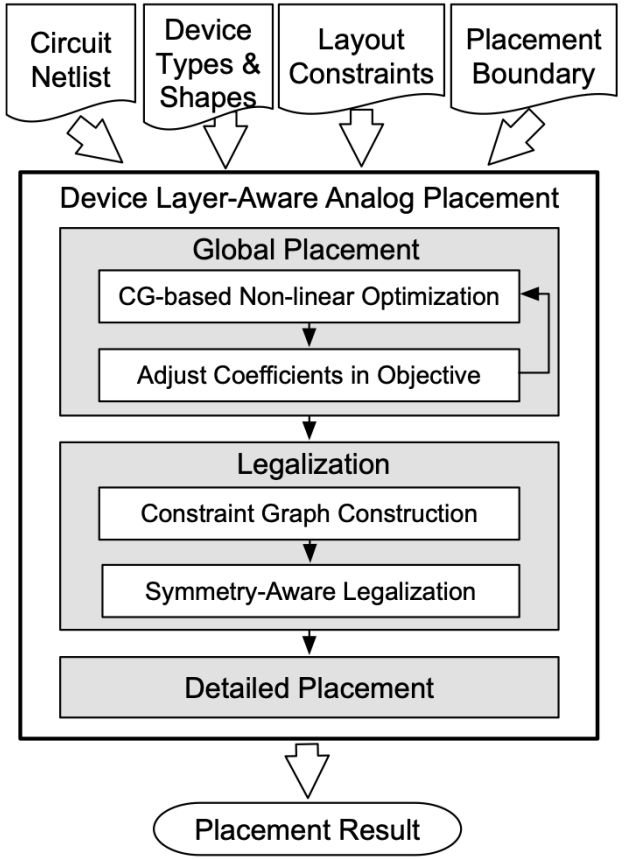


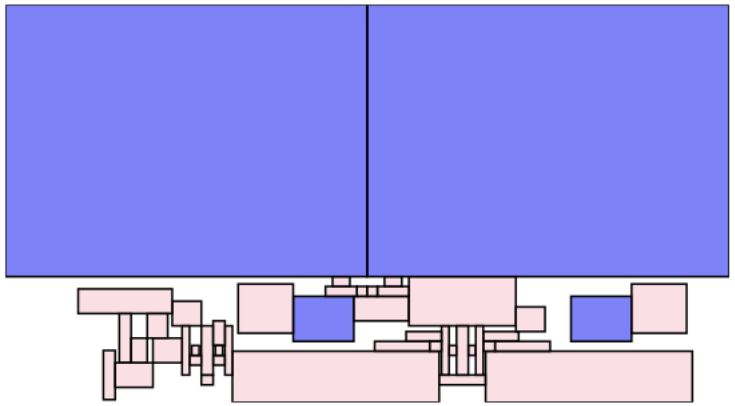
DARPA

Motivation: placer v1

Placer v1. [Xu+ ISPD19]

- First version of MAGICAL placer prototype
- Abstracted problem formulation
- Not really consider performance yet
- NLP+LP





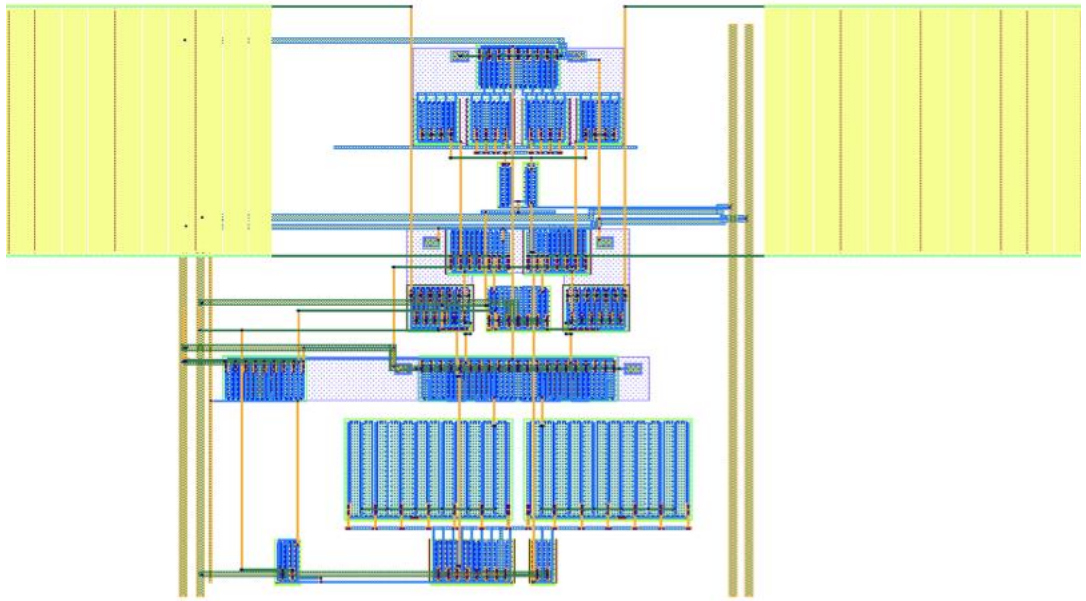
B. Xu, S. Li, C.-W. Pui, D. Liu, L. Shen, Y. Lin, N, Sun and D. Z. Pan, "Device Layer-Aware Analytical Placement for Analog Circuits," ISPD'19

Motivation: router v1

Placer v1. [Xu+ ISPD19]

Router v1. [Zhu+ ICCAD20]

- First version of MAGICAL router
- LVS correct
- Start working on optimizing performance with simulation results
- OTA/Comparator benchmarks



K. Zhu, M. Liu, Y. Lin, B. Xu, S. Li, X. Tang, N. Sun and D. Z. Pan, "GeniusRoute: A New Routing Paradigm using Generative Neural Network," ICCAD'19

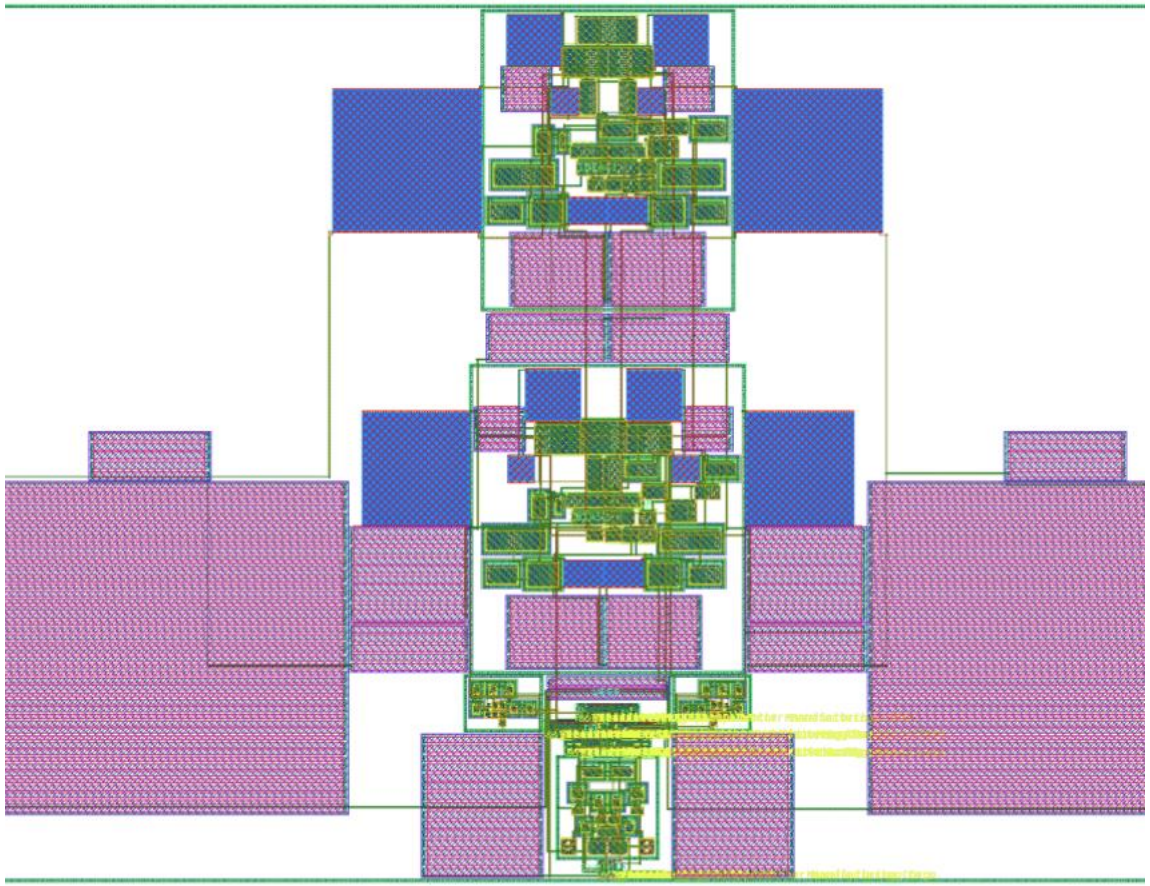
Motivation: hierarchical flow

Placer v1. [Xu+ ISPD19]

Router v1. [Zhu+ ICCAD19]

Hierarchical flow [Liu+ DAC20]

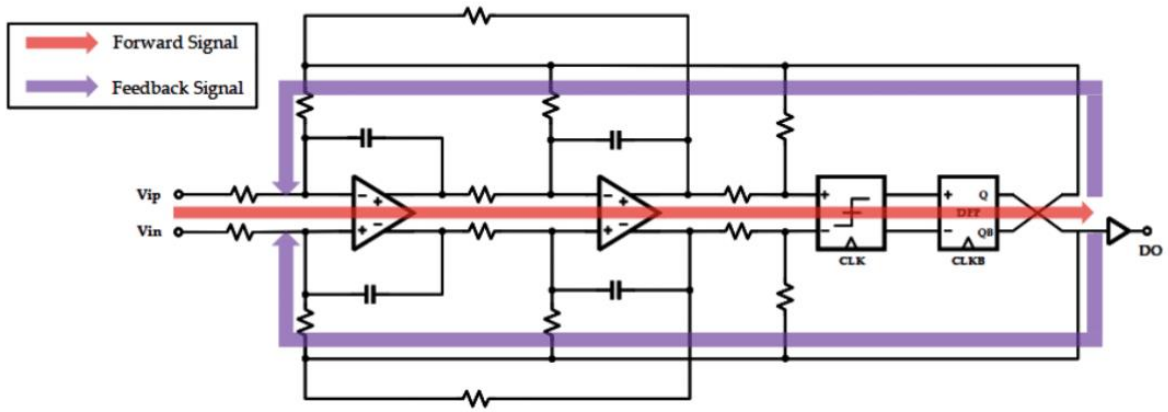
- MAGICAL start working on ADC
- Automatically tuning parameters for building block-level performance
- Manual tuning on top-level placement

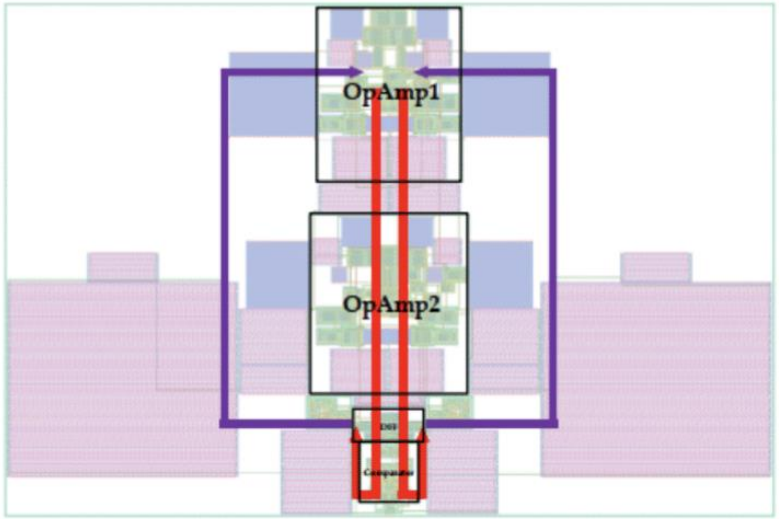


M. Liu, K. Zhu, X. Tang, B. Xu, W. Shi, N. Sun and D. Z. Pan, ”Closing the Design Loop: Bayesian Optimization Assited Hierarchical Analog Layout Synthesis," DAC’20

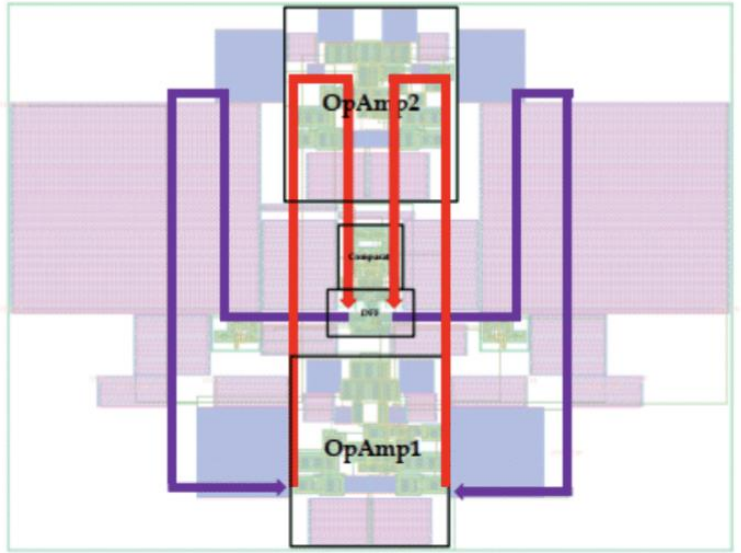
Problem 1: system signal flow

- Manual tuned in DAC20





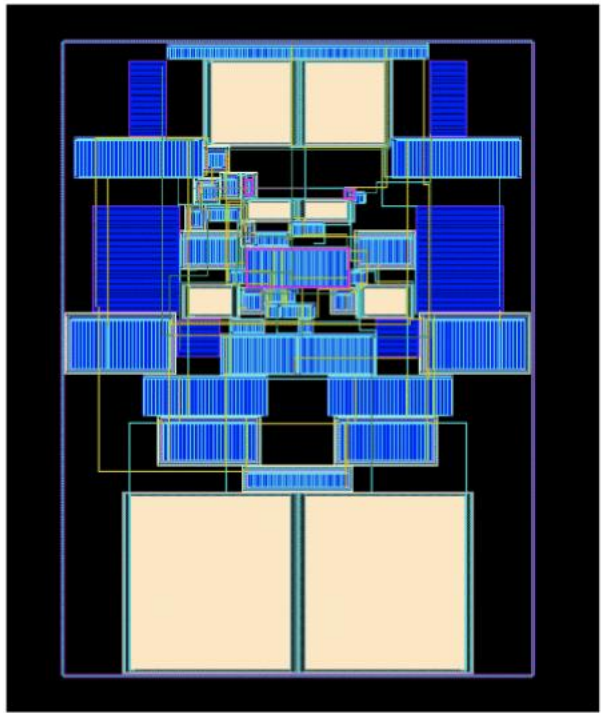
Optimized signal flow



Irregular signal flow (Default parameters)

Problem 2: sensitive building block performance

- Placer is not robust
  - Sensitive to the initial condition and parameters
  - Good results need some luck
  - Numerical optimization need to be improved
- IR drop is an issue
  - Placer should consider more in planning power routing

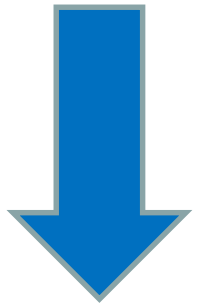


Motivation: placer v2

Placer v1 [Xu+ ISPD19]

Router v1 [Zhu+ ICCAD19]

Hierarchical flow [Liu+ DAC20]



Placer v2 [Zhu+ ICCAD20]
This work

Motivation: router v2

Placer v1 [Xu+ ISPD19]

Router v1 [Zhu+ ICCAD19]

Hierarchical flow [Liu+ DAC20]

Placer v2 [Zhu+ ICCAD20]
This work

Router v2 [Chen+ ICCAD20]

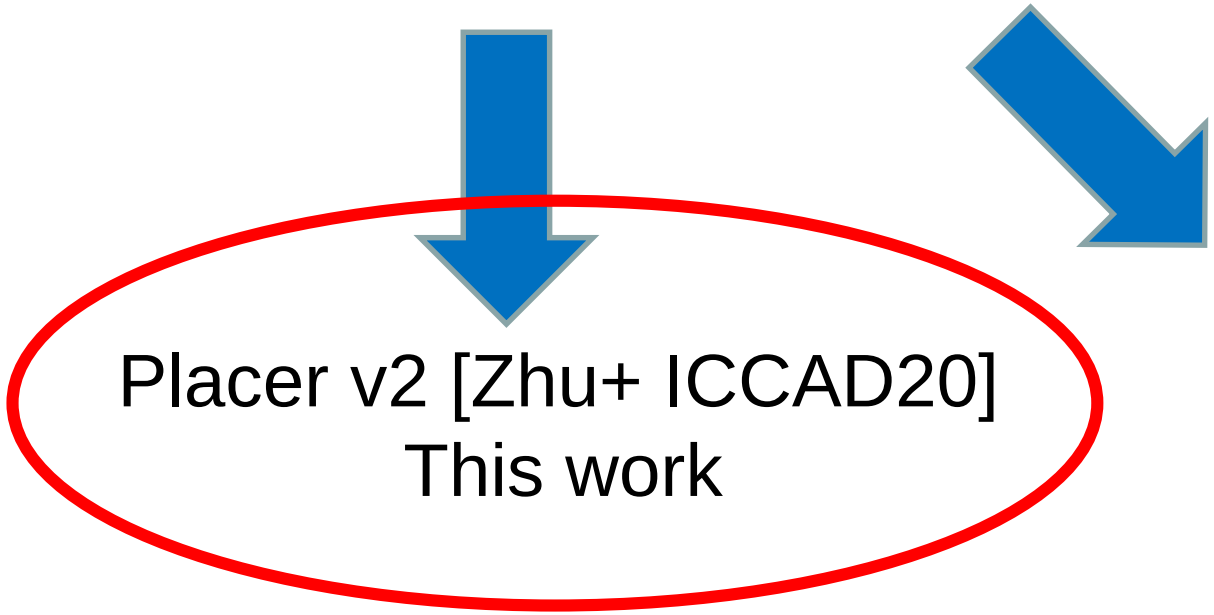
2A.3 Toward Silicon-Proven Detailed Routing for Analog and Mixed-Signal Circuits

Motivation: router v2

Placer v1 [Xu+ ISPD19]

Router v1 [Zhu+ ICCAD19]

Hierarchical flow [Liu+ DAC20]



Placer v2 [Zhu+ ICCAD20]
This work

Router v2 [Chen+ ICCAD20]

2A.3 Toward Silicon-Proven Detailed Routing for Analog and Mixed-Signal Circuits

Placer v2 contributions in high-level view

- Magical placer v2 has:

New Power Net WL model

New System Signal Flow Cost

Self-adaptive multiplier updates

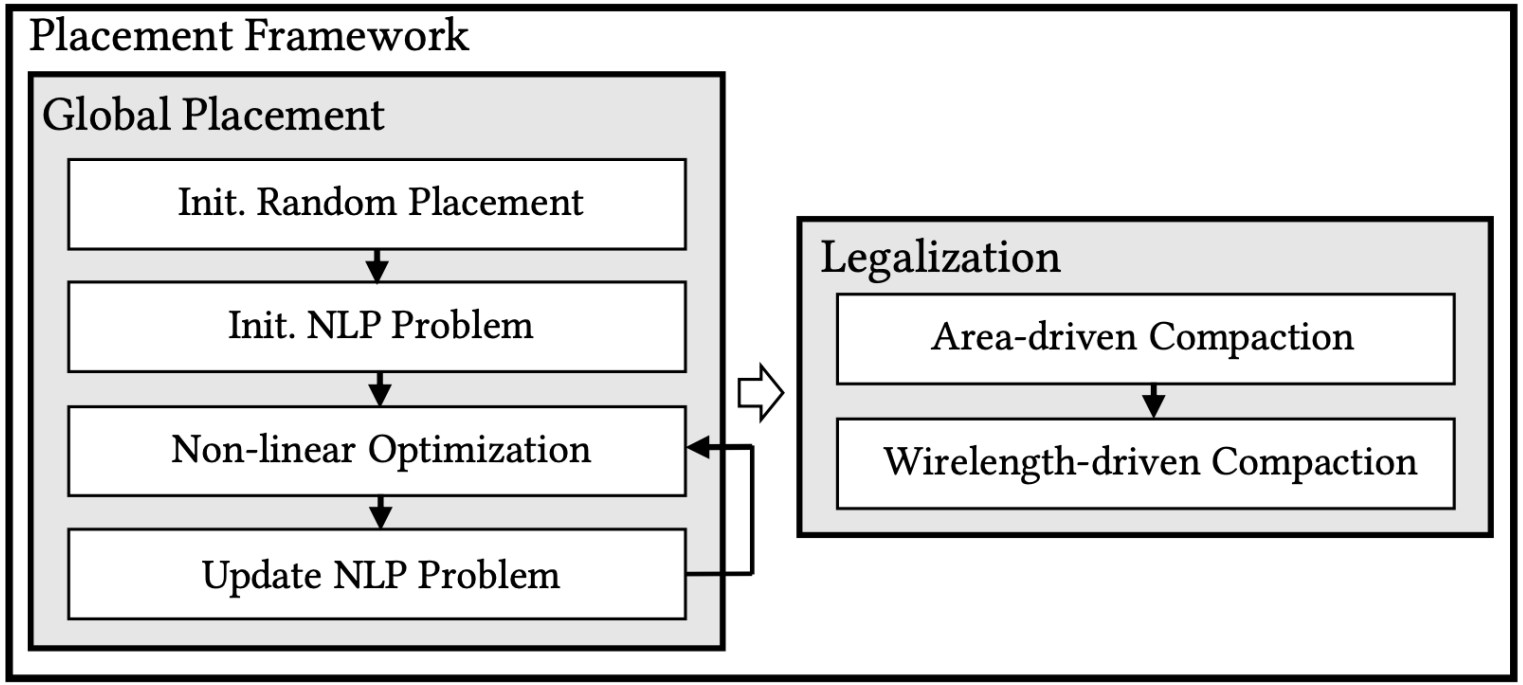
Gradient-based NLP optimization

Building Block Level

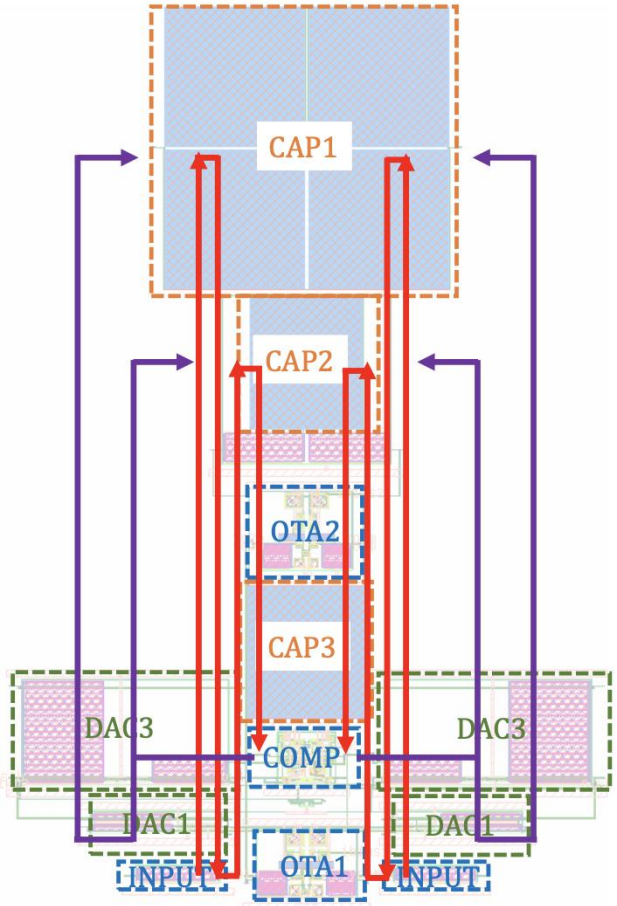
System Level

Placer v2 flow

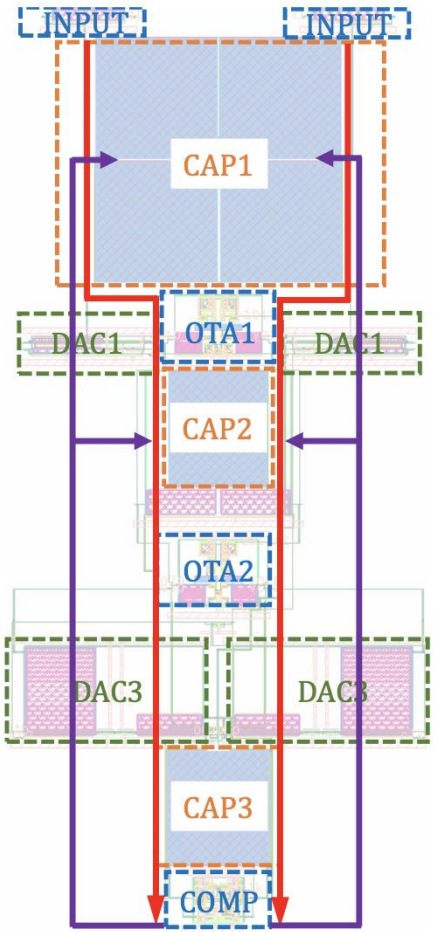
- Global placement decides the rough locations of each blocks
  - Iterative numerically solve non-linear optimization problem
  - Increase penalty multipliers for overlapping, etc. in each iteration
- Legalization ensure spacing and symmetry
  - Constraint graph + Linear programming

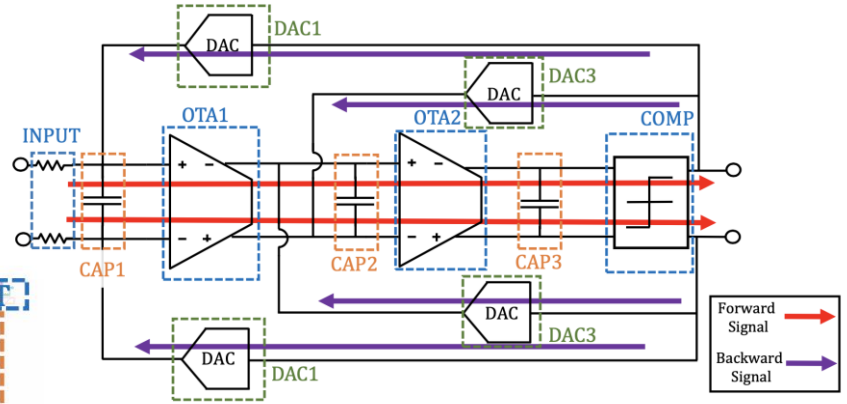


System signal flow cost formulation

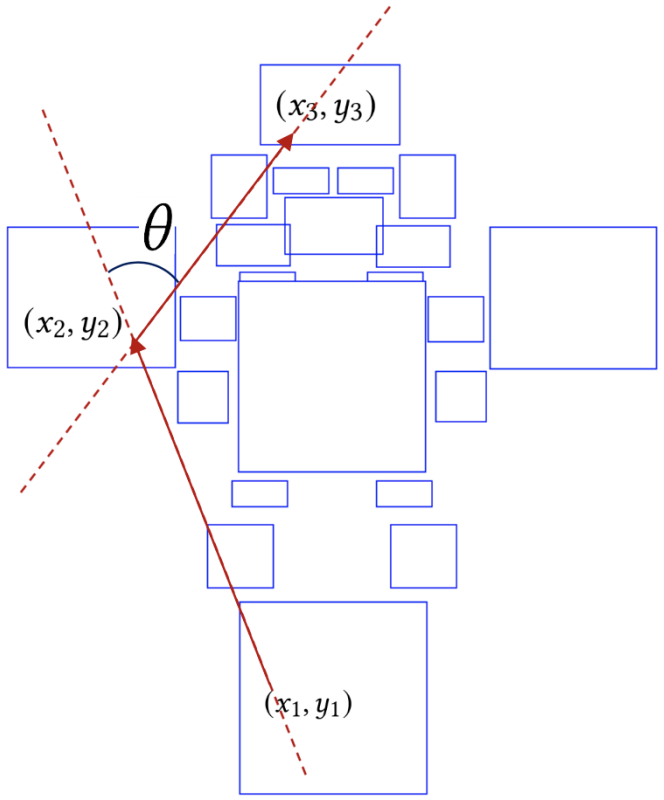


Want straight signal flow





System signal flow cost formulation



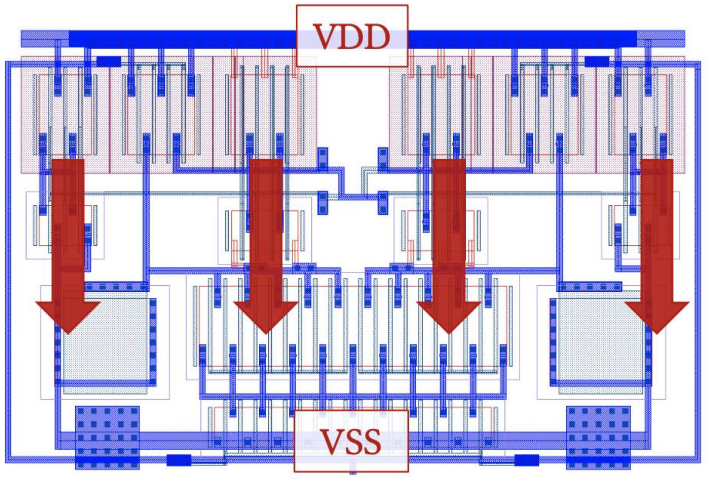
Minimize the angle θ

$$1 - \cos(\theta) = 1 - \frac{\vec{\mathbf{v}}_{i,j} \cdot \vec{\mathbf{v}}_{j,k}}{\left\|\vec{\mathbf{v}}_{i,j}\right\| \cdot \left\|\vec{\mathbf{v}}_{j,k}\right\|},$$

$$\vec{\mathbf{v}}_{i,j} = \begin{pmatrix} x_j - x_i \\ y_j - y_i \end{pmatrix}.$$

Fit more accurate power WL model

Disclaimer: this WL model is targeting for MAGICAL router v2



Pin-to-stripe power routing

$$O_i^{CRF} = \sum_{k=1}^{k \le |\mathcal{P}_i^{CRF}|-1} \max(y^*_{i,k+1} - y^*_{i,k}, 0),$$

Better multiplier updating scheme

- For better numerical robustness
- Matching initial gradient norm
  - Encourage comparable efforts to different costs

$$\lambda^{(0)} = \min\left(\frac{\left\|\nabla_{x,y} f^{SWL(0)}\right\|}{\left\|\nabla_{x,y} f / \Phi^{(0)}\right\|}, \lambda_{MAX}\right),$$

Use WL as common reference

- Subgradient method to increase penalty

$$\lambda^{(t)} = \lambda^{(t-1)} + \eta \cdot \Phi^{(t)}$$

Increase penalty based on how much is the violations

Gradient-based optimization

Algorithm 2 Optimization Kernel

$m_0 \leftarrow 0$
$v_0 \leftarrow 0$
$t \leftarrow 0$
while (x, y) not converged **do**
  $t \leftarrow t + 1$
  if $t \leq t_{GD}$ **then**
    $g_t \leftarrow \nabla f(x, y)$
    $m_t \leftarrow \beta_1 \cdot m_{t-1} + (1 - \beta_1) \cdot g_t$
    $v_t \leftarrow \beta_2 \cdot v_{t-1} + (1 - \beta_2) \cdot g_t^2$
    $\widehat{m}_t \leftarrow m_t / (1 - \beta_1^t)$
    $\widehat{v}_t \leftarrow v_t / (1 - \beta_2^t)$
    $(x, y) \leftarrow (x, y) - \alpha \cdot \widehat{m}_t / (\sqrt{\widehat{v}_t} + \epsilon)$
  else
    $(x, y) \leftarrow (x, y) - \delta \cdot \nabla f(x, y)$

Disclaimer: not well tuned. Adam with lower step size itself might also works

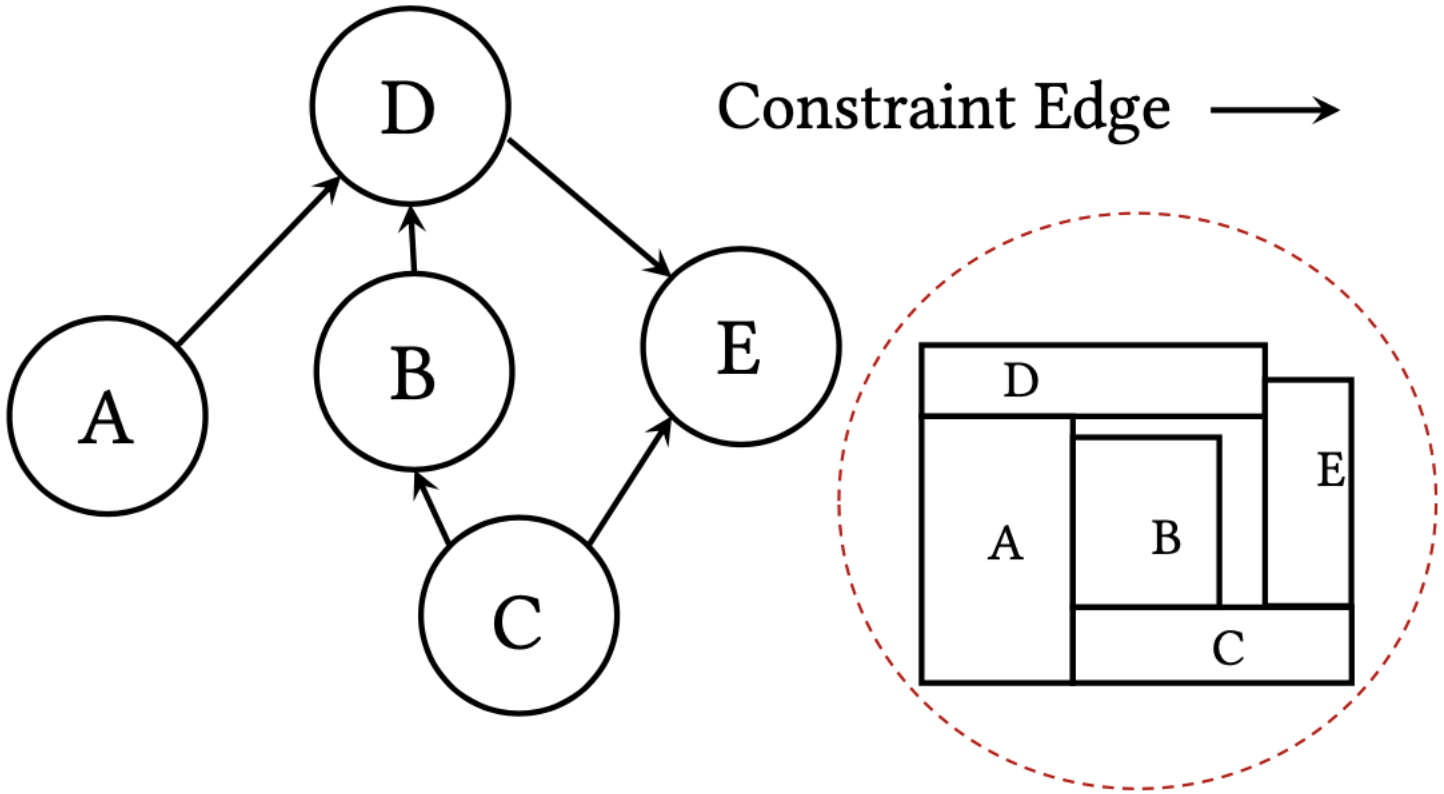
How to update multipliers is in general more important than optimization kernels

Adam optimizer for general cases

Vanilla gradient descant when convergence is slow

Legalization

- Generate a relational constraints and use linear programming to solve the compaction
- Similar to [Xu+ ISPD'19]



Experimental results on two ADCs

- System signal flow boosts the performance for two CTDSM ADCs

Circuits		Schematic	Without SSF	With SSF
ADC1	SNDR (dB)	66.2	61.4	63.6
	SFDR (dB)	76.9	75.0	77.1
	THD (dB)	75.0	70.6	73.8
	ENOB (bits)	10.70	9.90	10.27
	Power (mW)	0.837	0.864	0.870
ADC2	SNDR (dB)	67.1	59.6	66.3
	SFDR (dB)	82.0	67.0	80.2
	THD (dB)	77.6	66.5	76.4
	ENOB (bits)	10.85	9.61	10.71
	Power (mW)	0.677	0.740	0.757

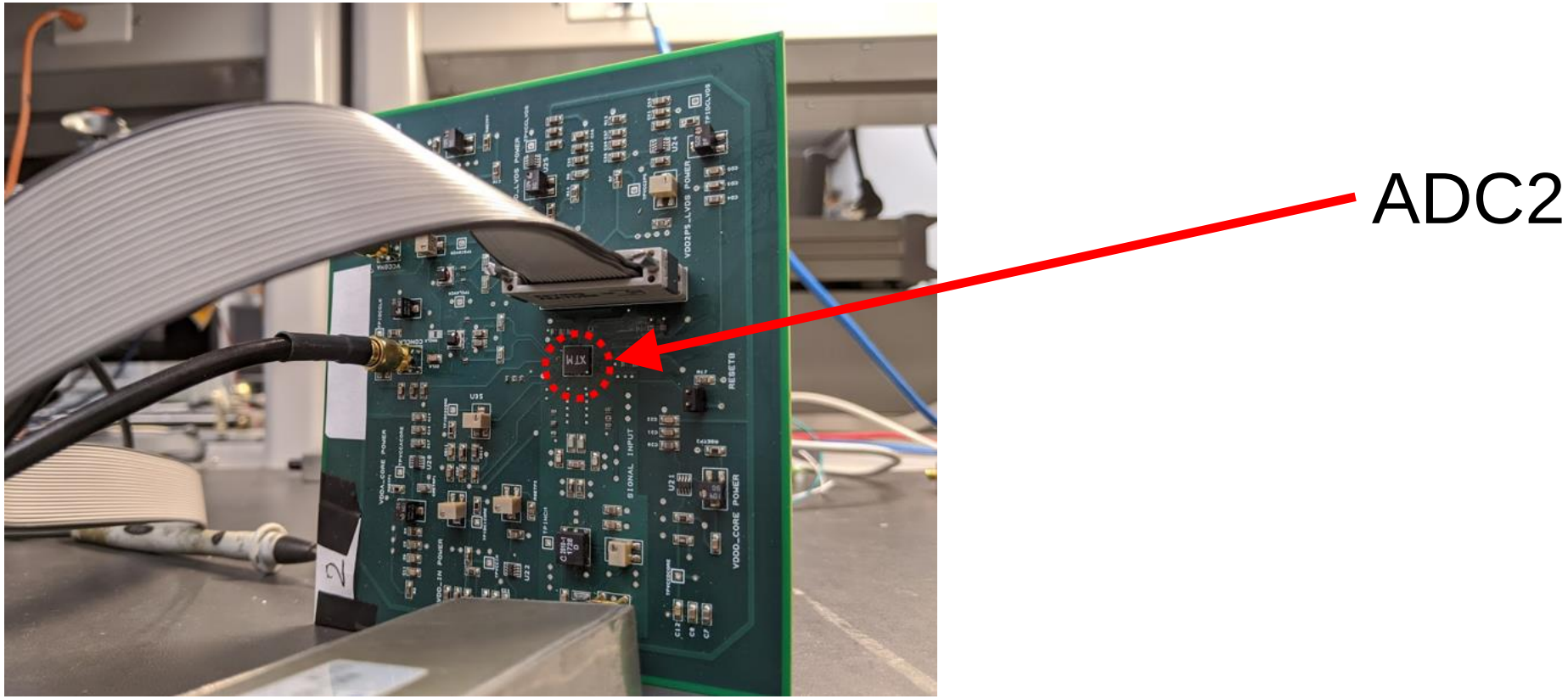
Experimental results on block-level circuits

- Outperform [Xu+ ISPD19] in both
  - WL and area
  - More details in the paper

CKTs	ISPD' 19				This Work			
	Area	HPWL	RWL	VIA	Area	HPWL	RWL	VIA
COMP	223	104	267	21	187	101	196	13
OP1	2366	767	1234	97	1584	691	905	84
OP2	2529	416	914	44	2047	466	732	50

The ADC2 chip

- The ADC2 core using the proposed placer has been taped-out and verified in measurements



Conclusion

- System signal flow is effective for two CTDSM-ADCs
  - Confirm with designers that this is a general approach for a broader range of circuit classes
- Better numerical optimization is effective in NLP global placement
- Fitting WL model to the target model is effective
  - Important for nets with special routing strategy

- Future works:
  - Placement and routing techniques for specific circuit classes
  - Advance technology nodes
    - E.g. FinFET technology