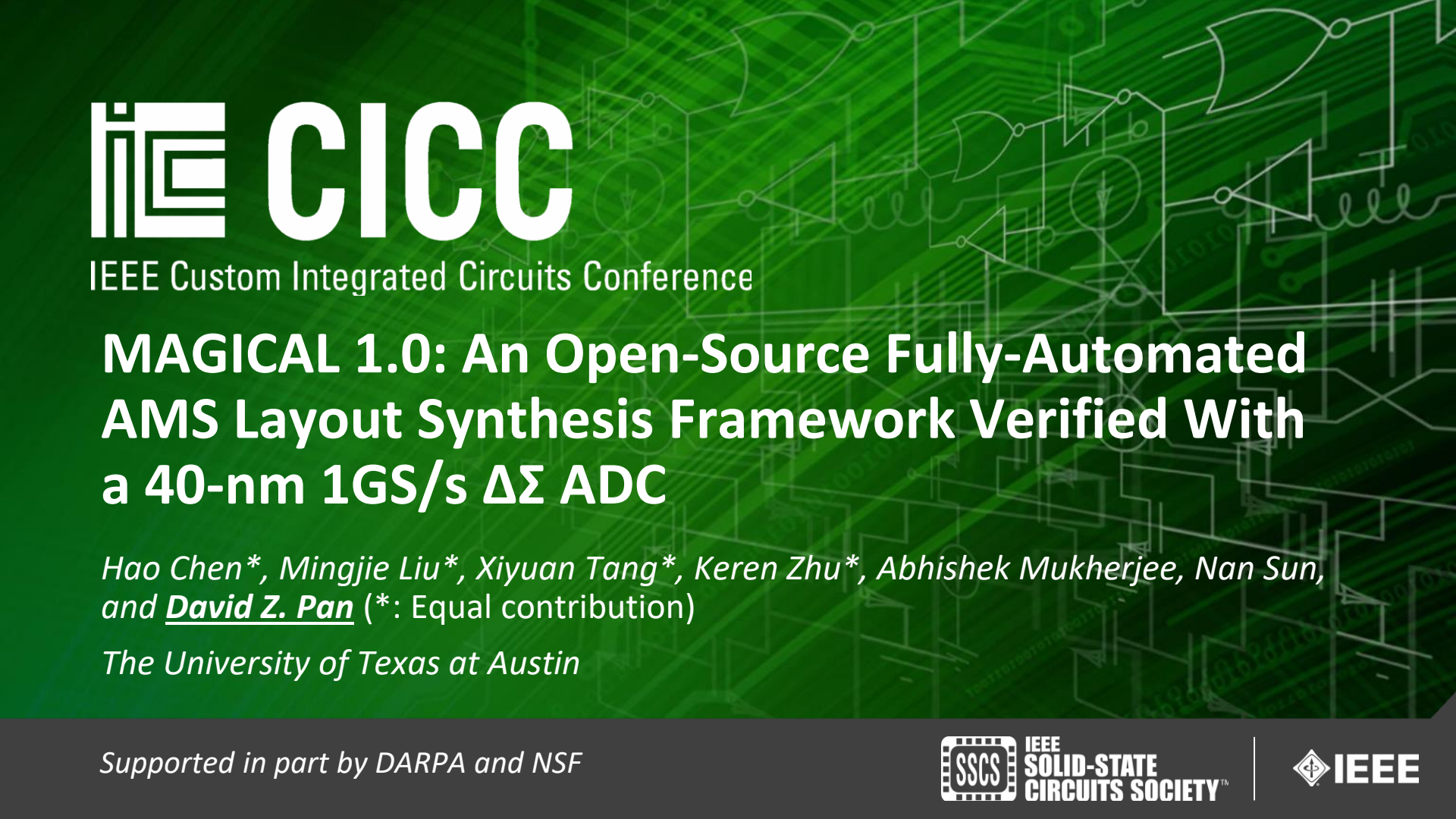


# MAGICAL 1.0: An Open-Source Fully-Automated AMS Layout Synthesis Framework Verified With a 40-nm 1GS/s ΔΣ ADC

*Hao Chen*, Mingjie Liu*, Xiyuan Tang*, Keren Zhu*, Abhishek Mukherjee, Nan Sun, and* ***David Z. Pan*** (*: Equal contribution)

*The University of Texas at Austin*

*Supported in part by DARPA and NSF*

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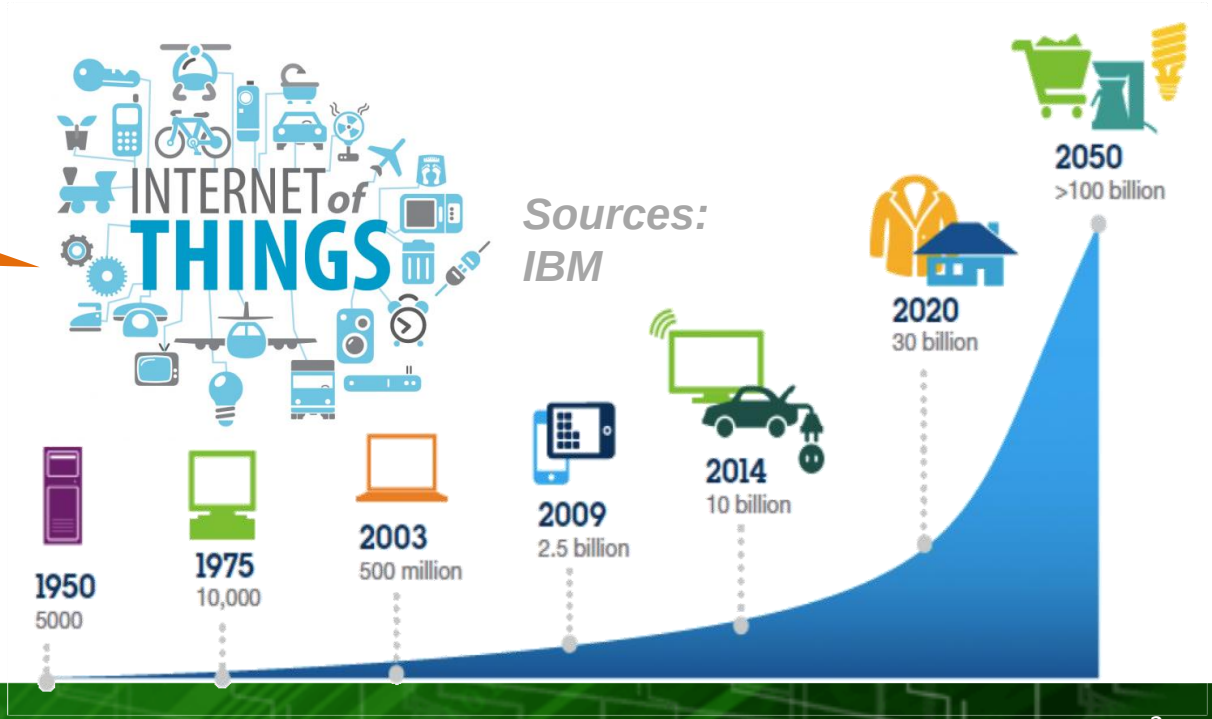
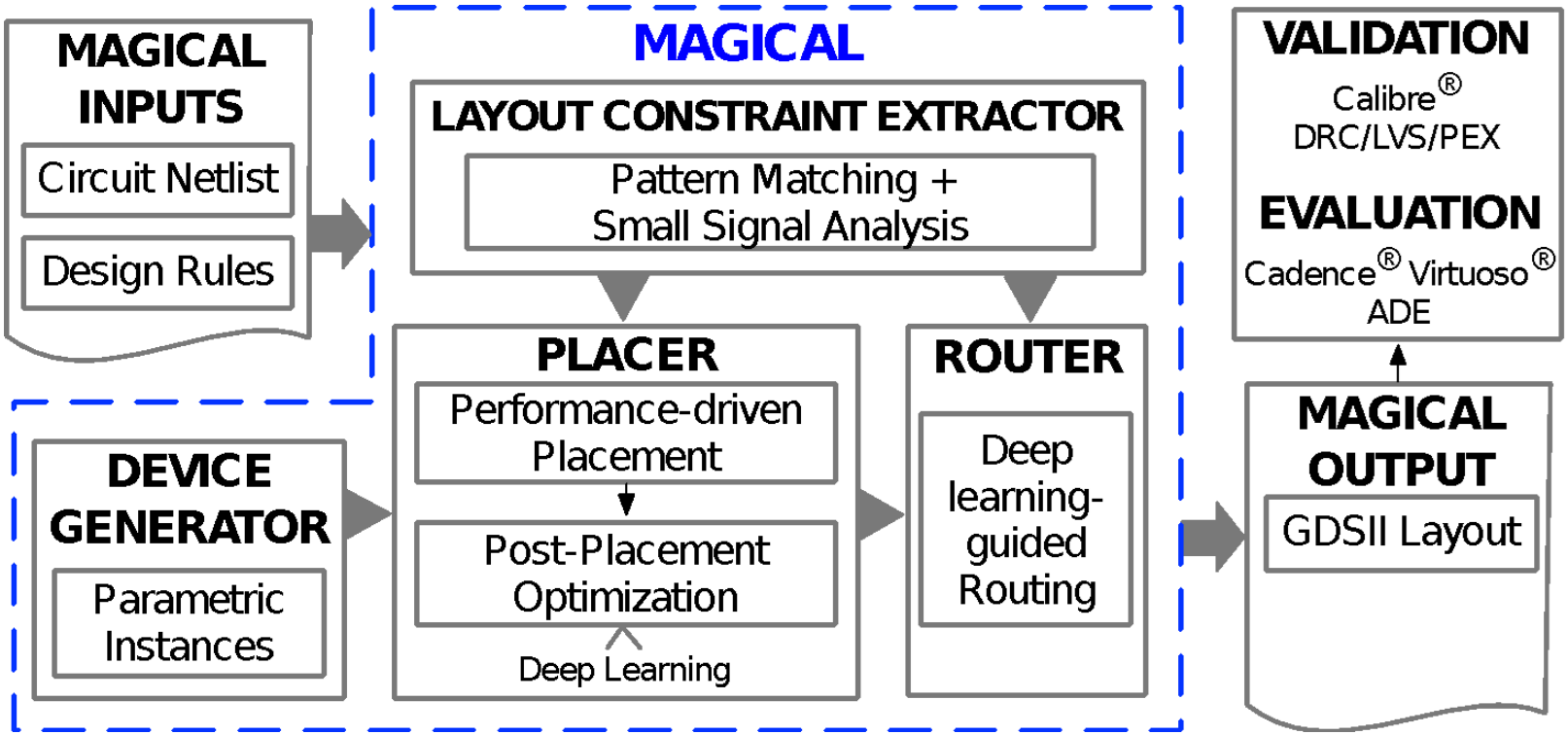
# Analog IC Design and Layout

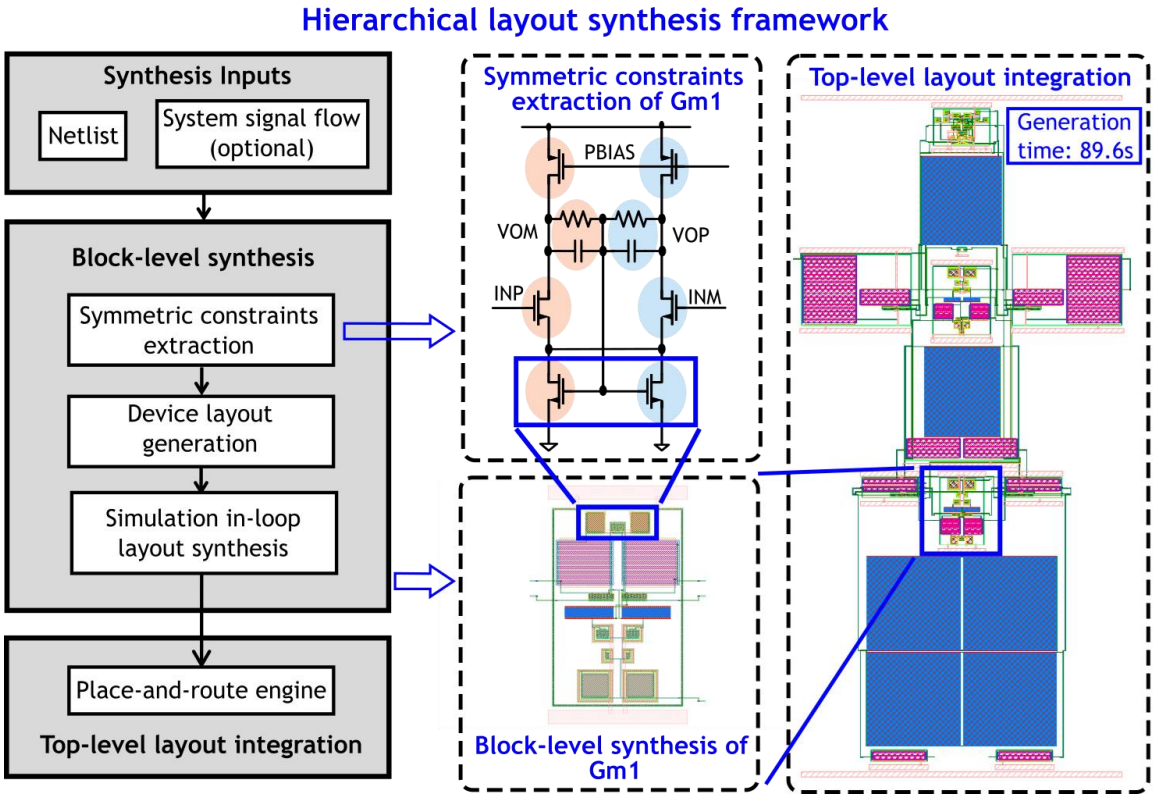
- High demand of analog/mixed-signal IC in emerging applications
  - Internet of Things (IoT), autonomous vehicles, 5G, wearable, sensors, …
  - X However, still mostly manually designed ➔ 20% or less analog in SOC may take 80% design time!

# MAGICAL: MAchine Generated IC Analog Layout

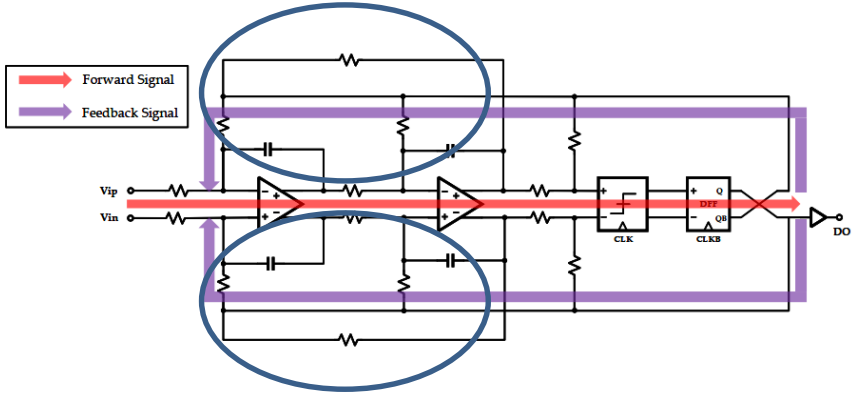


# MAGICAL 1.0: Hierarchical Framework

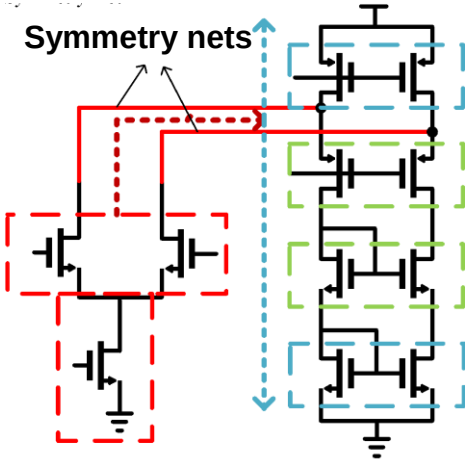


# MAGICAL 1.0: Constraint Generation

- Pattern detection for building block symmetry [Xu+, ICCAD'19]
- Graph similarity for system symmetry constraint [Liu+, ASPDAC'20]
- Customizable signal-flow constraints



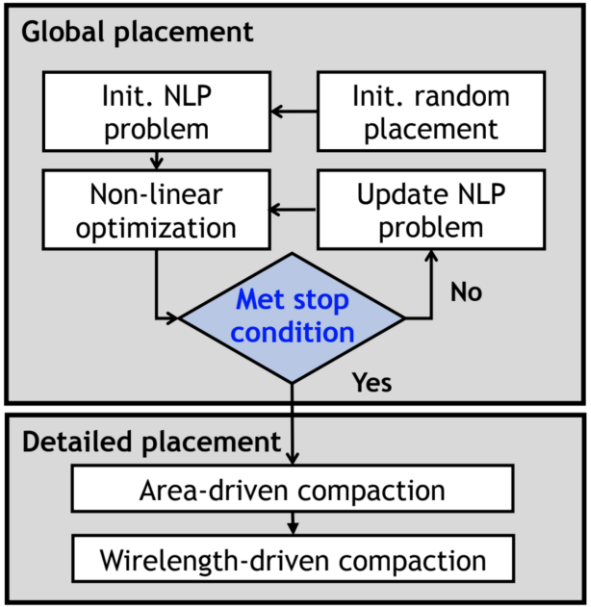

System-level constraints




Building block symmetry

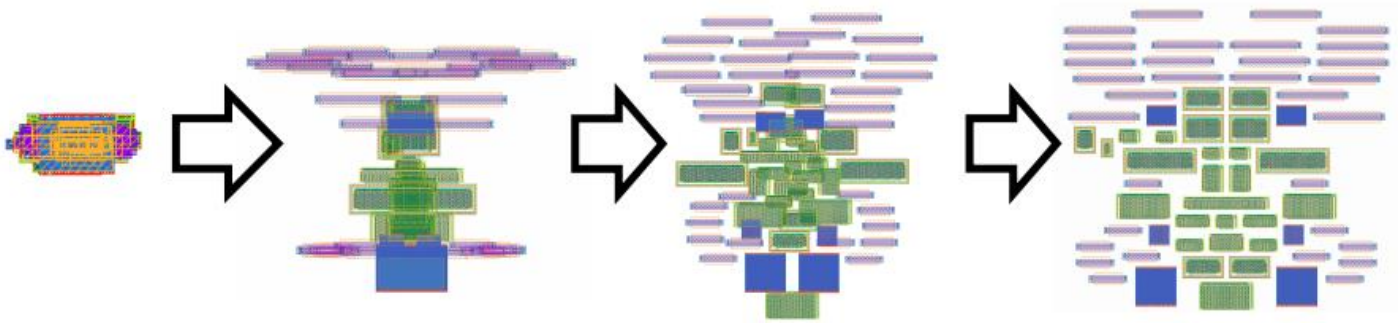
# MAGICAL 1.0: Placer

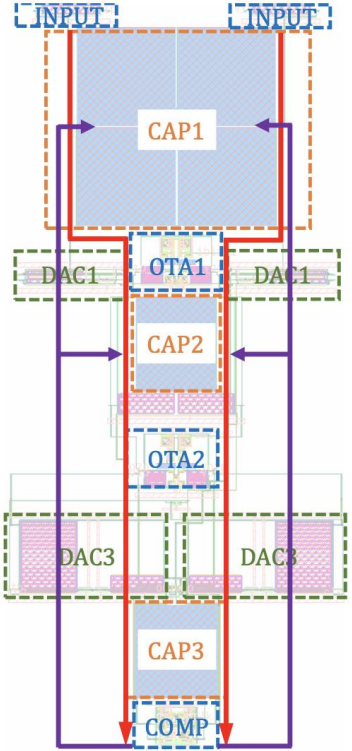
- Nonlinear programming-based global placement
- Linear programming-based detailed placement
- Using system signal flow to guide placement for mixed-signal placement
- [Zhu+, ICCAD'20]



# MAGICAL 1.0: Placer

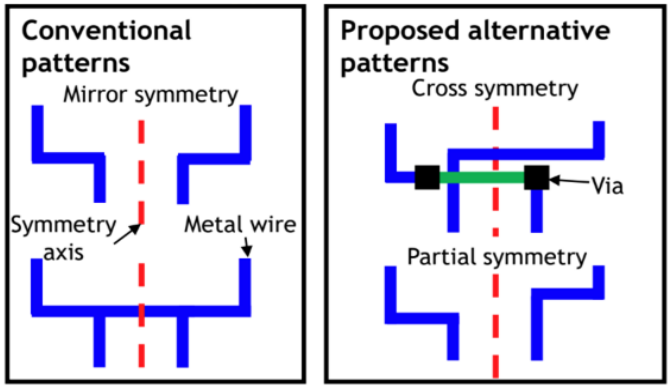
- Consider regularity of system signal flow in placement
- Improved numerical optimization kernel
- Better post-layout simulation performance and placement metrics

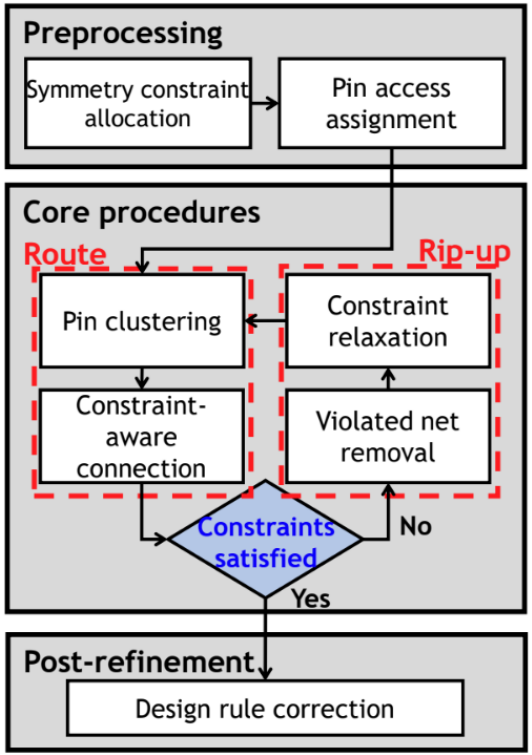




# MAGICAL 1.0: Router

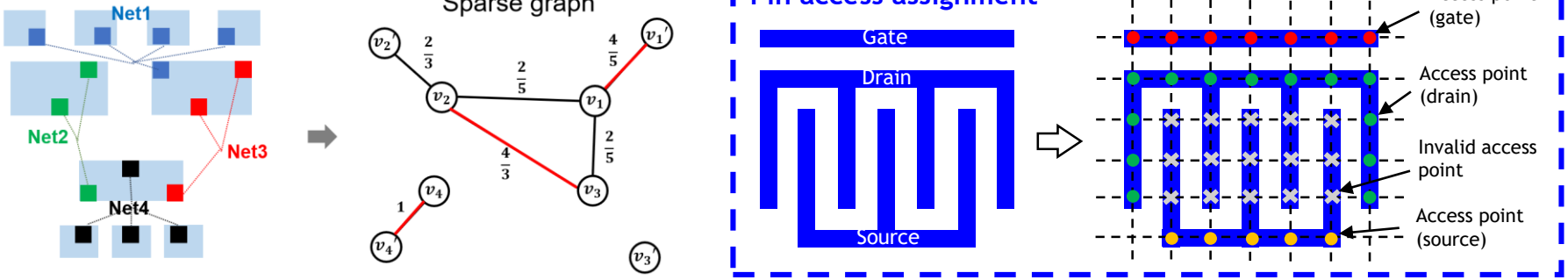
- Grid-based routing kernel w/ DRC handling
- New symmetry routing patterns
- Special power/ground routing
- [Chen+, ICCAD'20]



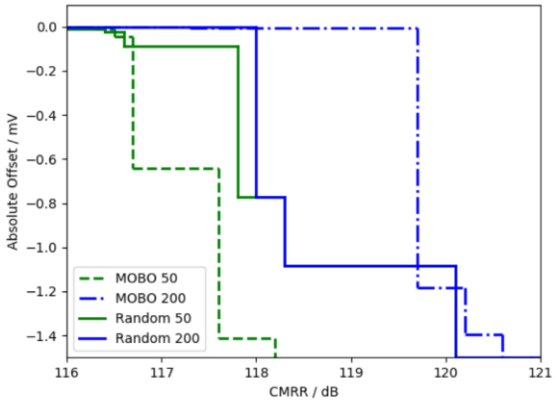
# MAGICAL 1.0: Router

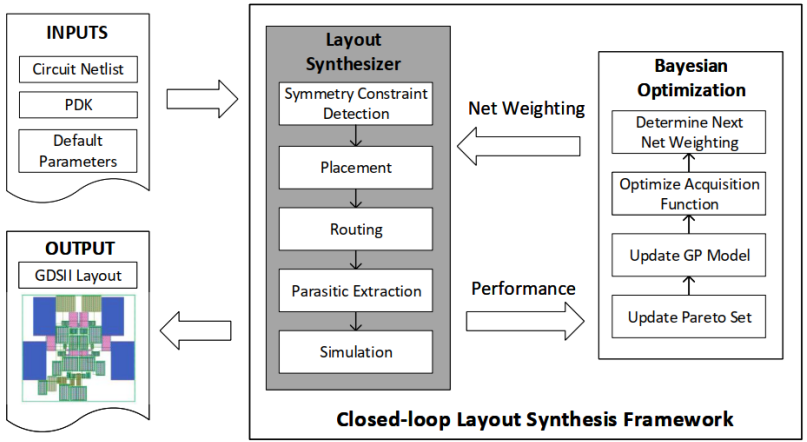
- Multiple vias and various wire widths for voltage drop consideration
- Symmetry constraint allocation
  - Maximize the overall potential routing symmetry (Weighted graph matching)
- Pin access assignment



# Simulation in the Loop

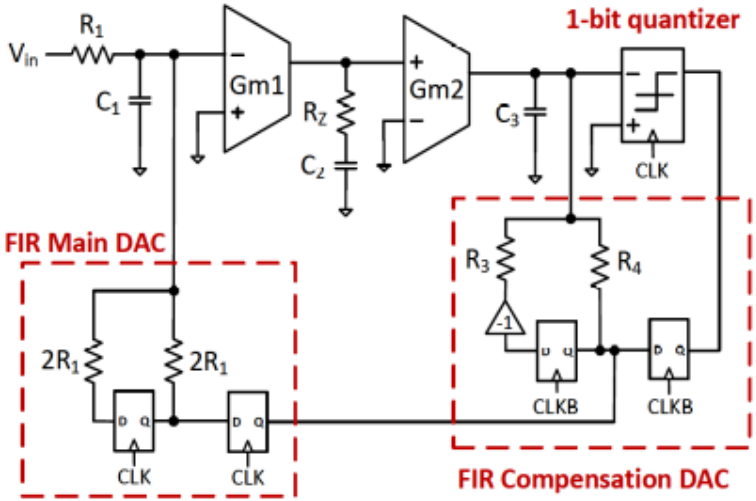
- Simulation-in-loop: use simulation results on building block level circuits as the feedback to the MAGICAL P&R
- Intelligent performance prediction will reduce #simulations
- [Liu+, DAC'20]



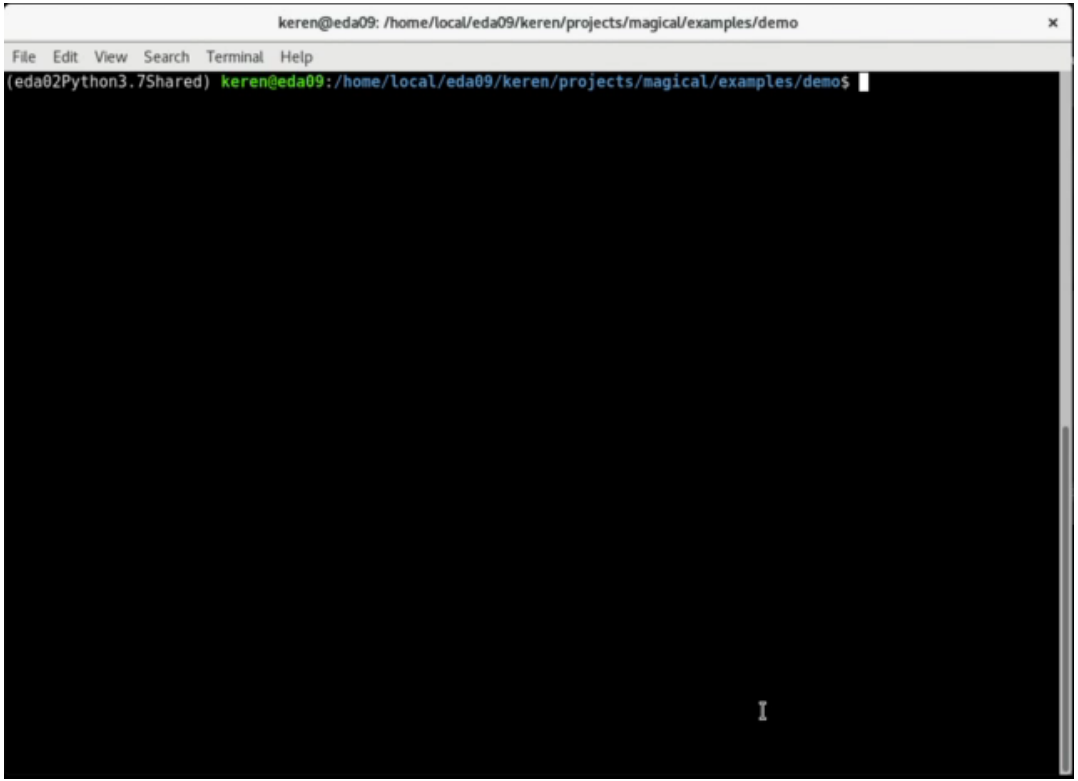



# MAGICAL 1.0: 3rd-order CTDSM Demo

- 1GS/s 3rd-order high-performance continuous time ΔΣ modulator
- State-of-the-art performance, originally published in IEEE SSC-L'20
- Include various sub-block types



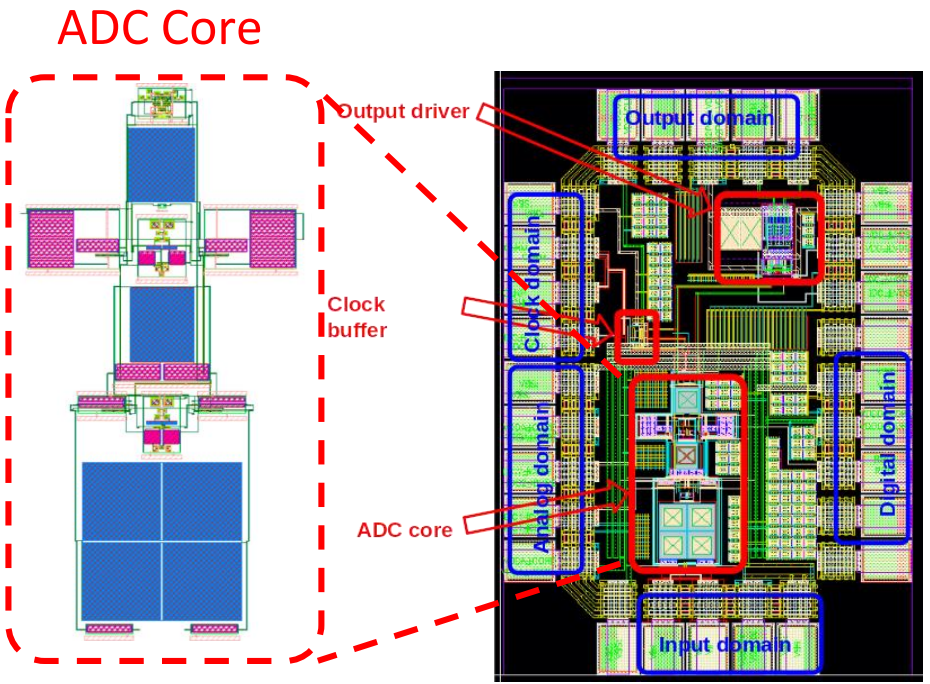
# MAGICAL 1.0: 3rd-order CTDSM Demo




*For demo purpose, simulation in the loop not included.

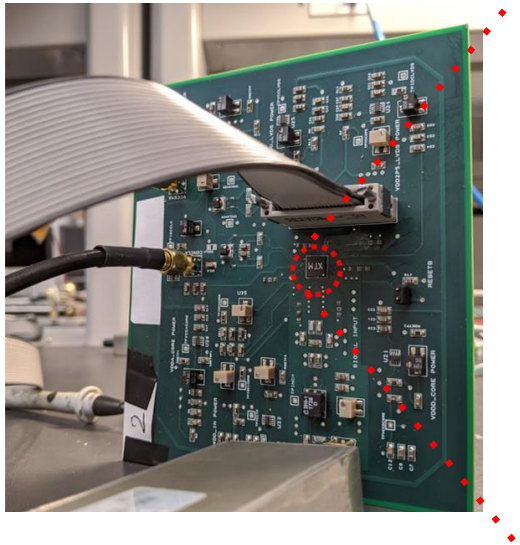
# MAGICAL 1.0: Fully Synthesized ADC Core

- After ~90 seconds….
- Core area: 22,000 $um^2$
- Tape-out with manually designed peripherals (buffer, driver, PADs)

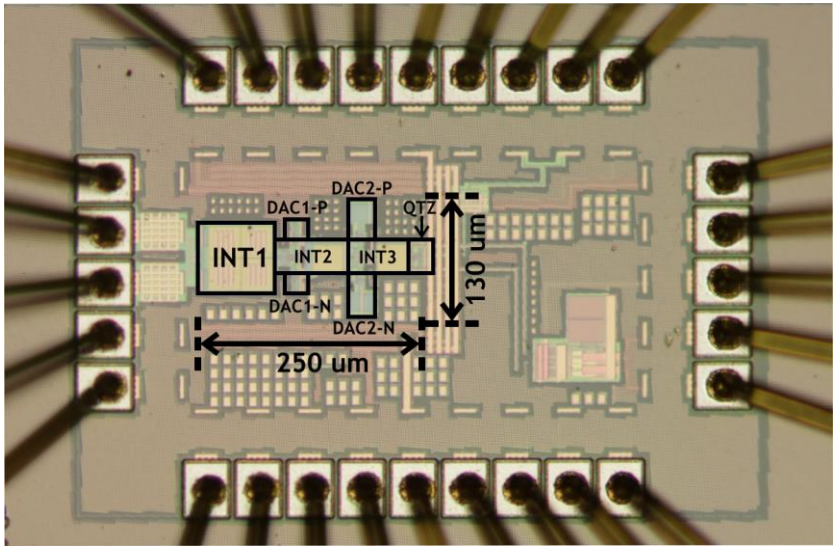


# MAGICAL 1.0: Measurement

- CTDSM ADC chip under TSMC40 technology

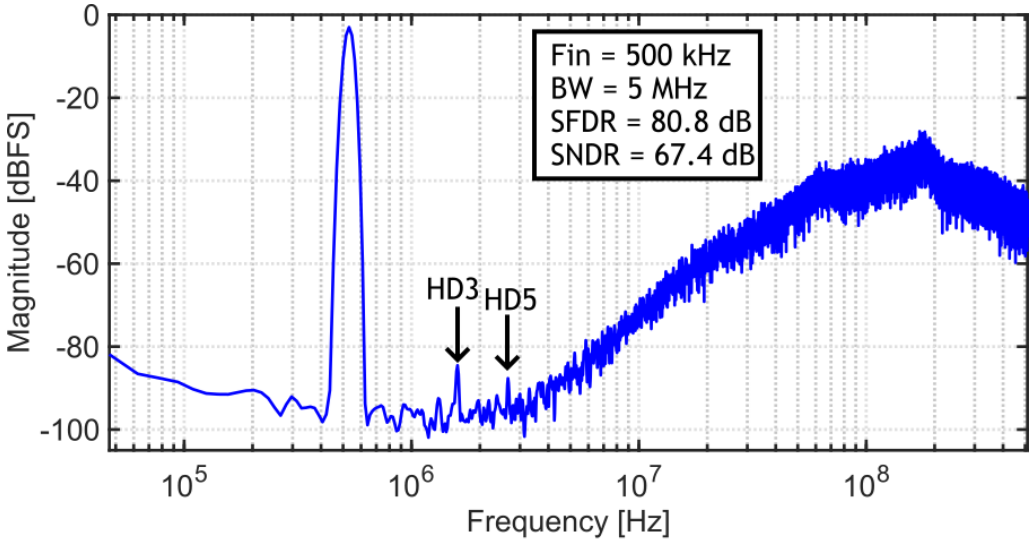


PCB board



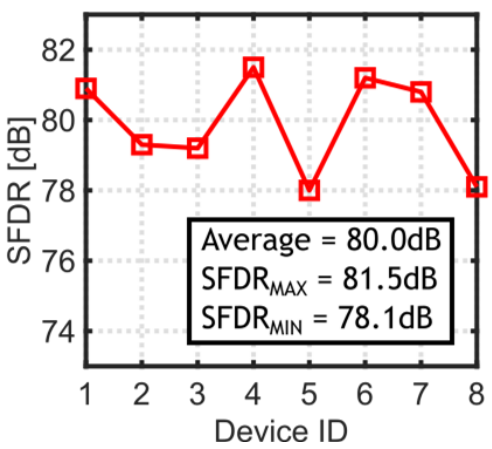

Chip micrograph of the synthesized CTDSM

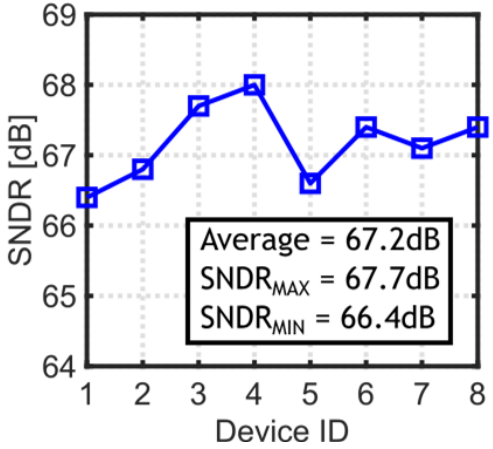
# MAGICAL 1.0: Measurement




Fs: 1GHz
BW: 5MHz
SNDR: 67.4dB
SFDR: 80.8dB

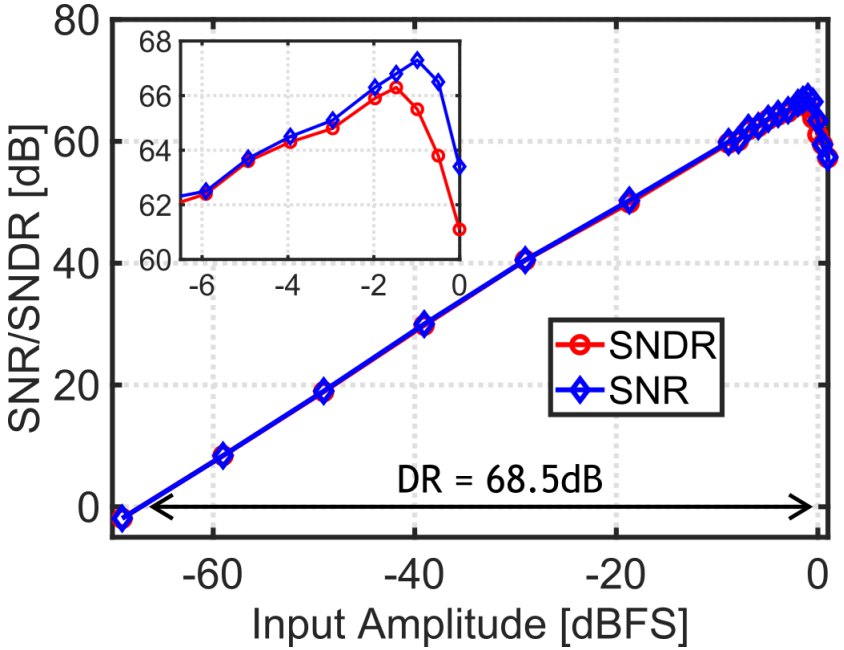
# MAGICAL 1.0: Measurement




Stable performance across 8 samples.

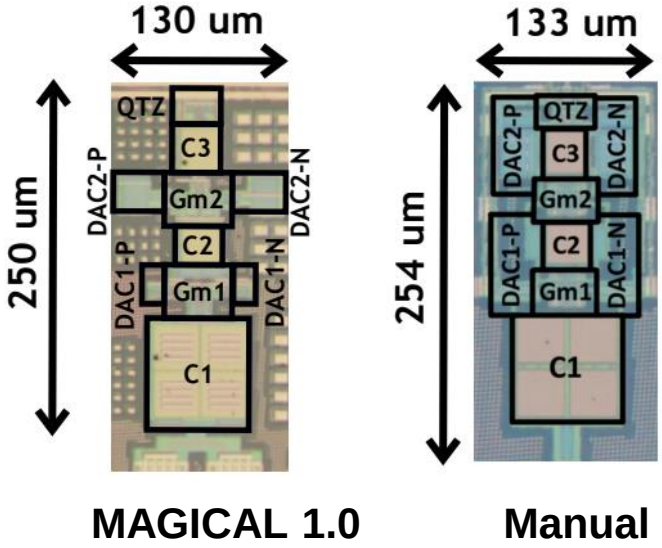
# MAGICAL 1.0: Measurement




DR: 68.5dB

# Comparison with SOTA CTDSM ADCs

- Only require signal flow information
- Comparable layout with manual design [SSCL ’20 Mukherjee]



# Comparison with SOTA CTDSM ADCs

- Fully-synthesized layout

| | JSSC-16 Weng | SSCL-20 Mukherjee[1] | CICC-19 Li | **This work[1]** |
|---|---|---|---|---|
| Architecture | CTΔΣM | CTΔΣM | VCO-CTΔΣM | CTΔΣM |
| Layout synthesized | ✗ | ✗ | ✓ | ✓ |
| Universal synthesis framework | N/A | N/A | ✗ | ✓ |
| Hierarchical flow | N/A | N/A | ✗ | ✓ |
| Constraint generation | N/A | N/A | ✗ | ✓ |

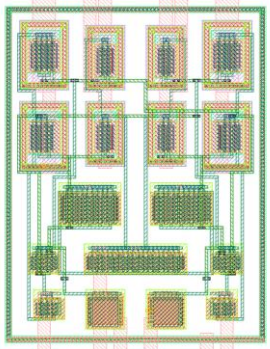
[1]: same schematic

# Comparison with SOTA CTDSM ADCs

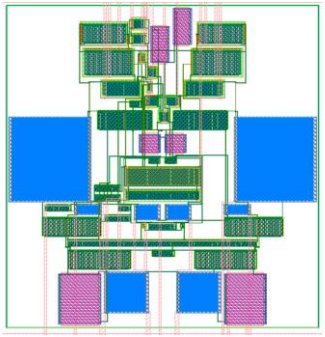
- Comparable results with other SOTA CTDSM ADCs

| | JSSC-16 Weng | SSCL-20 Mukherjee[1] | CICC-19 Li | **This work[1]** |
|---|---|---|---|---|
| Architecture | CTΔΣM | CTΔΣM | VCO-CTΔΣM | CTΔΣM |
| Order | 4th | 3rd | 1st | 3rd |
| Area [$mm^2$] | 0.1 | 0.034 | 0.01 | 0.033 |
| Fs [MHz] | 320 | 1024 | 600 | 1024 |
| Power [mW] | 4.2 | 0.79 | 1.08 | 0.77 |
| BW [MHz] | 10 | 5 | 4 | 5 |
| SNDR [dB] | 74.4 | 65.6 | 68.8 | 67.4 |
| FoMw [fJ/c-s] | 49.3 | 51 | 60 | 40.2 |
| FoMs [dB] | 174.5 | 163.6 | 164.3 | 165.5 |

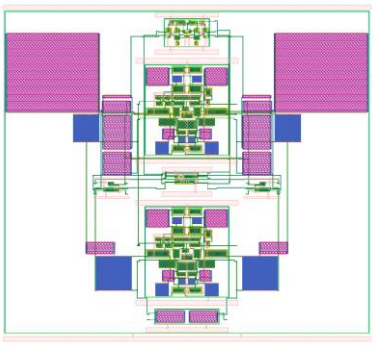
# MAGICAL 1.0: Other Circuits



Comparator



Inverter-Based Feed-Forward OTA



2nd-Order CTDSM

# MAGICAL 1.0: Public Release

- **Open-sourced MAGICAL 1.0** (under BSD-3 license), https://github.com/magical-eda/MAGICAL with key updates:
  - Push-button, no-human-in-the-loop (can take user constraints too)
  - End-to-end analog layout generation from netlist to GDSII
  - New placement and routing engines
  - DRC clean, LVS clean
- Real-world circuit examples (PDK-stripped)
  - https://github.com/magical-eda/MAGICAL-CIRCUITS
- Open-sourced UT-AnLay dataset and ML model for analog post-layout performance prediction https://github.com/magical-eda/UT-AnLay

## Acknowledgments


- The authors thank DARPA and NSF for supporting this project and TSMC for university shuttle program.


# Thank you!
# Q & A