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DEC 5 - 9, 2021 ◆ San Francisco, California

Universal Symmetry Constraint Extraction for Analog and Mixed-Signal Circuits with Graph Neural Networks

Hao Chen, Keren Zhu, Mingjie Liu, Xiyuan Tang, Nan Sun, and David Z. Pan

ECE Department, The University of Texas at Austin

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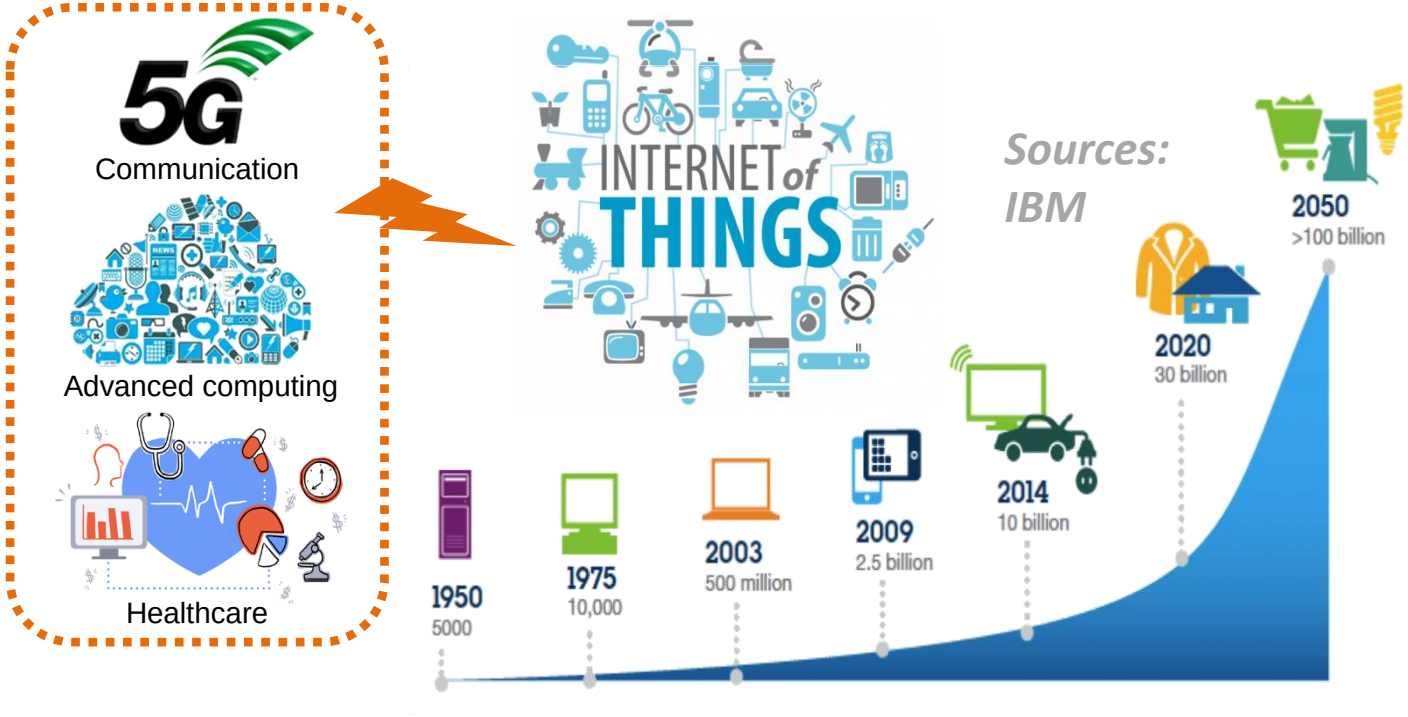
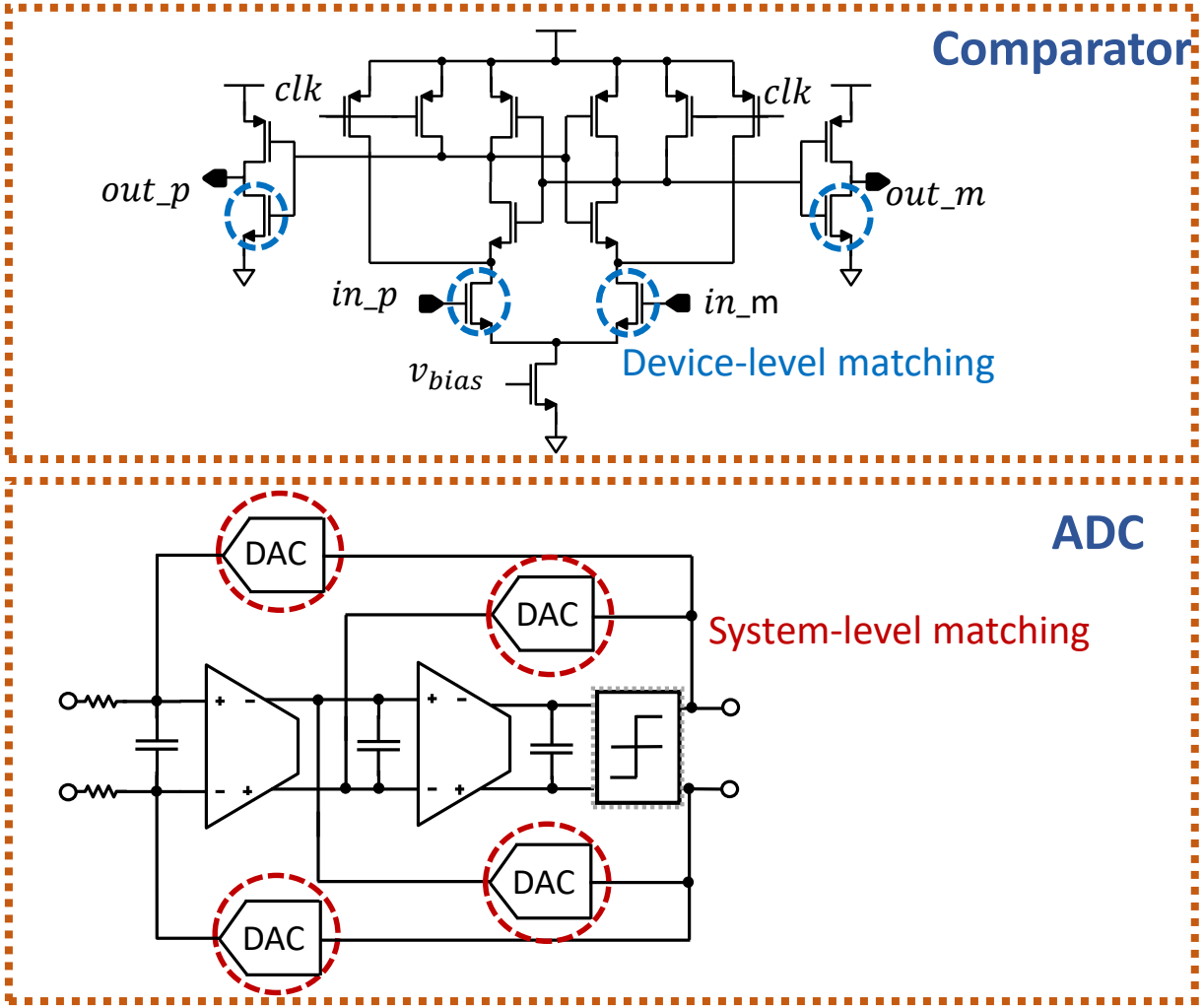
High Demand of Analog/Mixed-Signal ICs

- Internet of Things (IoT), autonomous and electric vehicles, communication and 5G networks…
- Every sensor-related application needs analog circuits!!

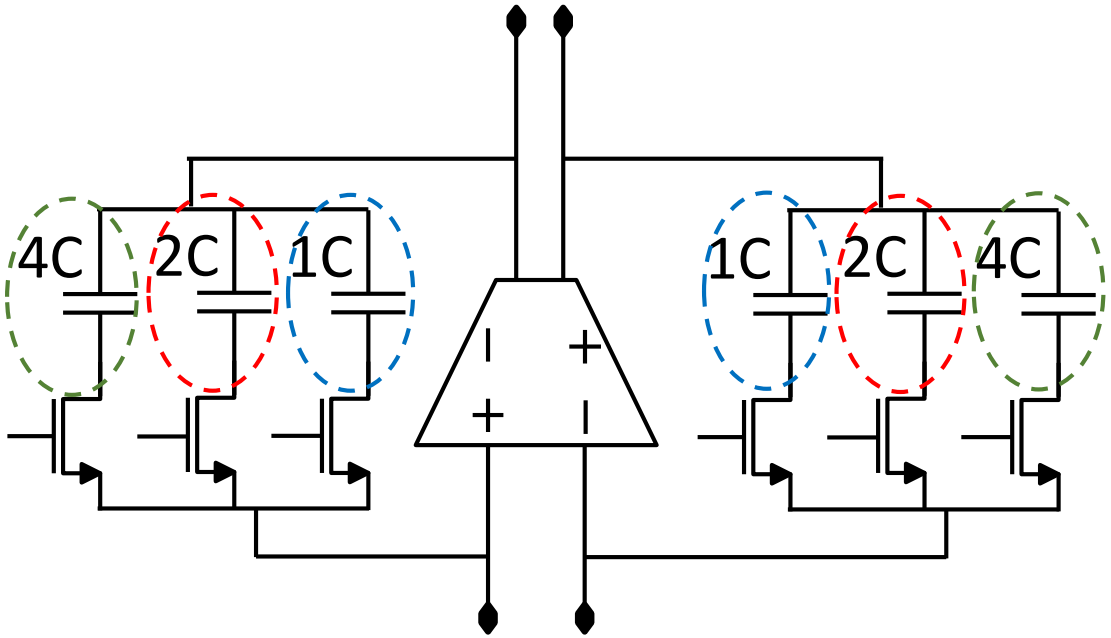


Symmetry Matching in Analog Circuits

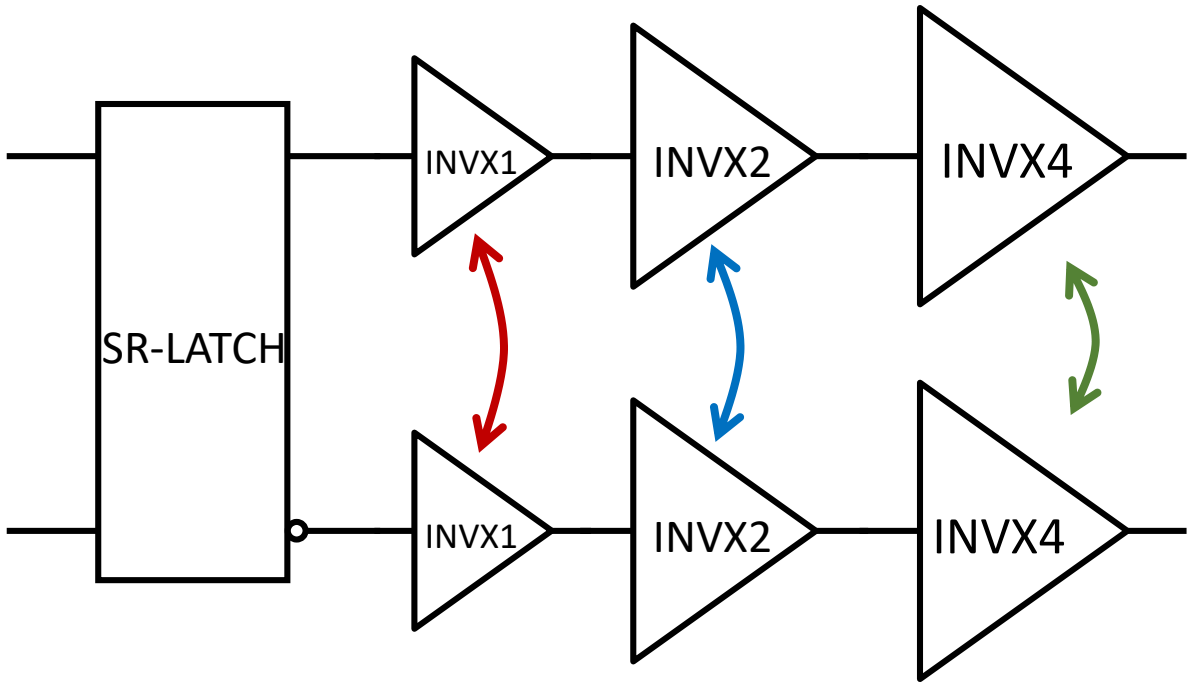
- Device-level matching
  - Symmetry constraints for primitive devices (transistors, capacitors, resistors, etc.)
- System-level matching
  - Symmetry constraints for building block circuits in larger systems (DACs, inverters, etc.)



Sizing Information for Symmetry Matching



Matched capacitors considering sizing information

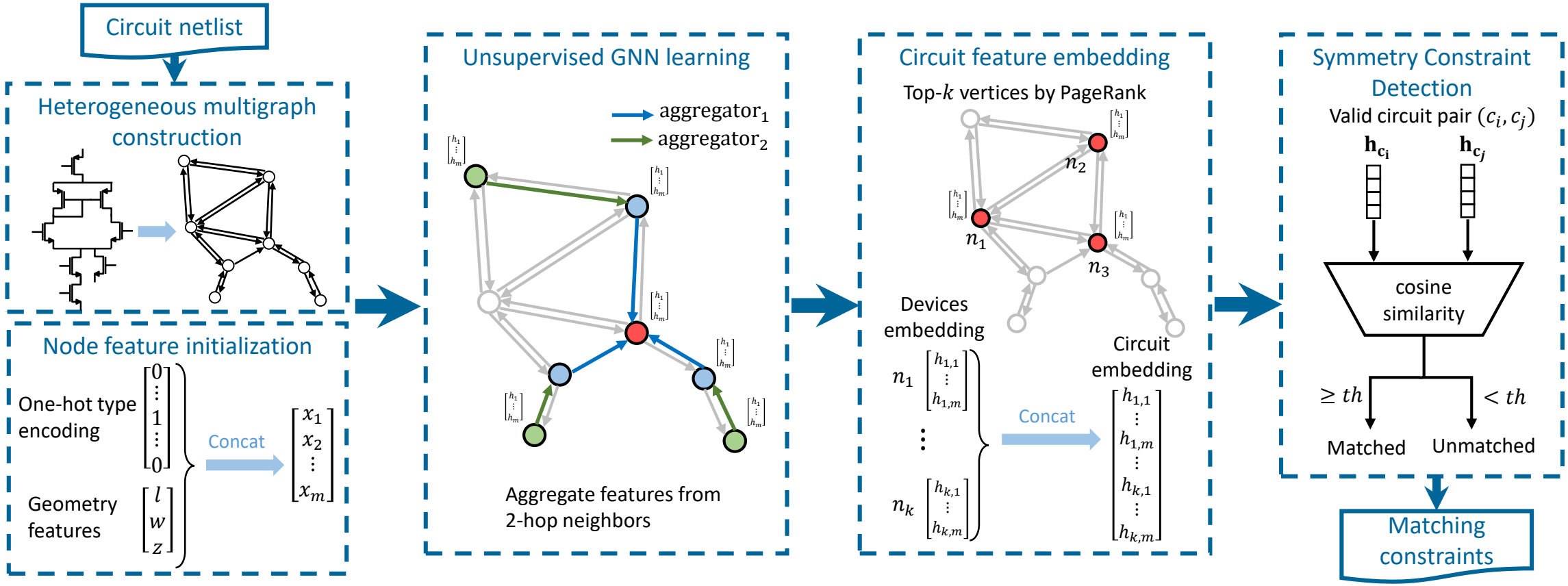


Matched subcircuits considering sizing information

Prior Art of Symmetry Constraint Extraction

	[Xu+, ICCAD'19]	[Liu+, ASPDAC'20]	[Kunal+, ICCAD'20]	[Gao+, ASPDAC'21]	Ours
Circuit representation	Graph	Graph	Bipartite graph	Graph	Heterogeneous multigraph
Training method	N/A	N/A	Supervised	Supervised (+path-based features)	Unsupervised
Circuit embedding	N/A	Graph Laplacian matrix	GNN	GNN	GNN
Sizing consideration	N/A	N/A	Devices	N/A	Devices + Circuits
Device-level matching	SFA + Heuristic patterns	N/A	Heuristic patterns	GNN classification	Cosine similarity
System-level matching	N/A	K-S test	GED	N/A	Cosine similarity

Our Symmetry Extraction Framework



Heterogeneous Multigraph Representation

Node (Device)

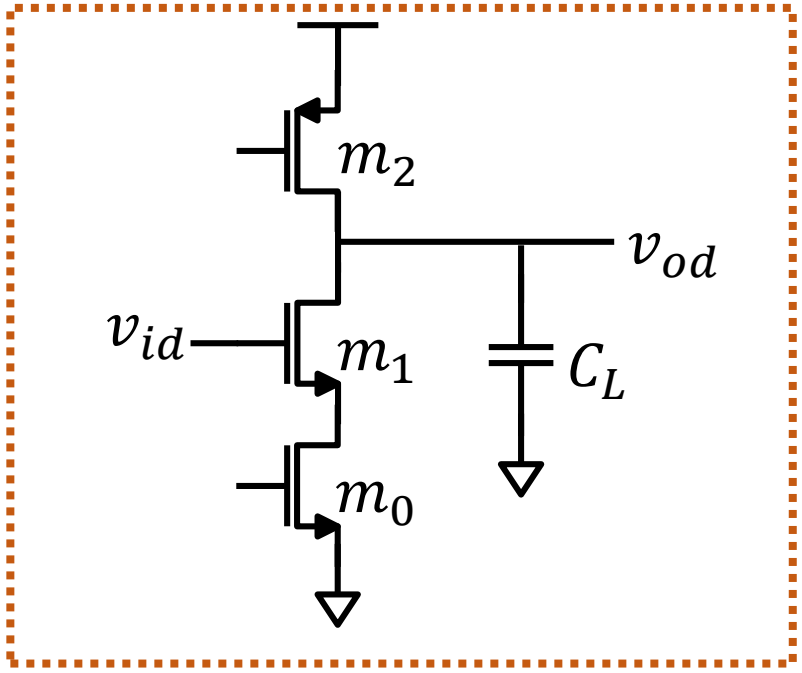
Edge (to passive)

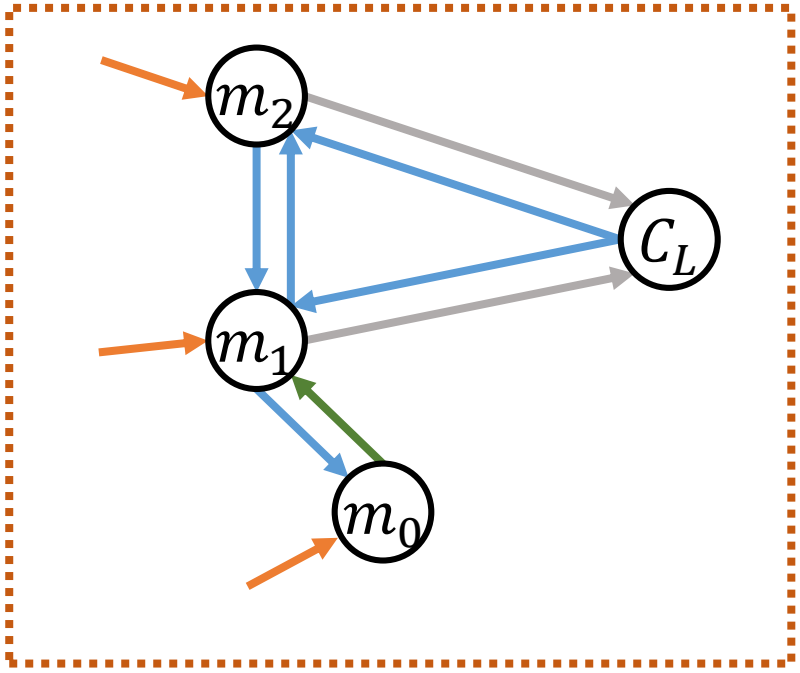
Edge (to drain)

Edge (to gate)

Edge (to source)

Four edge types





Graph Node Features and Training

Features

- Device type (15)
- Geometry
  - Width (1)
  - Length (1)
- #Layers (1)

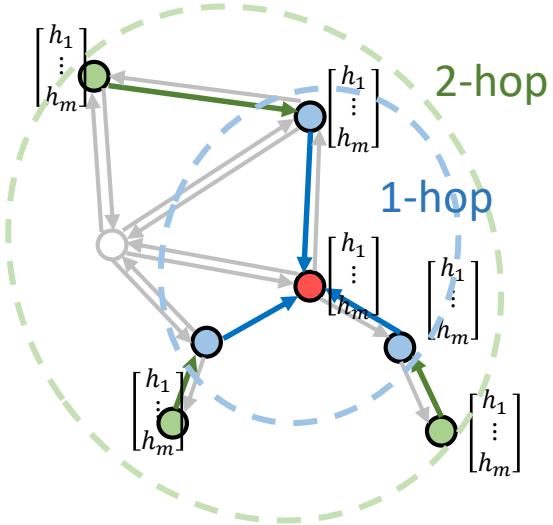
Aggregation function

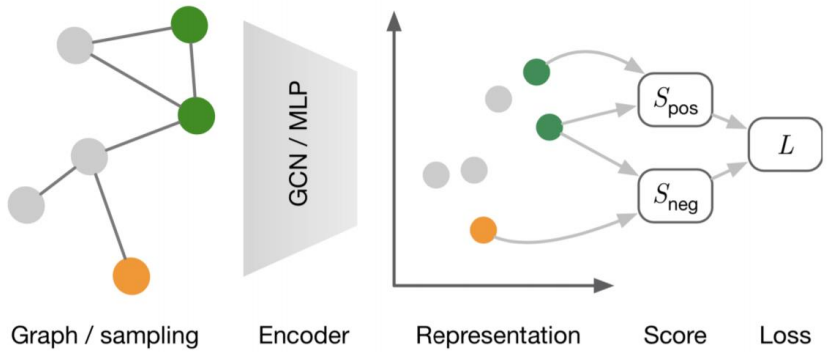
$$h_v^{(k)} = GRU\left(h_v^{(k-1)}, \sum_{u \in \mathcal{N}_{in}(v)} W_{e_{uv}} h_u^{(k-1)}\right)$$

Training loss function

$$\mathcal{L}(z_v) = -\sum_{u \in \mathcal{N}_{in}(v)} \log\left(\sigma(z_u^\top z_v)\right) - \sum_{i=1}^{B} \mathbb{E}_{\tilde{u} \sim Neg(v)} \log\left(1 - \sigma\left(z_{\tilde{u}}^\top z_v\right)\right)$$

$$\mathcal{L}_{total} = \sum_v \mathcal{L}(z_v)$$

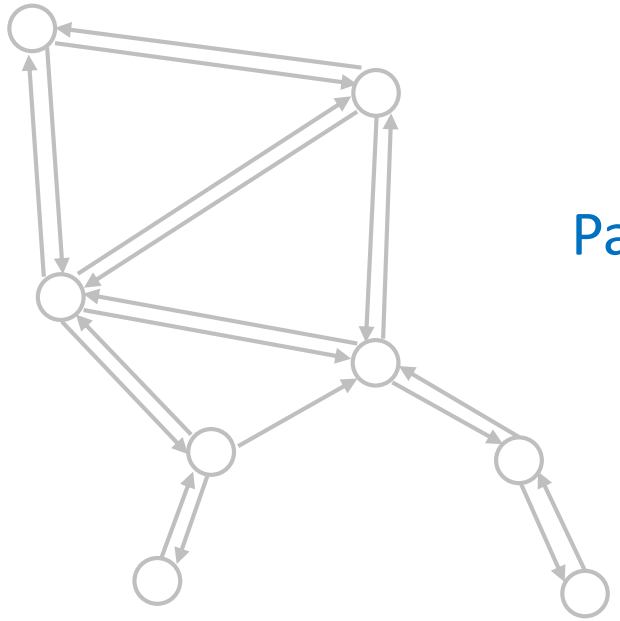




***Courtesy of [Kipf**, GLWS4'19]*

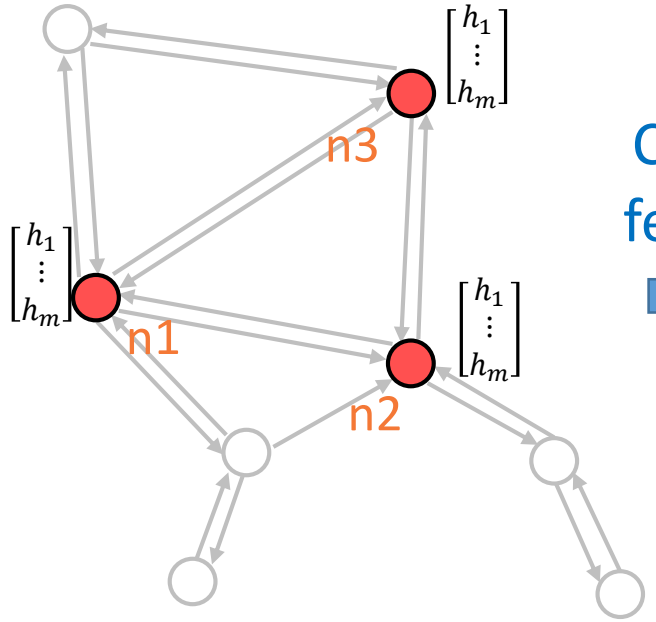
Circuit Feature Embedding

C1



Circuit multigraph representation

PageRank



Extract the top-k most representative nodes

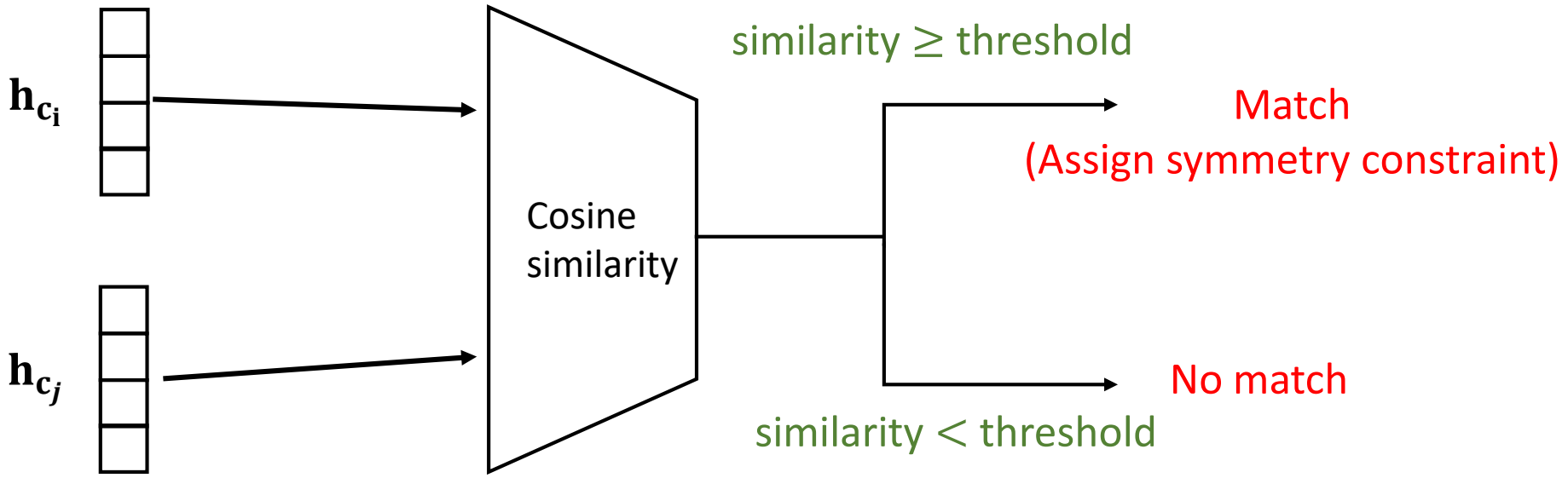
Concat. features

C1 feature

$$\begin{bmatrix} h_{1,1} \\ \vdots \\ h_{1,m} \\ \vdots \\ h_{3,1} \\ \vdots \\ h_{3,m} \end{bmatrix}$$

Symmetry Constraint Generation

For each valid circuit pair (c_i, c_j)



Compute the Cos. similarity of the two embedded feature

Experimental Results (Setup)

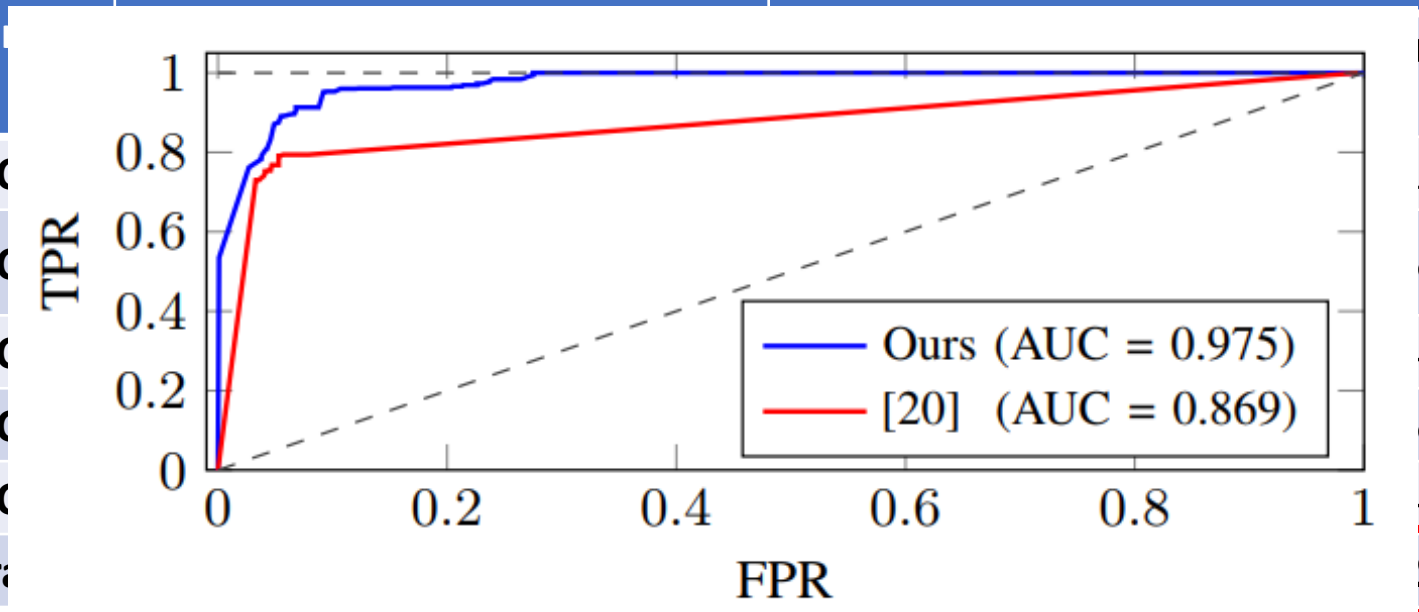
Setup
- Python with DGL
- CPU: Intel i9-7900X @ 3.3GHz

Benchmark circuits
- System-level circuits x5:
  - 2nd-order CT ΔΣ modulator x2
  - 3rd-order CT ΔΣ modulator x1
  - SAR x1
  - Hybrid CT ΔΣ SAR x1
- Block-level circuits x15:
  - OTA x6, COMP x6, DAC x2, LATCH x1

Experimental Results (System-level)

Spectral method with graph similarity

Benchr	[Liu+, ASPDAC'20]	Ours	ne
ADC			
ADC			
ADC			
ADC			
ADC			
Avera			



>200X speedup

Comparison on system-level symmetry constraint extraction

ROC curve

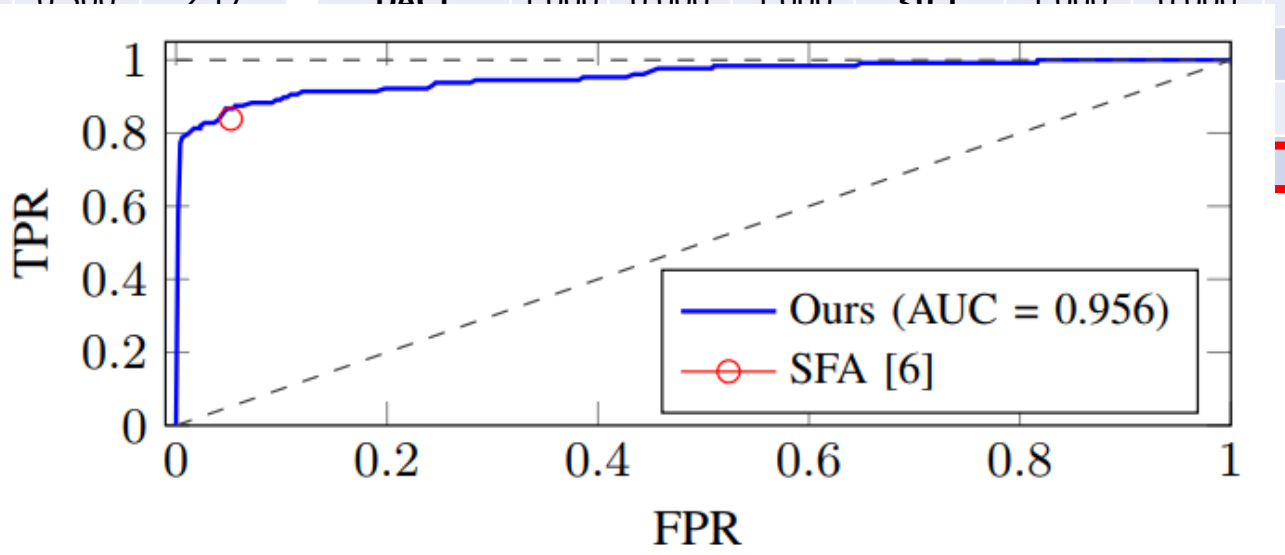
Training time: $\sim 30s$

Experimental Results (Device-level)

Signal flow analysis with pattern matching

Benchmark	[Xu+, ICCAD'19]				Ours			
	ACC	FPR	F-1 Score	Runtime	ACC	FPR	F-1 Score	Runtime
OTA1	0.941	0.000	0.800	**<0.1**	0.882	0.000	0.500	2.17
OTA2	0.833	0.171	0.483	**<0.1**	0.922	0.049		
OTA3	0.867	0.083	0.667	**<0.1**	0.867	0.000		
OTA4	0.861	0.131	0.271	**<0.1**	0.981	0.007		
OTA5	0.989	0.004	0.870	**<0.1**	0.975	0.011		
OTA6	0.870	0.000	0.727	**<0.1**	1.000	0.000		
COMP1	0.895	0.108	0.329	**<0.1**	0.989	0.011		
COMP2	1.000	0.000	1.000	**<0.1**	1.000	0.000		
COMP3	0.978	0.016	0.824	**<0.1**	0.996	0.004		
COMP4	0.921	0.057	0.526	**<0.1**	0.956	0.019		
COMP5	0.875	0.143	0.667	**<0.1**	1.000	0.000		
COMP6	1.000	0.000	1.000	**<0.1**	1.000	0.000	1.000	2.17

Benchmark	[Xu+, ICCAD'19]				Ours			
	ACC	FPR	F-1 Score	Runtime	ACC	FPR	F-1 Score	Runtime
DAC1	1.000	0.000	1.000	**<0.1**	1.000	0.000	1.000	2.17
							1.000	2.17
							0.750	2.18
							0.815	2.17



ROC curve

Comparison on device-level symmetry constraint extraction

Conclusions

GNN-based AMS symmetry constraint extraction

- Heterogeneous multigraph circuit representation
- Circuit feature with sizing information consideration
- Unsupervised learning on GNNs for generalizability

Future directions

- More analog constraints (common-centroid, etc.)
- Improvement on precision/accuracy
- Handling extended circuit classes

Thank you!!