Programming Assignment #2

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Data Structure

To implement the B*-tree floorplanning representation proposed in [1] , we require 2 primary data structures: a binary tree (B*-tree) and a doubly linked list for the horizontal contour. Consequently, each module `Block` is equipped with 5 `Block*` pointers: 3 for the B*-tree (`left_`, `right_`, and `parent_`) and 2 for the doubly linked list (`prev_` and `next_`).

The perturbation methods for the B*-tree and the process of updating the contour doubly linked list are identical to those described in [2]:

1. Perturbation methods for the B*-tree:
   (1) Rotate: doesn't affect B*-tree structure $\Rightarrow O(1)$.
   (2) Move: delete a node and insert it somewhere. Deletion may need $O(h)$ if the node to delete has 2 children; otherwise $O(1)$. Insertion is always $O(1)$.
   (3) Swap: by exchanging pointers of the 2 nodes $\Rightarrow O(1)$.
2. Updating the contour doubly linked list: for a module, start from its `parent_` and keeps updating the contour list until there's no x-coordinate overlapping with it in the list. The y-coordinate of each module can be computed in amortized $O(1)$.

Algorithm

I adopt the adaptive Fast-SA scheme for fixed-outline floorplanning proposed in [3] to optimize the floorplan, with some modification:

1. **Hyperparameters**: I adjusted certain hyperparameters from [3] for improved result, such as k, c in the temperature function, and α_{base}, n in adaptive SA.
2. **Cost function**: in the Fixed-Outline Floorplanning section of [3], the 3 terms in the cost function (area, wirelength, and aspect ratio penalty) are not normalized. However, in the evaluator's cost function, area and wirelength are normalized:

$$\text{Cost} = \alpha \frac{A}{A_{\text{norm}}} + (1-\alpha)\frac{W}{W_{\text{norm}}}$$

And it lacks the aspect ratio penalty term. Therefore, I adjust my cost function to

$$\text{Cost} = \alpha_{\text{adapt}} \left[\alpha \frac{A}{A_{\text{norm}}} + (1-\alpha)\frac{W}{W_{\text{norm}}} \right] + (1-\alpha_{\text{adapt}}) \left(\frac{R-R^*}{D_{\text{norm}}} \right)^2$$

where α_{adapt} is the original adaptive α in adaptive SA, and D_{norm} is the normalization term of the aspect ratio Difference $|R - R^*|$.

For the detail operation in a single SA iteration, I follow steps similar to those in [4], such as performing $O(n)$ times perturbations in a single iteration and prematurely exiting the current iteration if too many uphill moves occur. A minor difference is in handling numerous rejected moves: while classic SA would typically terminate the entire SA process, fixed-outline floorplanning requires checking for any recorded feasible solutions. If none exist, the temperature is reset to initial high values in an attempt to escape the current local minimum.

Findings

After conducting several tests, I found that the hyperparameters of simulated annealing significantly impact the results. Given that it's a probabilistic technique, there are no consistent patterns for certain hyperparameters, making it challenging to identify an optimal set of parameters for each scenario.

Result

Run my program on EDA Workstation edaU13, with $\alpha = 0.5$ for each case.

Case	Area	Wirelength	Runtime (s)	Score
ami33	1233232	74097	3.908803	7.87128
ami49	40090624	767214	0.617996	9.28877
apte	47313280	748244	0.004008	9.91845
hp	9436616	259069	0.051410	18.40602
xerox	21304416	515773	0.016991	8.93281

Reference

[1] Yun-Chih Chang, Yao-Wen Chang, Guang-Ming Wu and Shu-Wei Wu, "B*-trees: a new representation for non-slicing floorplans," Proceedings 37th Design Automation Conference, Los Angeles, CA, USA, 2000, pp. 458-463, doi: 10.1145/337292.337541.

[2] L. T. Wang, Y. W. Chang, and K. T. Cheng, Electronic Design Automation: Synthesis, Verification, and Test. Morgan Kaufmann, 2009.

[3] Tung-Chieh Chen and Yao-Wen Chang, "Modern floorplanning based on B/sup */-tree and fast simulated annealing," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 25, no. 4, pp. 637-650, April 2006, doi: 10.1109/TCAD.2006.870076.

[4] D. F. Wong and C. L. Liu, "A New Algorithm for Floorplan Design," 23rd ACM/IEEE Design Automation Conference, Las Vegas, NV, USA, 1986, pp. 101-107, doi: 10.1109/DAC.1986.1586075.