COL216 Computer Architecture

Encoding of instructions to be implemented

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Cond				F		I	Opcode				S	Rn				Rd				Operand2													Instruction
1110				00		1	0100				0	Rn				Rd				RotSpec 0000				Imm8								ADD imm
							0010																									SUB imm
							1101																									MOV imm
							1010				1																					CMP imm
						0	0100				0									ShftSpec 00000000								Rm				ADD reg
							0010																									SUB reg
							1101																									MOV reg
							1010				1																					CMP reg

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Cond				F		I	P	U	B	W	L	Rn				Rd				Offset												Instruction
1110				01		0	0	1	0	0	0	Rn				Rd				Imm12												STR imm offset (+)
											1																					LDR imm offset (+)
								0			0																					STR imm offset (-)
											1																					LDR imm offset (-)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Cond				F		Opc		Offset																								Instruction
1110				10		10		Imm24																								B
0000																																BEQ
0001																																BNE

This should be '1' instead of '0'