Single Cycle CPU Design Synthesis and Testing on FPGA Board

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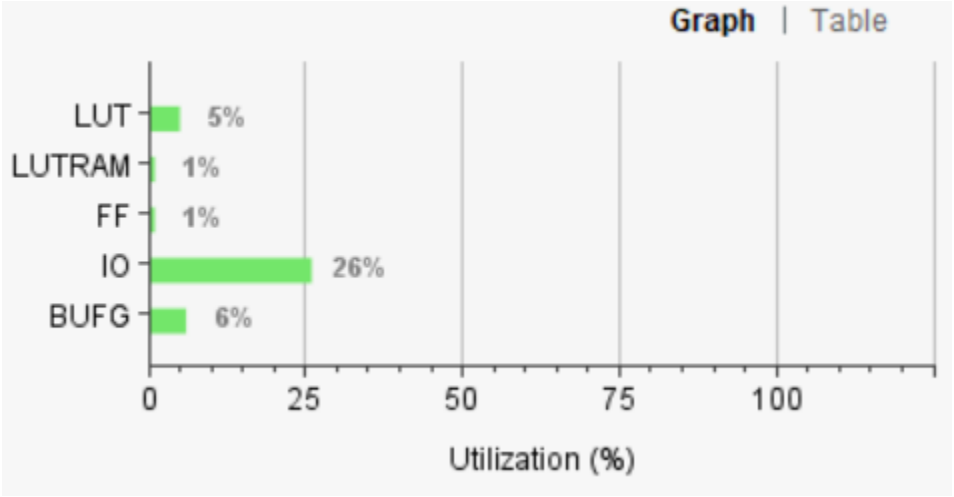
This was an extension of Lab Assignment 4 and Lab Assignment 5. Here we have designed a Finite State Machine(`FSM`) for execution of instructions. The `FSM` helps in execution of instructions step-by-step and also there is an option of executing entire program in one go.

After each step the registers of Register File(`RF`) can be seen on `LEDs` by specifying the register number to be seen by slide switches(`R2 T1 U1 W2`). Since, the registers are 32 bit and only 16 bit can be shown at a time, therefore another slide switch(`R3`) can be used to choose which part of register is to be seen at the time('1' for upper half and '0' for lower half).

Multiple Programs(Maximum 8) can be executed by specifying the program number to be executed through slide switches(`W16 V16 V17`). In the current bit file, Program No 0,1,2,3,4, and 6 are for calculating Array Sum, and Program No 5 and 7 for calculating Fibonacci number. Push button `U18` is for Reset, `W19` is for executing instructions step-by-step, and `T17` is for executing step in one go. Everytime a new program is loaded, reset button has to be pressed.



Utilization Report

Site Type	Used	Fixed	Available	Util%
Slice LUTs	998	0	20800	4.80
LUT as Logic	870	0	20800	4.80
LUT as Memory	128	0	9600	1.33
LUT as Distributed RAM	128	0		
LUT as Shift Register	0	0		
Slice Registers	642	0	41600	1.54
Register as Flip Flop	607	0	41600	1.46
Register as Latch	35	0	41600	0.08
F7 Muxes	257	0	16300	1.58
F8 Muxes	96	0	8150	1.18

Timing Summary Report

WNS(ns)	0.236
TNS(ns)	0.000
TNS Failing Endpoints	0
TNS Total Endpoints	2473
WHS(ns)	0.049
THS(ns)	0.000
THS Failing Endpoints	0
THS Total Endpoints	2473
WPWS(ns)	3.750
TPWS(ns)	0.000
TPWS Failing Endpoints	0
TPWS Total Endpoints	731