COL216 Computer Architecture

Lab Assignments 9

CPU with all ARM Data Transfer (DT) instructions

Objective

The Data transfer instructions implemented in the previous assignments include only full word (32-bit) load/store with the following variants.

- Only immediate offset
- Offset addition (U = '1') as well as offset subtraction (U = '0')

This assignment aims to extend this to include transfers of all types as well as all variants of addressing.

Scope

Transfer types:

Apart from full word transfers, now half word transfers {ldrh, strh} as well as byte transfers {ldrb, strb} are to be implemented, including signed variants of load instructions for half word and byte {ldrsh, ldrsb}.

Address offset:

Register offset, with shift specification similar to DP instructions, is to be implemented in addition to immediate offset.

Addressing modes:

Addition/subtraction of the offset to the base register may be performed either before (pre-indexed, P = '1') or after (post-indexed, P = '0') the base is used as the transfer address. The write-back bit W gives optional auto increment and decrement addressing modes. The modified base value may be written back into the base (W = '1'), or the old base value may be kept (W = '0'). In the case of post-indexed addressing, the write back bit is redundant and must be set to zero. Post-indexed data transfers always write back the modified base.

Design

The following changes need to be made to the previous design.

Instruction decoder

Encoding of all the instructions, covered up to this assignment, is shown in file "Instruction encoding for Lab9.pdf". In the Instruction decoder, check all the fields shown in light green shade in order to ensure that all incorrectly encoded instructions are rejected.

Processor-Memory datapath

This is the combinational circuit that needs to be introduced in the processor-Memory datapath. It can extract a byte or half word from the full data word coming from memory, extending it with zeroes or sign bit. Also, it can form the data word going to memory by taking a byte or half word from the processor and replicating it. Refer to slides 18-22 of Lecture 11 for details. The data memory needs to be structured as a set of four 8-bit wide memories with common address input, but separate write enable inputs.

Memory address

No change is required for computing the memory address for instructions {ldr, str, ldrb, strb}, since the logic already exists for adding / subtracting the offset to Rn, which can be the12-bit immediate field or Rm shifted by an amount specified by a 5-bit immediate field. However, instructions {ldrh, strh, ldrsb, ldrsh} have an 8 bit offset, specified by instruction bits 11-8 and 3-0. That would require some additional multiplexing.

Register file and control states

Depending upon how the instructions are broken into cycles, additional control states or additional register file ports would be required. The preferred approach is to keep the number of register file ports same (2R, 1W) and sequentialize additional RF reads and writes, by introducing new control states, if required. Slides 16-17 of Lecture 11 show some examples.