

# **A Complete ARM architecture-based CPU**

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We have completed all the 14 assignments and are submitting in time. An individual bit file for all the assignments are included in the submission, except for the Lab 13 & 14, they have a common bit file. All the assignments are implanted in their regular normal version. No assignment is implemented in their lite version. We have already given the demonstration of Lab 7-12.

The working of Assignment 7-11 on the FPGA board is the same. All the buttons and switches used are exactly the same, which we can see in their individual constraint file. Since Lab 7 was the base for all the assignments and till Lab 11 we just had to extend the code. We are submitting the code of Lab 11 which includes all the previous lab starting from Lab 7. There were slight changes in Lab 12 and hence its code is submitted separately. And also Lab 13 & 14 combined are submitted separately.

From Lab 7-11 we had a COE file which could take up to 8 programs at a time. And we used slide switches to determine which program to run. In Lab 7 and 8, Data and Program Memory were each 32 bit wide and had a depth of 256. From Lab 9 onwards we separated the Data Memory into 4 modules. Each module had a depth of 256 and a width of one byte. This was done in order to ease the processing of DT instructions such as ldrb, ldrh, strb, strh, etc. Program Memory was the same so there was no change in format of COE file.

From Lab 12 onwards we had unified the memory, and now program memory and Data Memory were the same. The COE file had changed completely, and now it can have only one program in it, with the user having access to only a few parts of the memory where it could read and write. Memory was unified in order to protect it and also to give our CPU a structure exactly as that of ARM. Now there was one main memory split into 4 modules. Each module was one byte wide and had a depth of 1024 . Since the memory module was changed the COE file was preprocessed using a small python script before loading into memory components and generating IP modules.

We have given functionality of step, go, one instruction and reset buttons in our CPU. Proper design practices were kept in mind while writing the code. All of our code is well commented and is properly separated into different modules.

We are also including the COE files corresponding to each bit file that is submitted. Bit file of each of the assignments contain different code; a few of them are mentioned below. (All the COE files contain various codes, but only the main program corresponding to that assignment is mentioned):

Lab 7- (i) Array Sum from 1 to 10 & (ii) 10<sup>th</sup> Fibonacci Number

Lab 8- A program that tests all the DP instructions. There was no main objective of this code.

Lab 9- A program that tests all the DT instructions.

Lab 10- A code that tests all the six available multiply instructions.

Lab 11- Fibonacci number and a program calculating power of 2 is written using instructions that use predications such as muleq, andne, etc.

Lab 12- It is the same COE file that was uploaded on Moodle.

Lab 13 & 14- A code that contains drivers to run SWI instructions. The main user code asks for hexadecimal digits from the user using PmodKYPD. The first digit entered is displayed on the seven-segment display at the extreme right, then the next at right middle, the next at left middle and the next at extreme left. It also asks for four more digits from user and then displays them accordingly on display all at a time.

We are also including a folder in our submission that contains various test cases that we have used to check our code exhaustively. Overall, this course was too much fun because of the labs and assignments. We enjoyed a lot while implementing them. It was an enthralling experience to design this processor week by week. We got to learn a lot from it, learning to use new tools in VHDL, understanding the ways to implement logic in VHDL while we used to debug our codes. And it was a joyous experience when we finally got our end product.

Thanks to all of you for helping us throughout the semester in bringing out this result !!