EE 671 VLSI Design
Course Project 1

Team 39

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Circuit Diagram and MOS Sizing

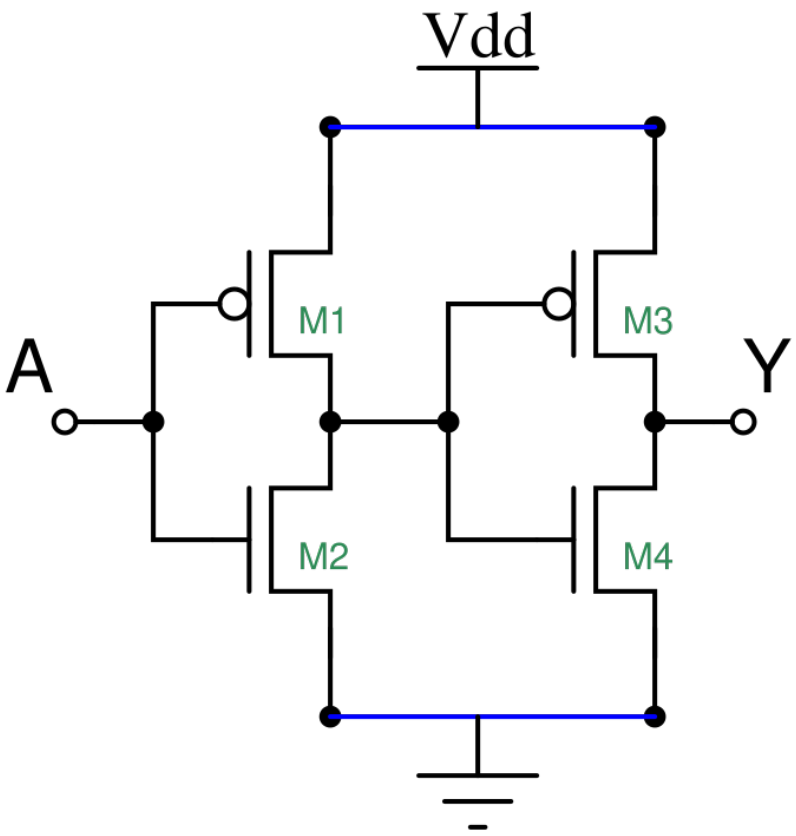

Figure 1: Circuit Diagram of Buffer

Index	Type of MOS	W (µm)	L (µm)
X0	n-MOS	0.42	0.15
X1	n-MOS	0.42	0.15
X2	p-MOS	1.27	0.15
X3	p-MOS	0.42	0.15

Table 1: MOSFET Parameters

Layout

Following is the layout, with the dimensions mentioned in the terminal for magic.

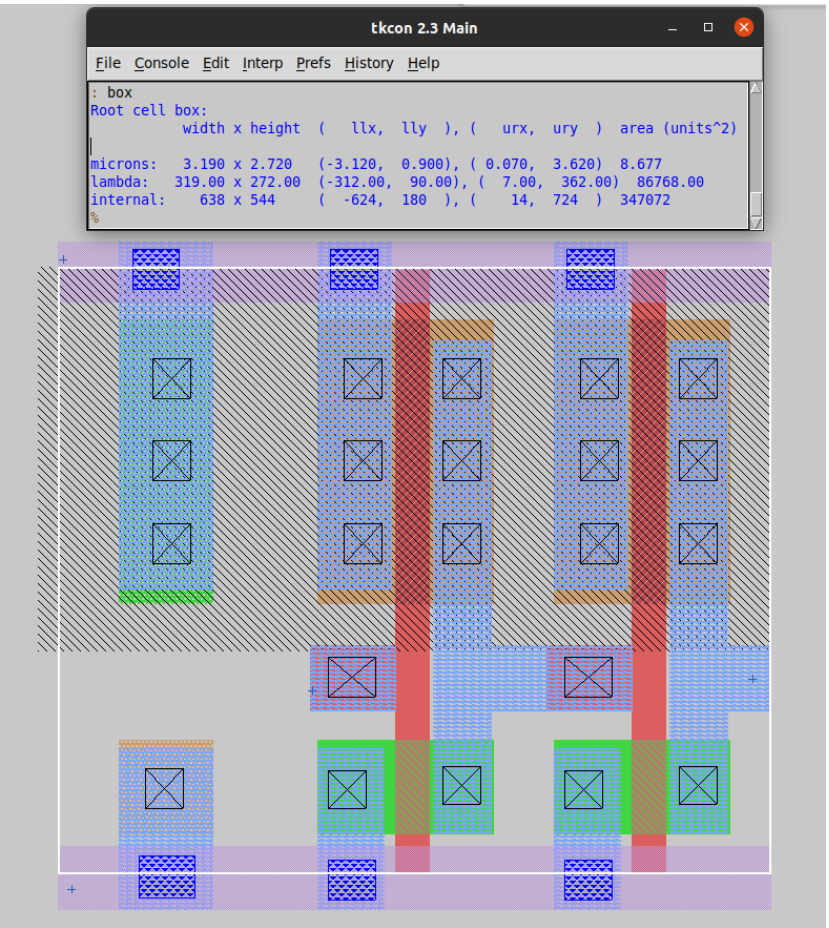

Figure 2: Layout for Bufffer with dimensions

PEX Netlist

Following is the netlist with parasitics generated using magic.

```
* NGSPICE file created from NOR.ext - technology: sky130A

.subckt BUFX1 gnd A Z vdd
X0 a_n294_216# A Gnd Gnd sky130_fd_pr__nfet_01v8 ad=0.1218 pd=1.42 as=0.147
ps=1.54 w=0.42 l=0.15
X1 Z a_n294_216# Vdd Vdd sky130_fd_pr__pfet_01v8 ad=0.3683 pd=3.12 as=0.4445
ps=3.24 w=1.27 l=0.15
X2 Z a_n294_216# Gnd Gnd sky130_fd_pr__nfet_01v8 ad=0.1218 pd=1.42 as=0.147
ps=1.54 w=0.42 l=0.15
X3 a_n294_216# A Vdd Vdd sky130_fd_pr__pfet_01v8 ad=0.3683 pd=3.12 as=0.4445
ps=3.24 w=1.27 l=0.15
C0 A a_n294_216# 0.07097f
C1 Z a_n294_216# 0.060637f
C2 Vdd A 0.116746f
C3 Z Vdd 0.117794f
C4 Vdd a_n294_216# 0.300854f
C5 Z Gnd 0.168793f
C6 A Gnd 0.214202f
C7 Vdd Gnd 0.999662f
```

```
C8 a_n294_216# Gnd 0.332985f
.ends
```

DRC and LVS Check

1.4.1 DRC Check:

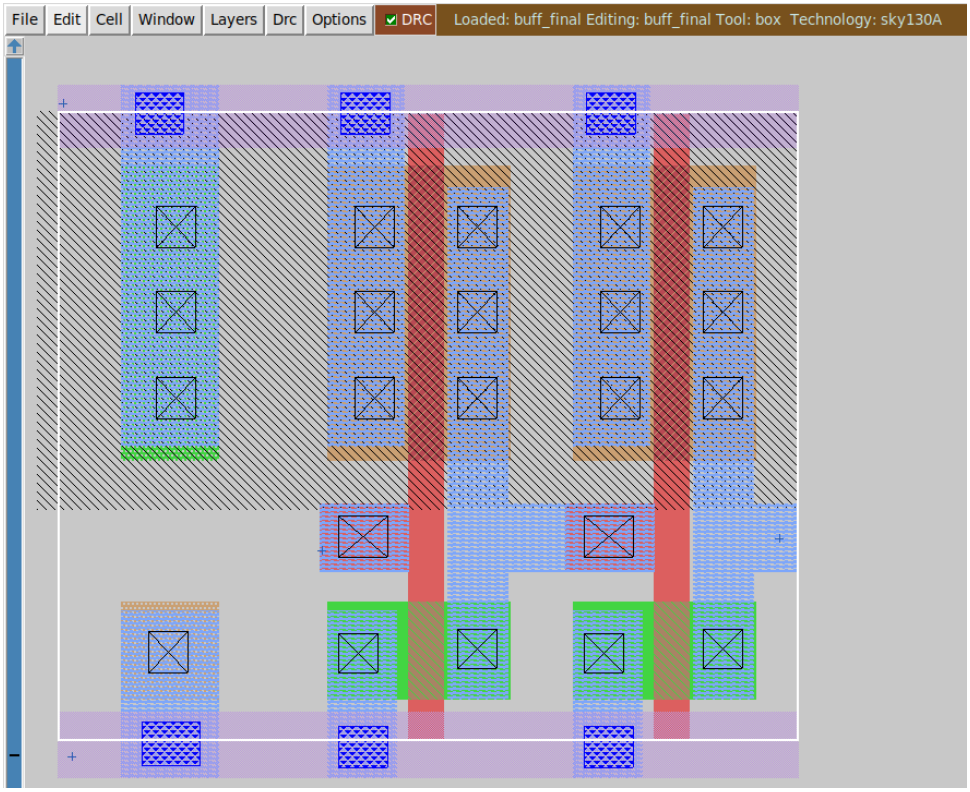

Figure 3: DRC Clean Proof

1.4.2 LVS Check:

```
jainam@jainam-HP-Laptop-15s-fq5xxx:~/new_pdk_sky/course_project1/buff_final$ netgen -batch lvs "buff_final.
spice" "buff_schematic.spice" /usr/local/share/pdk/sky130A/libs.tech/netgen/sky130A_setup.tcl | tail -n 22
Contents of circuit 1:  Circuit: 'buff_final.spice'
Circuit buff_final.spice contains 13 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:   2
  Class: c                       instances:   9
  Class: sky130_fd_pr__pfet_01v8 instances:   2
Circuit contains 5 nets.
Contents of circuit 2:  Circuit: 'buff_schematic.spice'
Circuit buff_schematic.spice contains 13 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:   2
  Class: c                       instances:   9
  Class: sky130_fd_pr__pfet_01v8 instances:   2
Circuit contains 5 nets.

Circuit 1 contains 13 devices, Circuit 2 contains 13 devices.
Circuit 1 contains 5 nets,    Circuit 2 contains 5 nets.


Final result:
Circuits match uniquely.
.
Logging to file "comp.out" disabled
LVS Done.
```

Figure 4: LVS Clean Proof

Waveforms

1.5.1 Rise and Fall Time

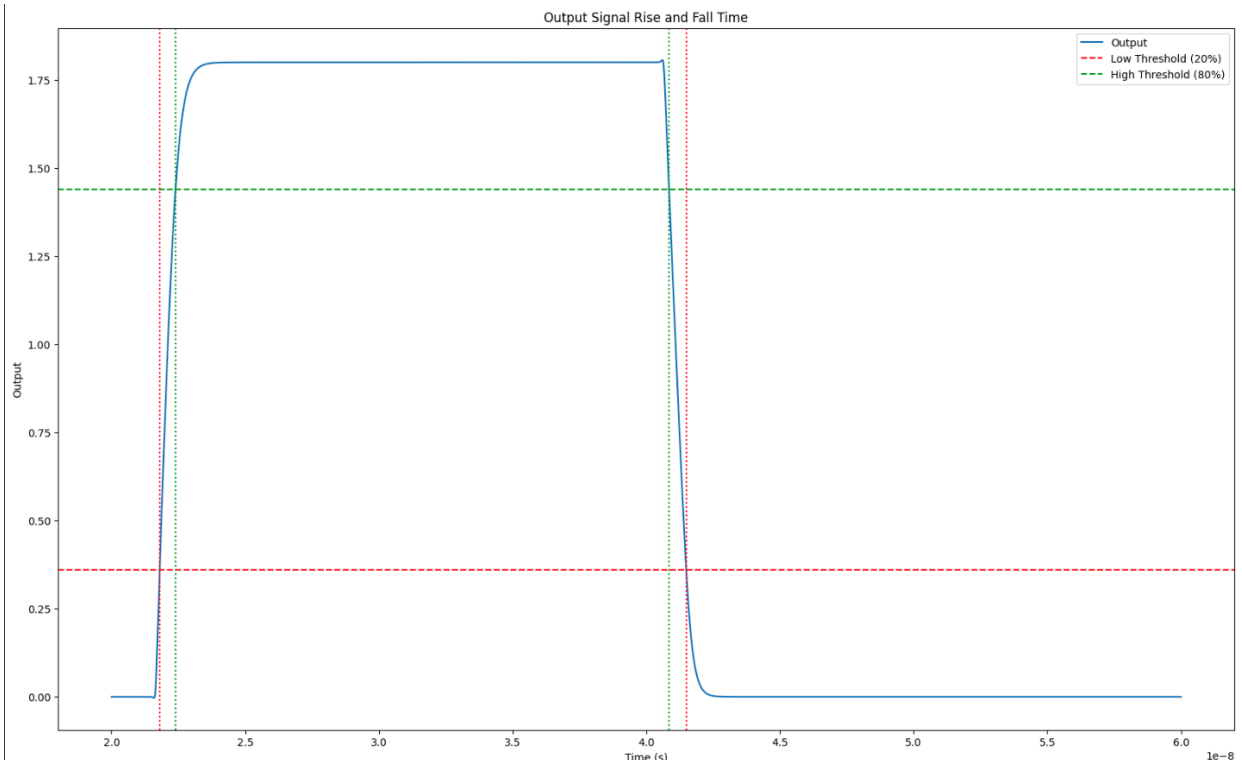

Figure 5: Rise and Fall Time

1.5.2 Propagation Delay

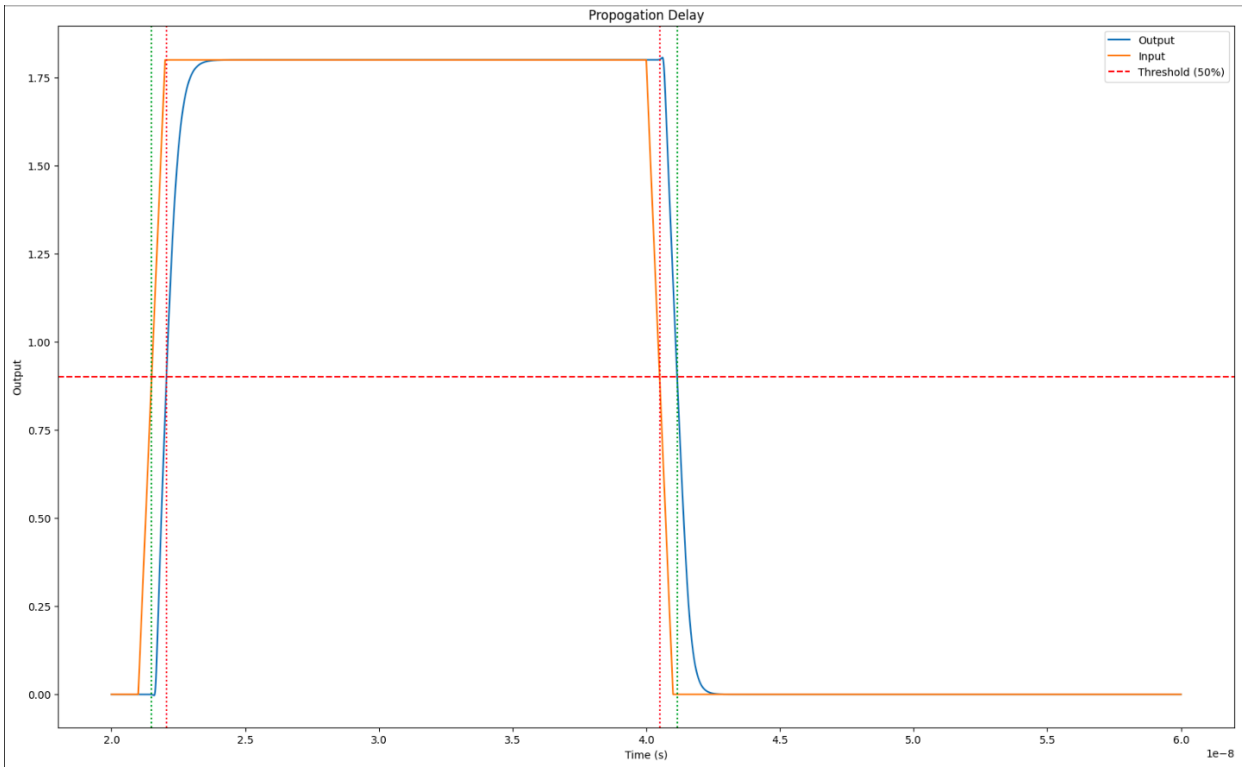

Figure 6: Propagation delay

Input Capacitances

Input Pins	Rise Cap (fF)	Fall Cap (fF)	Average Cap (fF)
A	2.317	2.281	2.30

Table 2: Input Pin Capacitances

Timing Tables

	10 ps	100 ps	1000 ps
0.5 fF	14.5 ps	14.7 ps	30.0
10 fF	67.4 ps	67.3 ps	73.7
100 fF	592.2 ps	592.2 ps	592.8

Table 3: Output Rise Transitions (in ns) [Input slew vs output capacitance]. Related pin A

	10 ps	100 ps	1000 ps
0.5 fF	14.5 ps	14.7 ps	27.8
10 fF	72.7 ps	72.8 ps	79.3
100 fF	641.3 ps	641.2 ps	642.2

Table 4: Output Fall Transitions (in ns) [Input slew vs output capacitance]. Related pin A

	10 ps	100 ps	1000 ps
0.5 fF	47.1 ps	65.6 ps	145.1
10 fF	87.6 ps	106.1 ps	196.8
100 fF	446.0 ps	464.6 ps	556.4

Table 5: Cell Rise Delay (in ns) [Input slew vs output capacitance]. Related pin A

	10 ps	100 ps	1000 ps
0.5 fF	46.1 ps	67.0 ps	157.6
10 fF	96.0 ps	117.6 ps	217.3
100 fF	532.0 ps	554.1 ps	656.3

Table 6: Cell Fall Delay (in ns) [Input slew vs output capacitance]. Related pin A

Power Tables

Condition (A)	Power (nW)
0	0.11634
1	0.11634

Table 7: Static Power (all possible input combinations of A)

	10 ps	100 ps	1000 ps
0.5 fF	88.39	24.05	5.59
10 fF	162.00	96.08	35.71
100 fF	170.29	173.12	36.79

Table 8: Dynamic Power Table (i) Rise Power (in uW) [Input slew vs output capacitance]. Related pin A

	10 ps	**100 ps**	**1000 ps**
0.5 fF	94.92	66.04	15.22
10 fF	96.00	67.36	15.60
100 fF	120.96	68.81	6.50

Table 9: Dynamic Power Table (ii) Fall Power (in uW) [Input slew vs output capacitance]. Related pin A

2 Cell 2 - DFXTP

Circuit Diagram and MOS sizing

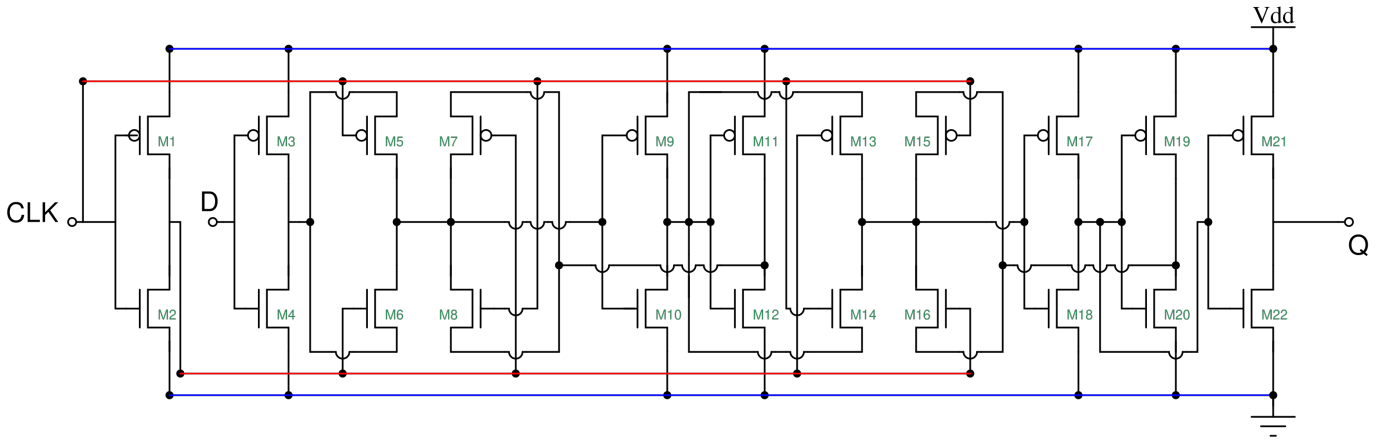

Figure 7: Circuit Diagram of Positive Edge Data Flip-Flop

Index	Type of MOS	W (µm)	L (µm)
X0	n-MOS	0.42	0.15
X1	n-MOS	0.42	0.15
X2	p-MOS	1.27	0.15
X3	n-MOS	0.42	0.15
X4	p-MOS	1.27	0.15
X5	n-MOS	0.42	0.15
X6	p-MOS	1.27	0.15
X7	p-MOS	1.27	0.15
X8	n-MOS	0.42	0.15
X9	n-MOS	0.42	0.15
X10	n-MOS	0.42	0.15
X11	n-MOS	0.42	0.15
X12	n-MOS	0.42	0.15
X13	p-MOS	1.27	0.15
X14	p-MOS	1.27	0.15
X15	n-MOS	0.42	0.15
X16	n-MOS	0.42	0.15
X17	p-MOS	1.27	0.15
X18	p-MOS	1.27	0.15
X19	p-MOS	1.27	0.15
X20	p-MOS	1.27	0.15
X21	p-MOS	1.27	0.15

Table 10: MOSFET Parameters

(NOTE: The indexes of MOSFETS are according to that generated in the pex file)

Layout

Following is the layout, with the dimensions mentioned in the terminal for magic. Note, the terminal shows 2.71um, but in reality it's 2.72um only. It shows 2.71 because of the grid length quantization constraints:

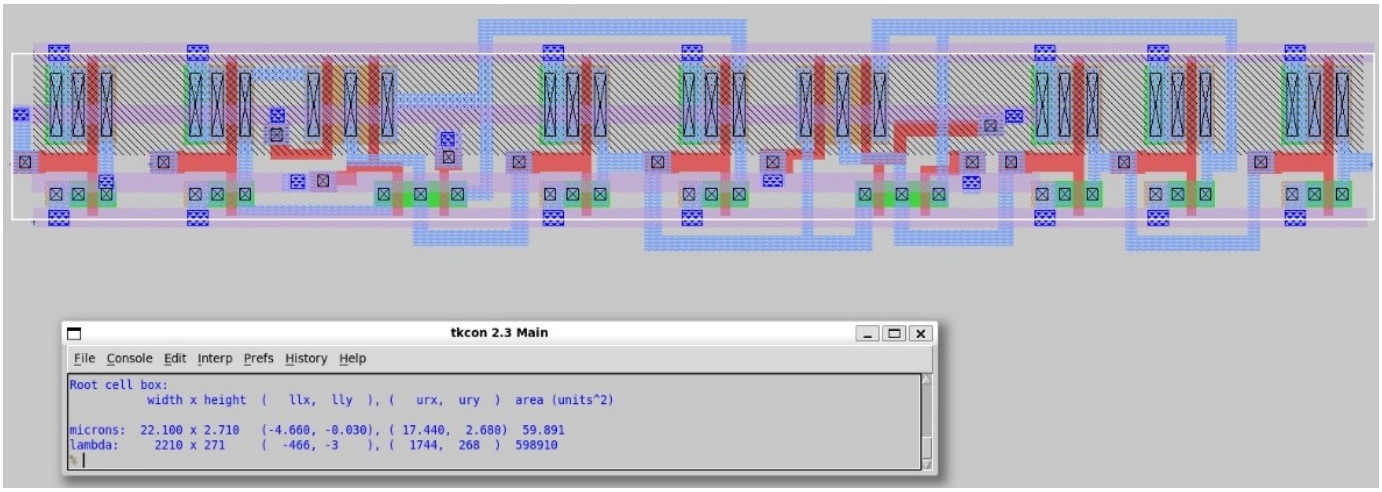

Figure 8: Layout for DFF with dimensions

PEX Netlist

```
* NGSPICE file created from dff.ext - technology: sky130A
.lib /usr/local/share/pdk/sky130A/libs.tech/ngspice/sky130.lib.spice tt
.subckt dff D clk Q vss vdd
X0 a_927_120# a_1272_18# vss vss sky130_fd_pr__nfet_01v8 ad=0.126 pd=1.44 as=0.126
ps=1.44 w=0.42 l=0.15
**devattr s=1260,144 d=1260,144
X1 a_927_120# a_n327_18# a_852_120# vss sky130_fd_pr__nfet_01v8 ad=0.126 pd=1.44
as=0.126 ps=1.02 w=0.42 l=0.15
**devattr s=1260,102 d=1260,144
X2 a_n327_18# clk vdd vdd sky130_fd_pr__pfet_01v8 ad=0.381 pd=3.14 as=0.381
ps=3.14 w=1.27 l=0.15
**devattr s=3810,314 d=3810,314
X3 a_852_120# clk a_474_18# vss sky130_fd_pr__nfet_01v8 ad=0.126 pd=1.02 as=0.126
ps=1.44 w=0.42 l=0.15
**devattr s=1260,144 d=1260,102
X4 a_927_120# clk a_852_120# vdd sky130_fd_pr__pfet_01v8 ad=0.381 pd=3.14 as=0.381
ps=1.87 w=1.27 l=0.15
**devattr s=3810,187 d=3810,314
X5 a_n102_18# D vss vss sky130_fd_pr__nfet_01v8 ad=0.126 pd=1.44 as=0.126
ps=1.44 w=0.42 l=0.15
**devattr s=1260,144 d=1260,144
X6 a_1272_18# a_852_120# vdd vdd sky130_fd_pr__pfet_01v8 ad=0.381 pd=3.14 as=0.381
ps=3.14 w=1.27 l=0.15
**devattr s=3810,314 d=3810,314
X7 a_n102_18# D vdd vdd sky130_fd_pr__pfet_01v8 ad=0.381 pd=3.14 as=0.381
ps=3.14 w=1.27 l=0.15
**devattr s=3810,314 d=3810,314
X8 a_n327_18# clk vss vss sky130_fd_pr__nfet_01v8 ad=0.126 pd=1.44 as=0.126
ps=1.44 w=0.42 l=0.15
**devattr s=1260,144 d=1260,144
X9 a_1272_18# a_852_120# vss vss sky130_fd_pr__nfet_01v8 ad=0.126 pd=1.44 as=0.126
```

```
ps=1.44 w=0.42 l=0.15
**devattr s=1260,144 d=1260,144
X10 a_54_120# a_n327_18# a_n102_18# vss sky130_fd_pr__nfet_01v8 ad=0.126 pd=1.02
as=0.126 ps=1.44 w=0.42 l=0.15
**devattr s=1260,144 d=1260,102
X11 a_129_120# clk a_54_120# vss sky130_fd_pr__nfet_01v8 ad=0.126 pd=1.44 as=0.126
ps=1.02 w=0.42 l=0.15
**devattr s=1260,102 d=1260,144
X12 a_474_18# a_54_120# vss vss sky130_fd_pr__nfet_01v8 ad=0.126 pd=1.44 as=0.126
ps=1.44 w=0.42 l=0.15
**devattr s=1260,144 d=1260,144
X13 a_129_120# a_474_18# vdd vdd sky130_fd_pr__pfet_01v8 ad=0.381 pd=3.14 as=0.381
ps=3.14 w=1.27 l=0.15
**devattr s=3810,314 d=3810,314
X14 a_927_120# a_1272_18# vdd vdd sky130_fd_pr__pfet_01v8 ad=0.381 pd=3.14 as=0.381
ps=3.14 w=1.27 l=0.15
**devattr s=3810,314 d=3810,314
X15 a_129_120# a_474_18# vss vss sky130_fd_pr__nfet_01v8 ad=0.126 pd=1.44 as=0.126
ps=1.44 w=0.42 l=0.15
**devattr s=1260,144 d=1260,144
X16 Q a_1272_18# vss vss sky130_fd_pr__nfet_01v8 ad=0.126 pd=1.44 as=0.126
ps=1.44 w=0.42 l=0.15
**devattr s=1260,144 d=1260,144
X17 a_852_120# a_n327_18# a_474_18# vdd sky130_fd_pr__pfet_01v8 ad=0.381 pd=1.87
as=0.381 ps=3.14 w=1.27 l=0.15
**devattr s=3810,314 d=3810,187
X18 a_474_18# a_54_120# vdd vdd sky130_fd_pr__pfet_01v8 ad=0.381 pd=3.14 as=0.381
ps=3.14 w=1.27 l=0.15
**devattr s=3810,314 d=3810,314
X19 Q a_1272_18# vdd vdd sky130_fd_pr__pfet_01v8 ad=0.381 pd=3.14 as=0.381
ps=3.14 w=1.27 l=0.15
**devattr s=3810,314 d=3810,314
X20 a_129_120# a_n327_18# a_54_120# vdd sky130_fd_pr__pfet_01v8 ad=0.381 pd=3.14
as=0.381 ps=1.87 w=1.27 l=0.15
**devattr s=3810,187 d=3810,314
X21 a_54_120# clk a_n102_18# vdd sky130_fd_pr__pfet_01v8 ad=0.381 pd=1.87 as=0.381
ps=3.14 w=1.27 l=0.15
**devattr s=3810,314 d=3810,187
C0 Q vdd 0.121471f
C1 clk a_852_120# 0.149059f
C2 D clk 0.039876f
C3 clk a_927_120# 0.167326f
C4 a_852_120# a_927_120# 0.16653f
C5 clk a_474_18# 0.120984f
C6 a_852_120# a_474_18# 0.168917f
C7 clk a_1272_18# 0.002125f
C8 a_927_120# a_474_18# 1.16e-19
C9 clk a_n327_18# 1.04126f
C10 a_852_120# a_1272_18# 0.064204f
C11 a_1272_18# a_927_120# 0.142062f
C12 a_n327_18# a_852_120# 0.215813f
C13 D a_n327_18# 0.052048f
C14 a_n327_18# a_927_120# 0.108192f
```

```
C15 a_1272_18# a_474_18# 5.4e-19
C16 a_n327_18# a_474_18# 0.261757f
C17 Q clk 1.06e-19
C18 a_n327_18# a_1272_18# 0.002477f
C19 a_n102_18# a_129_120# 4.41e-20
C20 vdd a_129_120# 0.620602f
C21 Q a_927_120# 0.002157f
C22 vdd a_n102_18# 0.185954f
C23 a_54_120# a_129_120# 0.230387f
C24 Q a_1272_18# 0.04166f
C25 a_54_120# a_n102_18# 0.140363f
C26 vdd a_54_120# 0.179205f
C27 Q a_n327_18# 6.22e-20
C28 clk a_129_120# 0.259362f
C29 a_852_120# a_129_120# 1.44e-19
C30 D a_129_120# 2.9e-20
C31 clk a_n102_18# 0.214076f
C32 clk vdd 1.94632f
C33 a_927_120# a_129_120# 0.009133f
C34 vdd a_852_120# 0.170864f
C35 D a_n102_18# 0.044298f
C36 D vdd 0.142067f
C37 vdd a_927_120# 0.68069f
C38 a_474_18# a_129_120# 0.13261f
C39 clk a_54_120# 0.146185f
C40 vdd a_474_18# 0.352639f
C41 D a_54_120# 4.4e-20
C42 a_n327_18# a_129_120# 0.140951f
C43 vdd a_1272_18# 0.466938f
C44 a_54_120# a_474_18# 0.058552f
C45 a_n327_18# a_n102_18# 0.196172f
C46 vdd a_n327_18# 0.434253f
C47 a_n327_18# a_54_120# 0.18053f
C48 Q vss 0.18321f
C49 D vss 0.281218f
C50 clk vss 0.84449f
C51 vdd vss 5.43907f
C52 a_927_120# vss 0.494246f
C53 a_129_120# vss 0.445621f
C54 a_n102_18# vss 0.332164f
C55 a_1272_18# vss 1.0964f
C56 a_852_120# vss 0.614379f
C57 a_474_18# vss 0.958008f
C58 a_54_120# vss 0.635279f
C59 a_n327_18# vss 2.34082f
.ends
.end
```

DRC and LVS Check

2.4.1 DRC Check:

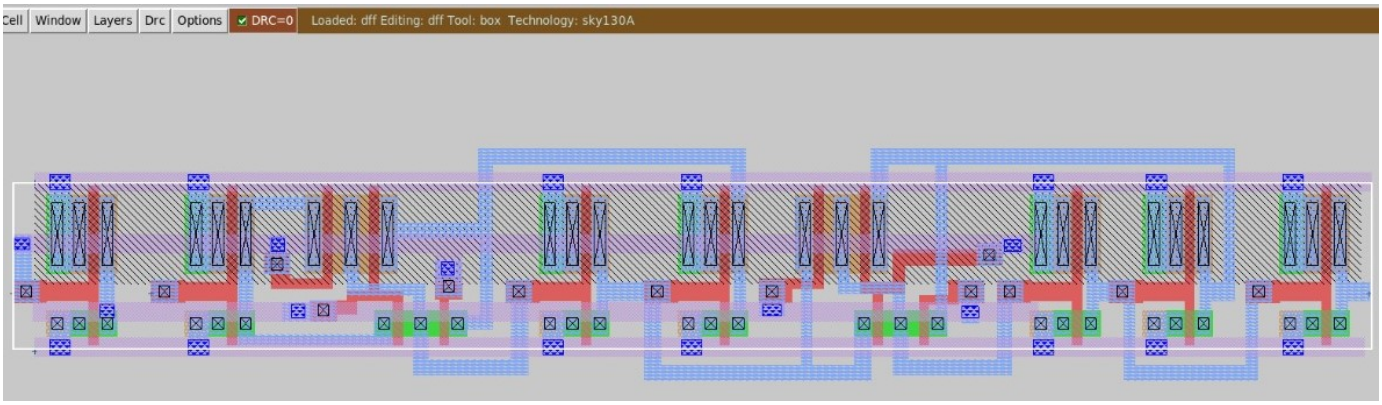

Figure 9: DRC Clean Proof

2.4.2 LVS Check:

```
Contents of circuit 1:  Circuit: 'dff'
Circuit dff contains 22 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:  11
  Class: sky130_fd_pr__pfet_01v8 instances:  11
Circuit contains 13 nets.
Contents of circuit 2:  Circuit: 'dff'
Circuit dff contains 22 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:  11
  Class: sky130_fd_pr__pfet_01v8 instances:  11
Circuit contains 13 nets.

Circuit 1 contains 22 devices, Circuit 2 contains 22 devices.
Circuit 1 contains 13 nets,    Circuit 2 contains 13 nets.


Final result:
Circuits match uniquely.
.
Logging to file "comp.out" disabled
LVS Done.
```

Figure 10: LVS Clean Proof

Waveforms

2.5.1 Setup Time

Rise setup time plot for input and clock skew both as 10ps (piecewise linear function was used to generate clk and D waveforms):

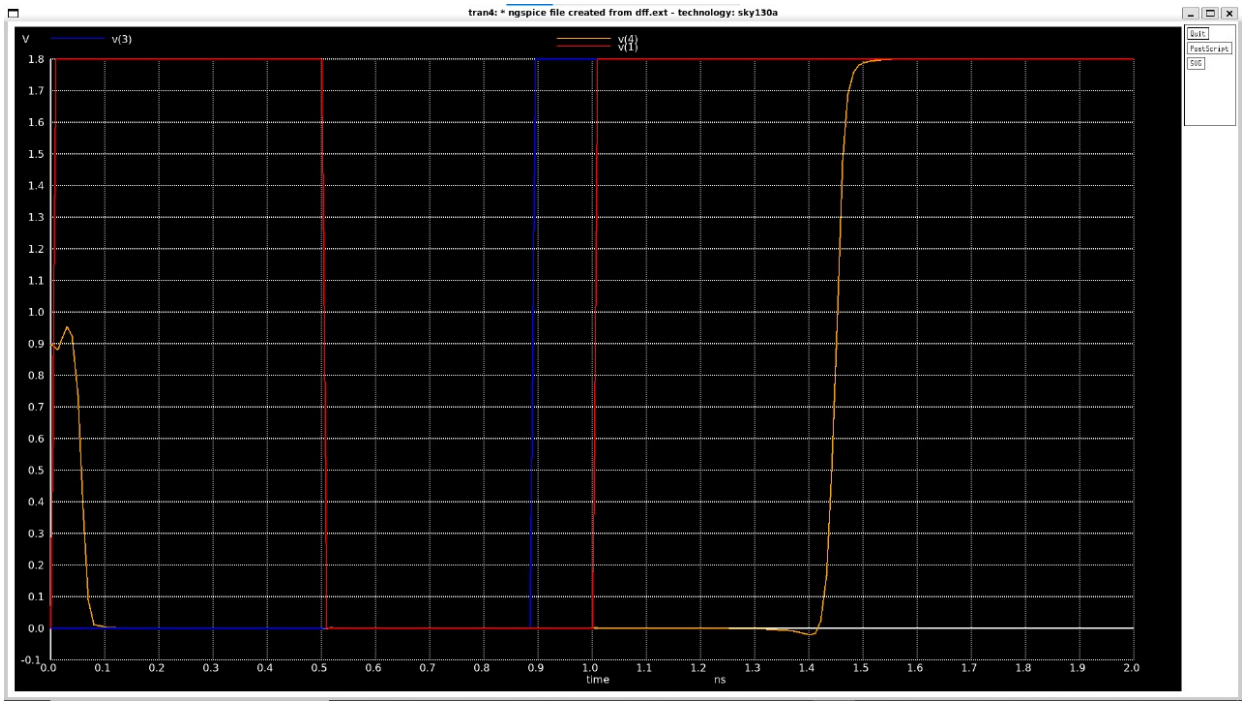

Figure 11: Setup time for 10ps slew for D and clk both

2.5.2 Hold Time

Fall hold time for slew as 1000ps for both input and clk(same legend as setup time plot):

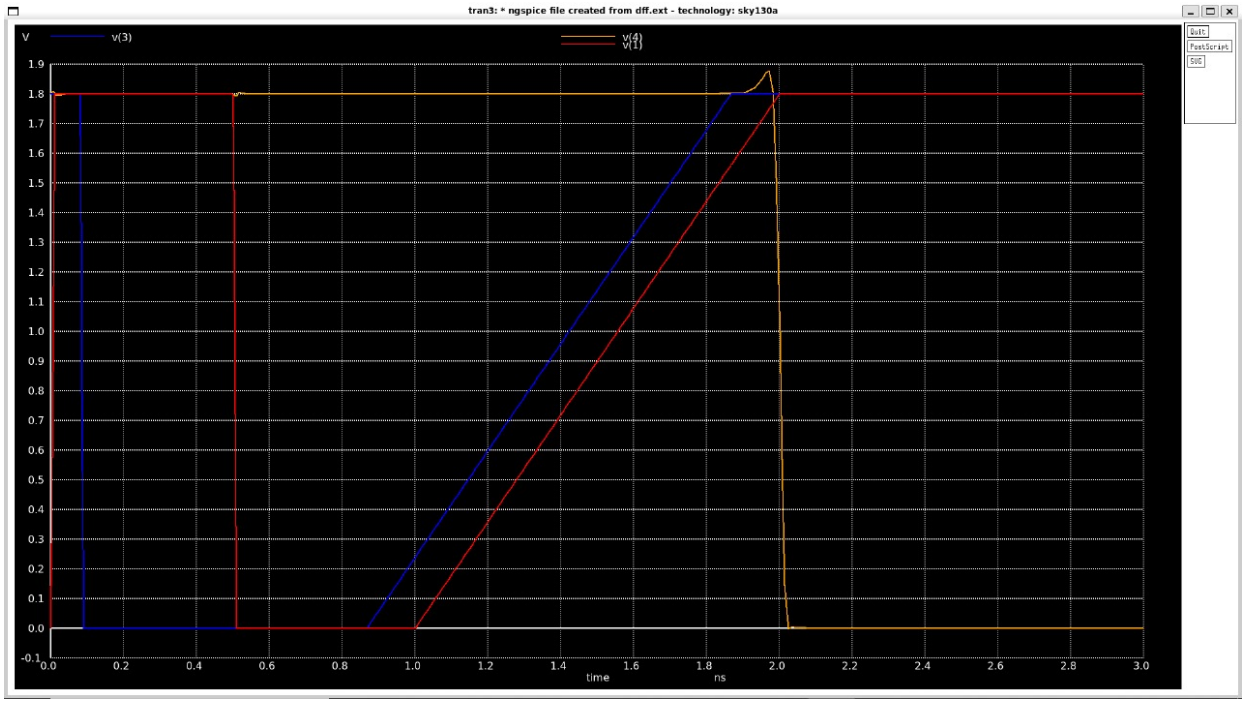

Figure 12: Hold time for 1000ps slew for D and clk

Legend:
Red - clk
Blue - D
Yellow - Q
(legend is same for hold time plot also)
NOTE: Setup and Hold times were measured as respective differences in time of D and CLK when the levels reach 50% of the vdd value. Hence, in some of the cases, values come out to be negative for the parameters.

2.5.3 Rise Time

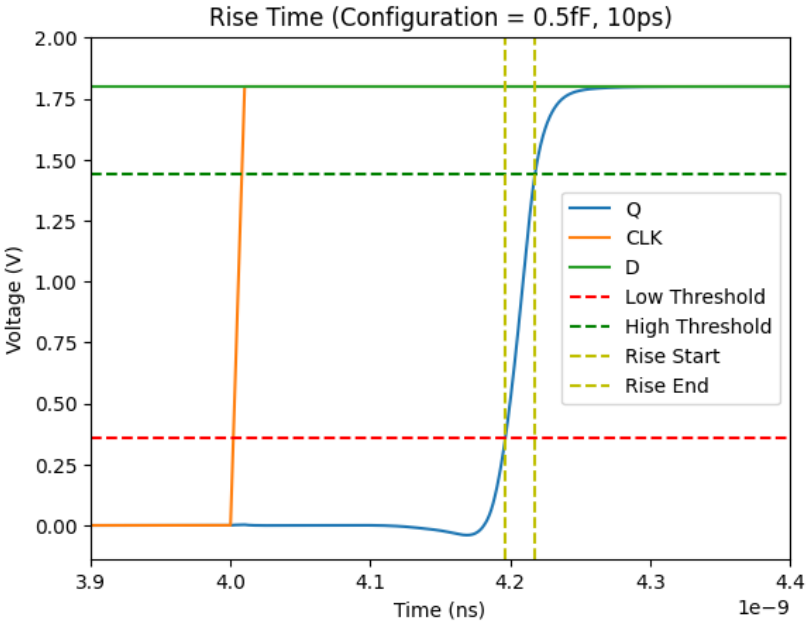

Figure 13: Rise Time

2.5.4 Fall Time

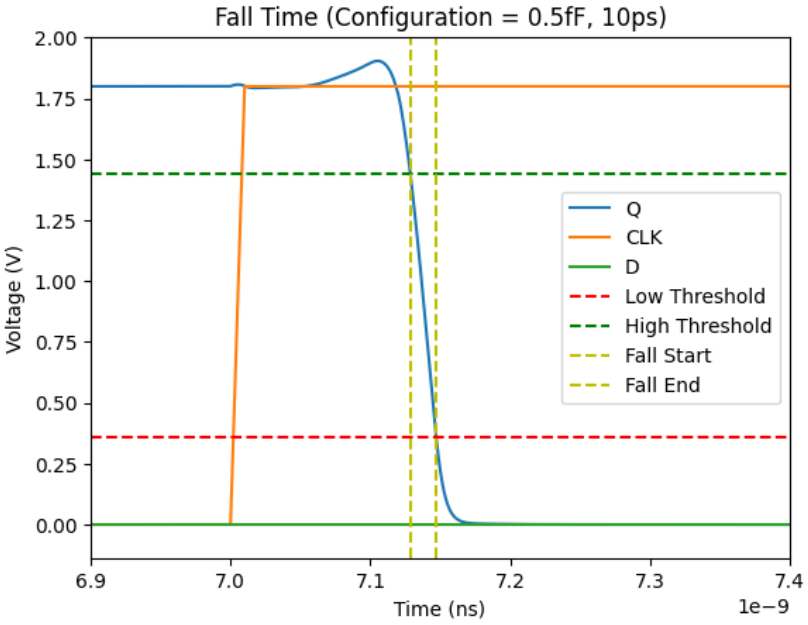

Figure 14: Fall Time

2.5.5 Propagation Delay

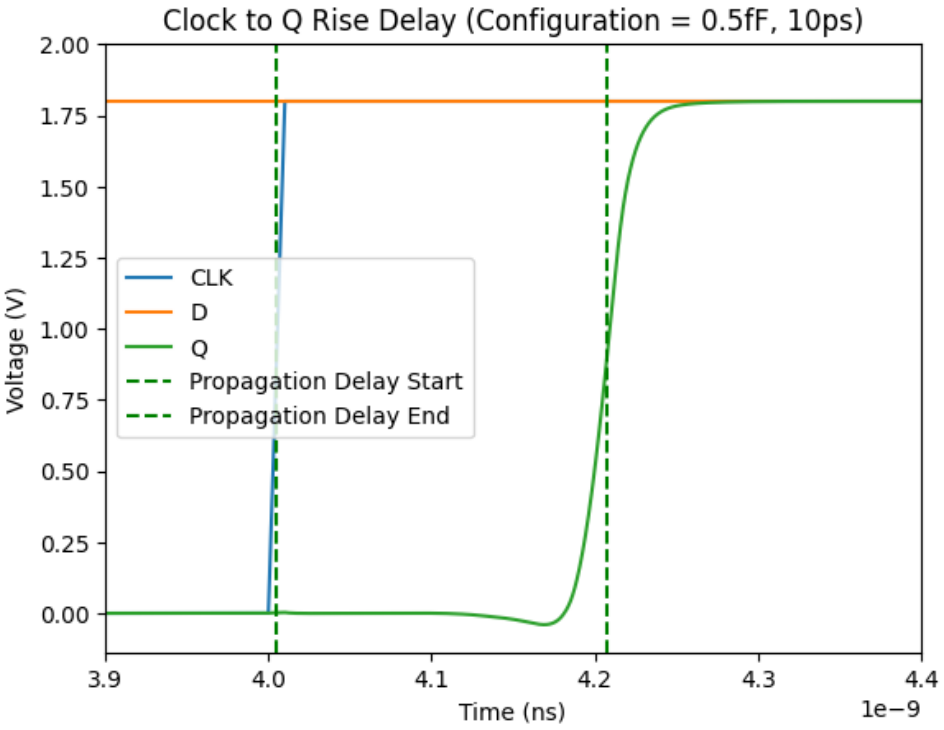

Figure 15: Propagation Delay - Rise

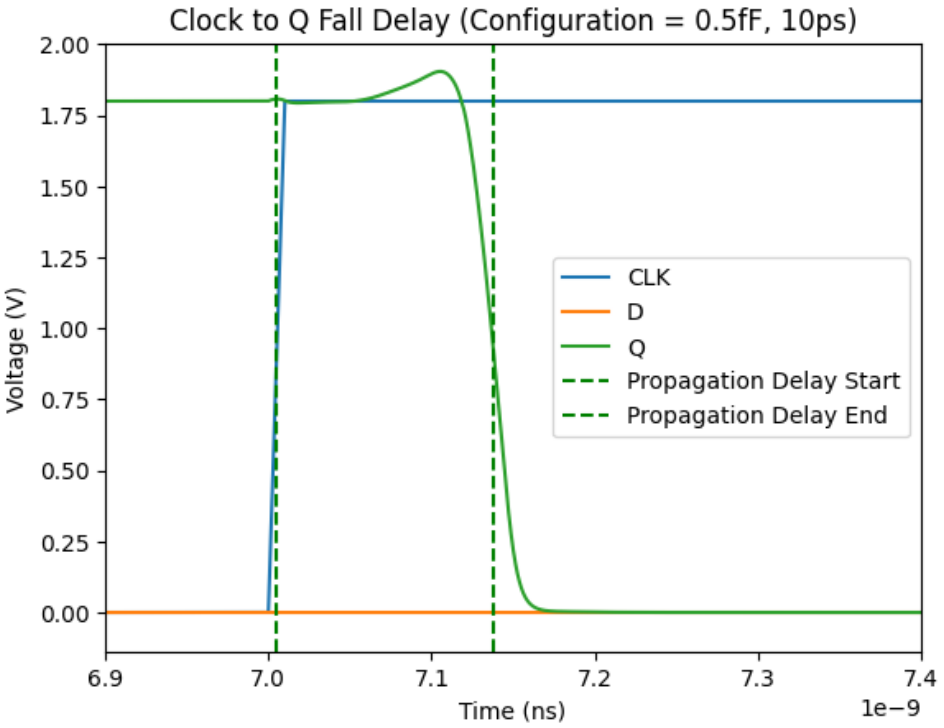

Figure 16: Propagation Delay - Fall

Input Capacitances

Input Pins	Rise Cap (pF)	Fall Cap (pF)	Average Cap (pF)
D	$2.4978*10^{-3}$	$2.4852*10^{-3}$	$2.4915*10^{-3}$
CLK	$9.3546*10^{-3}$	$9.3358*10^{-3}$	$9.3452*10^{-3}$

Table 11: Input Pin Capacitances

Timing Table

	10 ps	1000 ps
10 ps	0.115	-0.008
1000 ps	0.282	0.140

Table 12: Set-up Time Table (i) Rise Constraint (in ns) [Input slew vs CLK slew]

	10 ps	1000 ps
10 ps	0.11	0.191
1000 ps	0.28	0.353

Table 13: Set-up Time Table (ii) Fall Constraint (in ns) [Input slew vs CLK slew]

	10 ps	1000 ps
10 ps	-0.069	-0.172
1000 ps	-0.228	-0.334

Table 14: Hold Time Table (i) Rise Constraint (in ns) [Input slew vs CLK slew]

	10 ps	1000 ps
10 ps	-0.062	0.01
1000 ps	-0.212	-0.133

Table 15: Hold Time Table (ii) Fall Constraint (in ns) [Input slew vs CLK slew]

	10 ps	100 ps	1000 ps
0.5 fF	$21.15*10^{-3}$	$21.15*10^{-3}$	$21.1*10^{-3}$
10 fF	$71.4*10^{-3}$	$71.4*10^{-3}$	$71.4*10^{-3}$
100 fF	$592.2*10^{-3}$	$592.2*10^{-3}$	$592.2*10^{-3}$

Table 16: Transition Time Table (i) Output Rise Transitions (in ns) [Input slew vs output capacitance]. Related pin D:

	10 ps	100 ps	1000 ps
0.5 fF	$18.46*10^{-3}$	$18.50*10^{-3}$	$19.4*10^{-3}$
10 fF	$75.96*10^{-3}$	$75.98*10^{-3}$	$76.4*10^{-3}$
100 fF	$641.3*10^{-3}$	$641.3*10^{-3}$	$641.3*10^{-3}$

Table 17: Transition Time Table (ii) Output Fall Transitions (in ns) [Input slew vs output capacitance]. Related pin D:

	10 ps	100 ps	1000 ps
0.5 fF	$202.48*10^{-3}$	$220.47*10^{-3}$	$374.8*10^{-3}$
10 fF	$249.29*10^{-3}$	$267.28*10^{-3}$	$421.6*10^{-3}$
100 fF	$608.8*10^{-3}$	$626.8*10^{-3}$	$781.2*10^{-3}$

Table 18: CLK-to-Q Delay Time Table (i) Cell Rise Delay (in ns) [Input slew vs output capacitance]. Related pin D:

	10 ps	100 ps	1000 ps
0.5 fF	$133.33*10^{-3}$	$150.97*10^{-3}$	$269.3*10^{-3}$
10 fF	$188.32*10^{-3}$	$206.02*10^{-3}$	$324.8*10^{-3}$
100 fF	$625.5*10^{-3}$	$643.2*10^{-3}$	$762.3*10^{-3}$

Table 19: CLK-to-Q Delay Time Table (ii) Cell Fall Delay (in ns) [Input slew vs output capacitance]. Related pin D:

Power Tables

Condition (CLK D)	Power (nW)
00	$380.91*10^{-3}$
01	$380.95*10^{-3}$
10	$490.58*10^{-3}$
11	$490.59*10^{-3}$

Table 20: Static Power (all possible input combinations of CLK and D)

	10 ps	100 ps	1000 ps
0.5 fF	$115.83*10^{3}$	$84.32*10^{3}$	$30.13*10^{3}$
10 fF	$198.62*10^{3}$	$143.17*10^{3}$	$56.03*10^{3}$
100 fF	$232.94*10^{3}$	$195.45*10^{3}$	$142.36*10^{3}$

Table 21: Dynamic Power Table (i) Rise Power (in nW) [Clk slew vs output capacitance]. Related pin D:

	10 ps	100 ps	1000 ps
0.5 fF	$112.37*10^{3}$	$69.24*10^{3}$	$20.52*10^{3}$
10 fF	$108.85*10^{3}$	$76.71*10^{3}$	$20.33*10^{3}$
100 fF	$46.39*10^{3}$	$42.29*10^{3}$	$18.65*10^{3}$

Table 22: Dynamic Power Table (ii) Fall Power (in nW) [Clk slew vs output capacitance]. Related pin D:

NOTE: We have changed the slew for clk rather than input while calculating the dynamic power as the transition in the state takes place at the rising edge of the clk and not the edge of input. Hence, it makes sense to change the slew of the rising edge of the clk while calculating the dynamic power.

3 Cell 3 - NOR2B

Circuit Diagram and MOS Sizing

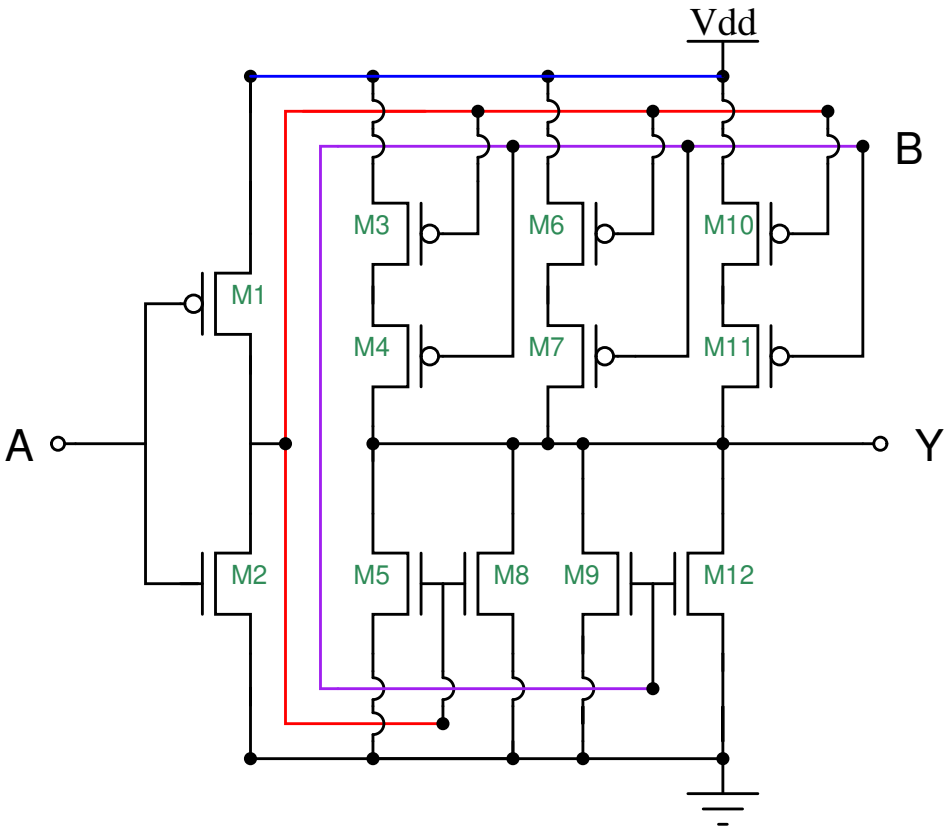

Figure 17: Circuit Diagram of NOR

Index	Type of MOS	W (µm)	L (µm)
xn1	p-MOS	1.27	0.15
xn2	p-MOS	1.27	0.15
xn3	p-MOS	0.66	0.15
xn4	p-MOS	1.27	0.15
xn5	p-MOS	1.27	0.15
xn6	p-MOS	0.66	0.15
xn7	n-MOS	0.42	0.15
xn8	n-MOS	0.42	0.15
xn9	n-MOS	0.42	0.15
xn10	n-MOS	0.42	0.15
x11	p-MOS	1.27	0.15
x12	n-MOS	0.42	0.15

Table 23: MOSFET Parameters

Layout

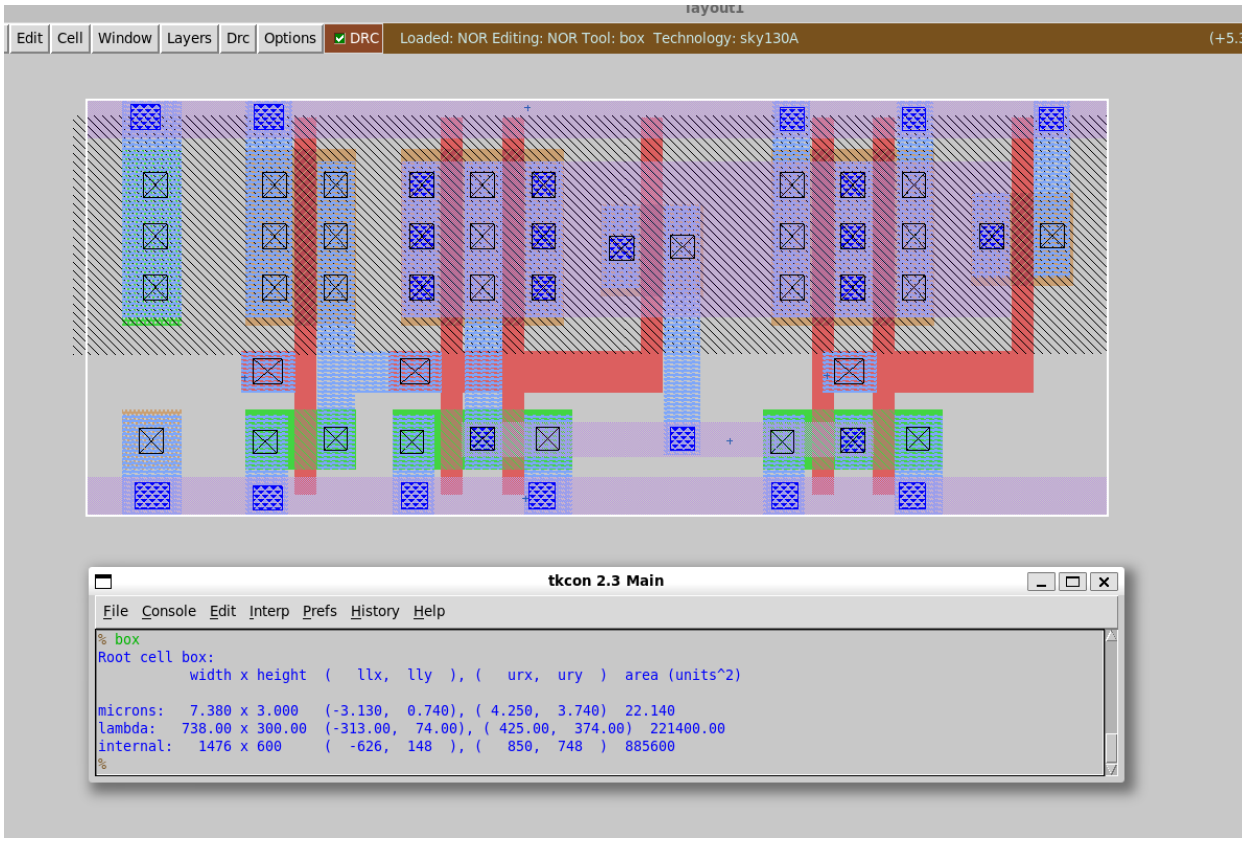

Figure 18: Layout for NOR with dimensions

PEX Netlist

```
* NGSPICE file created from NOR.ext - technology: sky130A

X0 a_n170_422# B vdd vdd sky130_fd_pr__pfet_01v8 ad=0.295215 pd=2.611438 as=0.38995
ps=3.233244 w=1.27 l=0.15
X1 a_n294_216# A vss vss sky130_fd_pr__nfet_01v8 ad=0.1218 pd=1.42 as=0.147
ps=1.54 w=0.42 l=0.15
X2 Y a_n294_216# a_n170_422# vdd sky130_fd_pr__pfet_01v8 ad=0.222131
pd=1.992312 as=0.295215 ps=2.611438 w=1.27 l=0.15
X3 vss B Y vss sky130_fd_pr__nfet_01v8 ad=0.147 pd=1.54 as=0.0609
ps=0.71 w=0.42 l=0.15
X4 a_n170_422# a_n294_216# Y vdd sky130_fd_pr__pfet_01v8 ad=0.295215
pd=2.611438 as=0.222131 ps=1.992312 w=1.27 l=0.15
X5 vdd B a_n170_422# vdd sky130_fd_pr__pfet_01v8 ad=0.202651 pd=1.680268 as=0.153419
ps=1.357125 w=0.66 l=0.15
X6 Y B vss vss sky130_fd_pr__nfet_01v8 ad=0.0609 pd=0.71 as=0.147
ps=1.54 w=0.42 l=0.15
X7 Y a_n294_216# vss vss sky130_fd_pr__nfet_01v8 ad=0.0609 pd=0.71 as=0.147
ps=1.54 w=0.42 l=0.15
X8 a_n294_216# A vdd vdd sky130_fd_pr__pfet_01v8 ad=0.3683 pd=3.12 as=0.38995
ps=3.233244 w=1.27 l=0.15
X9 vdd B a_n170_422# vdd sky130_fd_pr__pfet_01v8 ad=0.38995 pd=3.233244 as=0.295215
ps=2.611438 w=1.27 l=0.15
X10 vss a_n294_216# Y vss sky130_fd_pr__nfet_01v8 ad=0.147 pd=1.54 as=0.0609
ps=0.71 w=0.42 l=0.15
```

```
X11 Y a_n294_216# a_n170_422# vdd sky130_fd_pr__pfet_01v8 ad=0.115438
pd=1.035375 as=0.153419 ps=1.357125 w=0.66 l=0.15
C0 vdd a_n294_216# 0.390535f
C1 B a_n170_422# 0.097495f
C2 a_n170_422# a_n294_216# 0.186942f
C3 A a_n294_216# 0.07097f
C4 vdd Y 0.075827f
C5 B a_n294_216# 0.016201f
C6 a_n170_422# Y 0.494385f
C7 a_n170_422# vdd 1.01649f
C8 A Y 4.72e-19
C9 vdd A 0.11508f
C10 a_n170_422# A 0.003227f
C11 B Y 0.05308f
C12 B vdd 0.283403f
C13 Y a_n294_216# 0.147628f
C14 B vss 0.417836f
C15 Y vss 0.643651f
C16 A vss 0.214244f
C17 vdd vss 2.12895f
C18 a_n170_422# vss 0.186014f
C19 a_n294_216# vss 0.555133f
```

DRC and LVS Check

3.4.1 DRC Check:

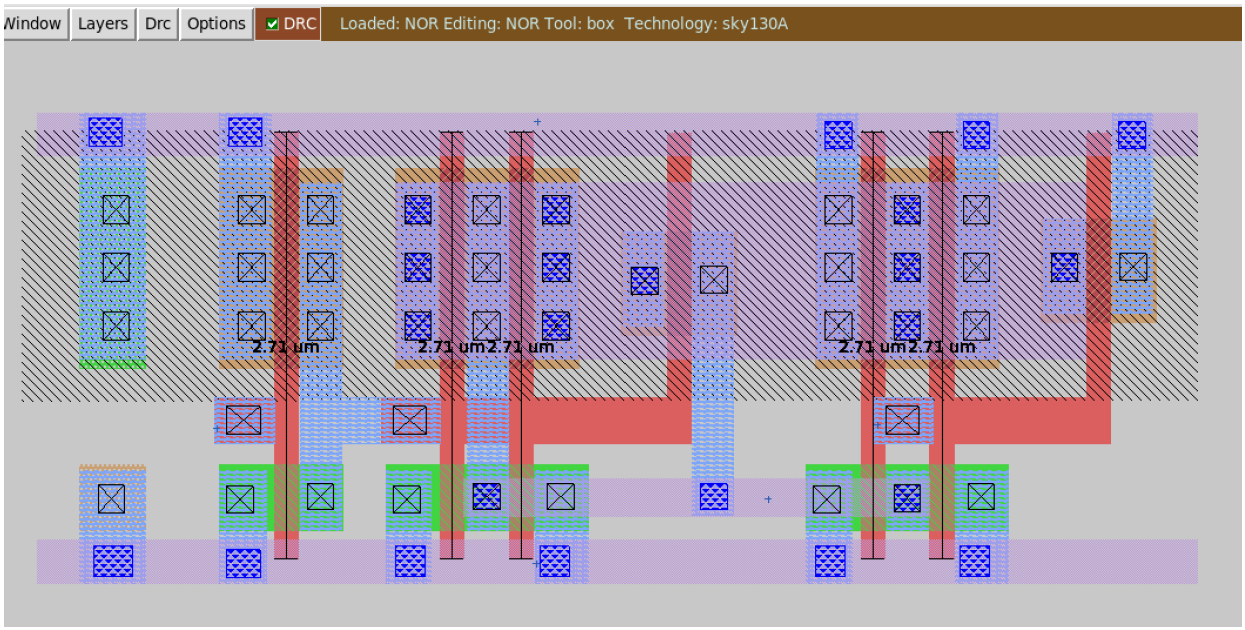

Figure 19: DRC Clean Proof

3.4.2 LVS Check:

```
amol_18@DESKTOP-Q99KTQ7:/mnt/d/VLSI_Design/Course_Project_All_Files/Final_NOR$ netgen -
batch lvs "norx1_layout.spice NORl" "norx1_schematic.spice NORs" /usr/local/share/pdk/s
ky130A/libs.tech/netgen/sky130A_setup.tcl | tail -n 22
Contents of circuit 1:  Circuit: 'NORl'
Circuit NORl contains 6 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:   3
  Class: sky130_fd_pr__pfet_01v8 instances:   3
Circuit contains 7 nets.
Contents of circuit 2:  Circuit: 'NORs'
Circuit NORs contains 6 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:   3
  Class: sky130_fd_pr__pfet_01v8 instances:   3
Circuit contains 7 nets.

Circuit 1 contains 6 devices, Circuit 2 contains 6 devices.
Circuit 1 contains 7 nets,    Circuit 2 contains 7 nets.

No more changes can be made to series/parallel networks.
No more changes can be made to series/parallel networks.

Final result:
Circuits match uniquely.
.
Logging to file "comp.out" disabled
LVS Done.
amol_18@DESKTOP-Q99KTQ7:/mnt/d/VLSI_Design/Course_Project_All_Files/Final_NOR$
```

Figure 20: LVS Clean Proof

Waveforms

3.5.1 Rise Time

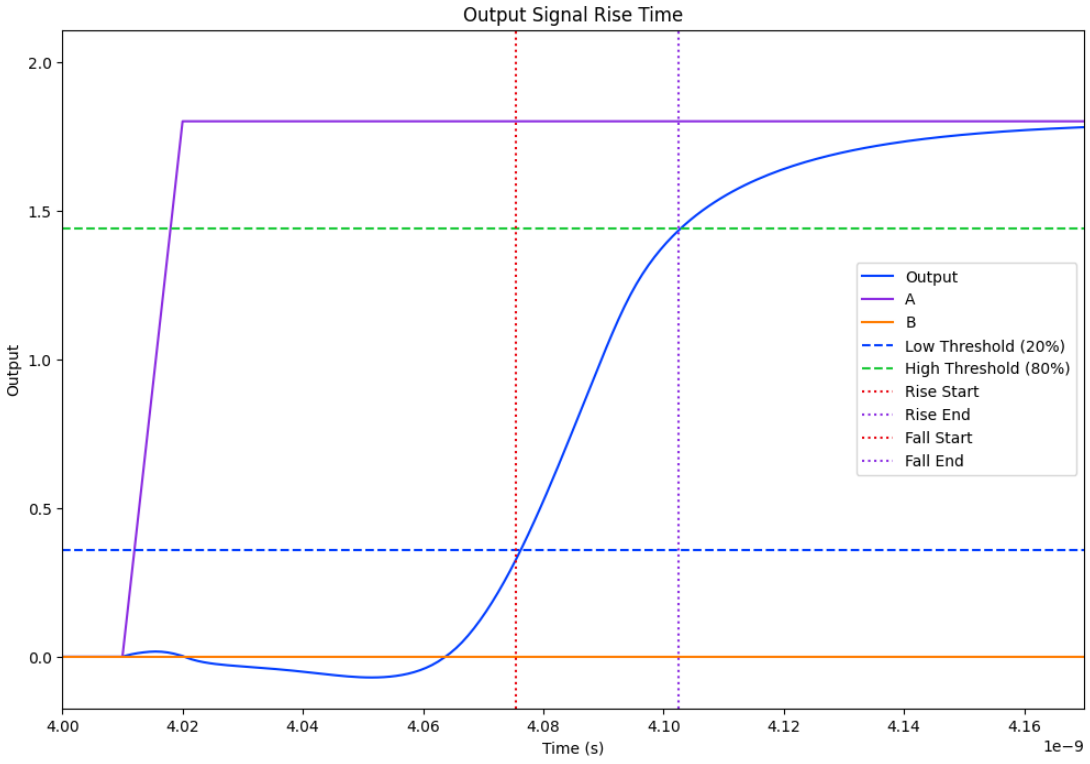

Figure 21: Rise Time

3.5.2 Fall Time

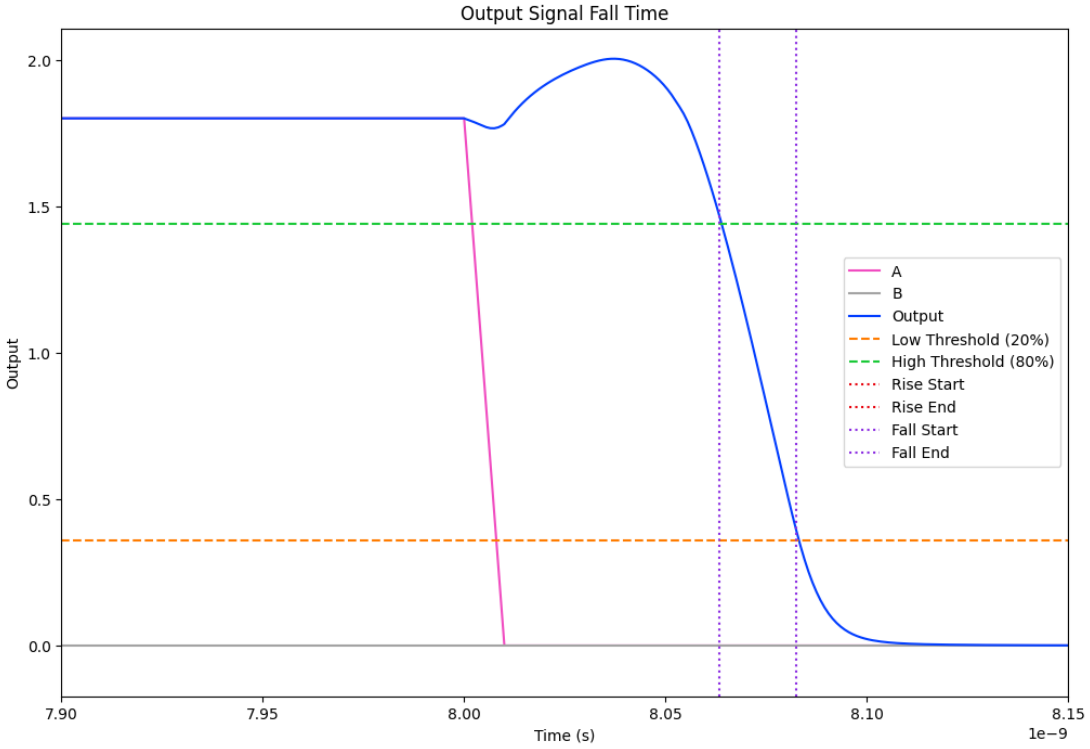

Figure 22: Fall Time

3.5.3 Propagation Delay

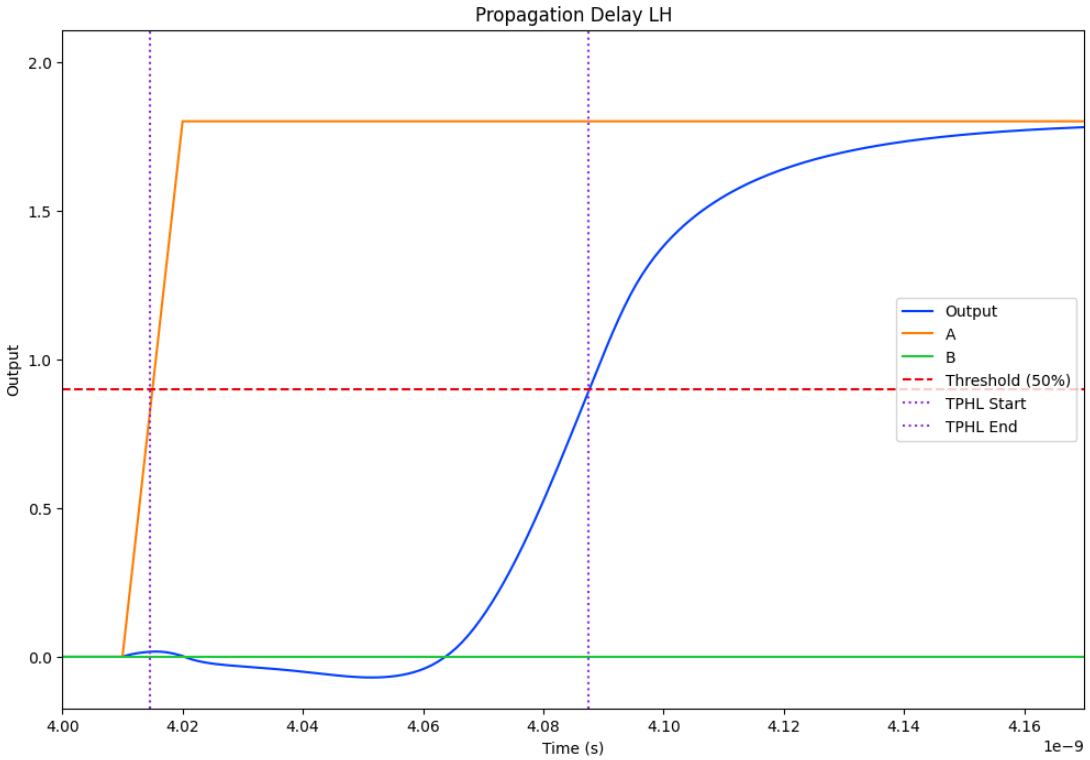

Figure 23: LH Propagation delay

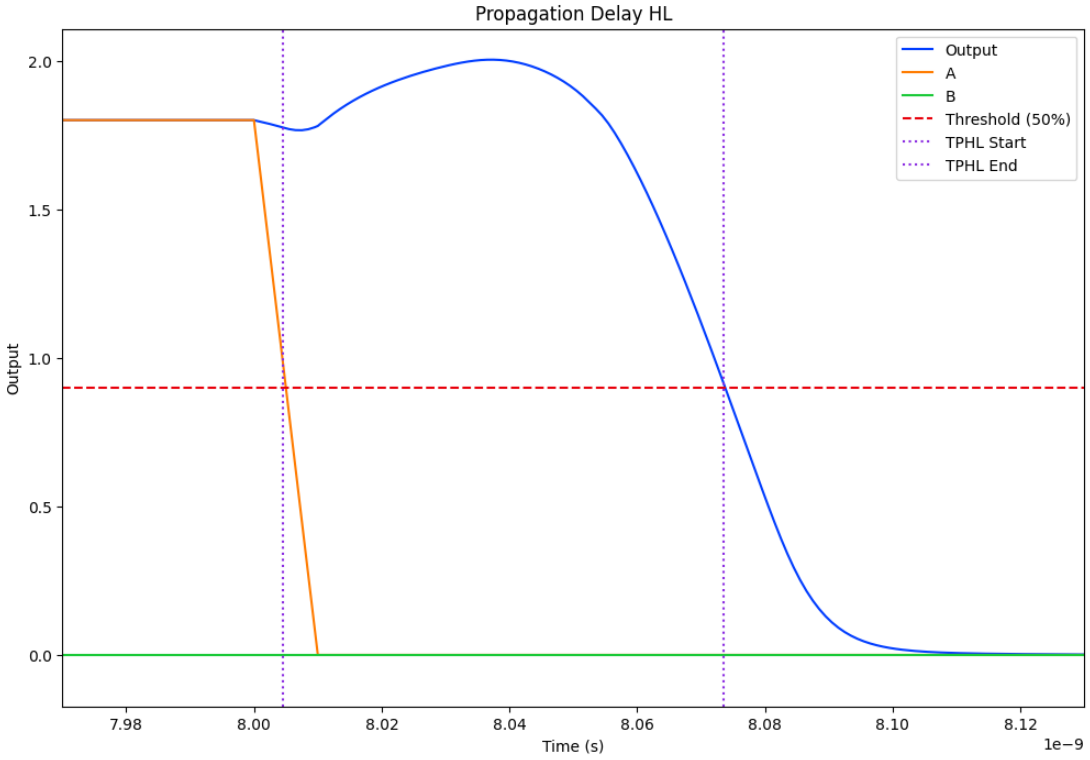

Figure 24: HL Propagation delay

Input Capacitances

Input Pins	Rise Cap (pF)	Fall Cap (pF)	Average Cap (pF)
A	$2.24*10^{-3}$	$2.32*10^{-3}$	$2.28*10^{-3}$
B	$5.6*10^{-3}$	$5.5*10^{-3}$	$5.55*10^{-3}$

Table 24: Input Pin Capacitances

Timing Tables

	10 ps	100 ps	1000 ps
0.5 fF	$27*10^{-3}$	$27*10^{-3}$	$42*10^{-3}$
10 fF	$68*10^{-3}$	$68.99*10^{-3}$	$79*10^{-3}$
100 fF	$484*10^{-3}$	$484.99*10^{-3}$	$483.99*10^{-3}$

Table 25: Output Rise Transitions (in ns) [Input slew vs output capacitance]. Related pin A

	10 ps	100 ps	1000 ps
0.5 fF	$24*10^{-3}$	$26.86*10^{-3}$	$89*10^{-3}$
10 fF	$68*10^{-3}$	$69*10^{-3}$	$138.99*10^{-3}$
100 fF	$484*10^{-3}$	$485*10^{-3}$	$502.86*10^{-3}$

Table 26: Output Rise Transitions (in ns) [Input slew vs output capacitance]. Related pin B

	10 ps	100 ps	1000 ps
0.5 fF	$19*10^{-3}$	$19*10^{-3}$	$34*10^{-3}$
10 fF	$47*10^{-3}$	$47*10^{-3}$	$59*10^{-3}$
100 fF	$329*10^{-3}$	$328.99*10^{-3}$	$329.99*10^{-3}$

Table 27: Output Fall Transitions (in ns) [Input slew vs output capacitance]. Related pin A

	10 ps	100 ps	1000 ps
0.5 fF	$26.99*10^{-3}$	$27.99*10^{-3}$	$96*10^{-3}$
10 fF	$57.99*10^{-3}$	$56*10^{-3}$	$146*10^{-3}$
100 fF	$340*10^{-3}$	$342*10^{-3}$	$433*10^{-3}$

Table 28: Output Fall Transitions (in ns) [Input slew vs output capacitance]. Related pin B

	10 ps	100 ps	1000 ps
0.5 fF	$73*10^{-3}$	$92*10^{-3}$	$201.99*10^{-3}$
10 fF	$106.99*10^{-3}$	$124.99*10^{-3}$	$244*10^{-3}$
100 fF	$402*10^{-3}$	$421*10^{-3}$	$538.99*10^{-3}$

Table 29: Cell Rise Delay (in ns) [Input slew vs output capacitance]. Related pin A

	10 ps	100 ps	1000 ps
0.5 fF	$37.86*10^{-3}$	$57.86*10^{-3}$	$116*10^{-3}$
10 fF	$70.86*10^{-3}$	$90.86*10^{-3}$	$198*10^{-3}$
100 fF	$364*10^{-3}$	$385.86*10^{-3}$	$561.86*10^{-3}$

Table 30: Cell Rise Delay (in ns) [Input slew vs output capacitance]. Related pin B

	10 ps	100 ps	1000 ps
0.5 fF	$68.99*10^{-3}$	$90.99*10^{-3}$	$221*10^{-3}$
10 fF	$97.99*10^{-3}$	$120*10^{-3}$	$257*10^{-3}$
100 fF	$318.99*10^{-3}$	$340.99*10^{-3}$	$483*10^{-3}$

Table 31: Cell Fall Delay (in ns) [Input slew vs output capacitance]. Related pin A

	10 ps	100 ps	1000 ps
0.5 fF	32.99×10^{-3}	51.99×10^{-3}	140.99×10^{-3}
10 fF	58.99×10^{-3}	77×10^{-3}	203.99×10^{-3}
100 fF	279.99×10^{-3}	298.99×10^{-3}	505.99×10^{-3}

Table 32: Cell Fall Delay (in ns) [Input slew vs output capacitance]. Related pin B

Power Tables

Condition (AB)	Power (nW)
00	0.623
01	0.618
10	0.986
11	0.616

Table 33: Static Power (all possible input combinations of AB)

	10 ps	**100 ps**	**1000 ps**
0.5 fF	$294.30*10^3$	$209.58*10^3$	$77.93*10^3$
10 fF	$428.53*10^3$	$369.81*10^3$	$143.51*10^3$
100 fF	$677.91*10^3$	$477.18*10^3$	$302.44*10^3$

Table 34: Dynamic Power Table (i) Rise Power (in nW) [Input slew vs output capacitance]. Related pin A

	10 ps	**100 ps**	**1000 ps**
0.5 fF	$334.29*10^3$	$252.24*10^3$	$66.84*10^3$
10 fF	$551.45*10^3$	$389.55*10^3$	$124.34*10^3$
100 fF	$708.68*10^3$	$466.52*10^3$	$319.09*10^3$

Table 35: Dynamic Power Table (i) Rise Power (in nW) [Input slew vs output capacitance]. Related pin B

	10 ps	**100 ps**	**1000 ps**
0.5 fF	$339.58*10^3$	$245.51*10^3$	$74.68*10^3$
10 fF	$593.35*10^3$	$433.21*10^3$	$137.05*10^3$
100 fF	$1059.69*10^3$	$739.64*10^3$	$421.02*10^3$

Table 36: Dynamic Power Table (ii) Fall Power (in nW) [Input slew vs output capacitance]. Related pin A

	10 ps	**100 ps**	**1000 ps**
0.5 fF	$877.52*10^3$	$409.89*10^3$	$68.15*10^3$
10 fF	$1102.91*10^3$	$612.16*10^3$	$126.78*10^3$
100 fF	$1431.54*10^3$	$1005.32*10^3$	$347.11*10^3$

Table 37: Dynamic Power Table (ii) Fall Power (in nW) [Input slew vs output capacitance]. Related pin B

4 Contributions

- Jay
    1. NOR layout design
    2. Power Calculations, Input Capacitances, Rise Time, Fall Time and Propagation Delays for DFF
- Vatsal
    1. DFF layout design
    2. Setup and Hold time calculations for DFF
- Jainam
    1. Buffer layout design
    2. Complete characterisation of Buffer
- Amol
    1. NOR layout design
    2. Complete characterisation of NOR gate