For Sequential cells, the following characterizations have to be performed and filled.

1. **Input pin capacitances:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Input Pins** | **Rise Cap (pF)** | **Fall Cap (pF)** | **Average Cap (pF)** |
| D | 2.4978e-3 | 2.4852e-3 | 2.4915e-3 |
| CLK | 9.3546e-3 | 9.3358e-3 | 9.3452e-3 |

1. **Set-up Time Table:**

**(i) Rise Constraint** **(in ns)** [Input slew vs CLK slew].

|  |  |  |
| --- | --- | --- |
|  | **10 ps** | **1000 ps** |
| **10 ps** | 0.115 | -0.008 |
| **1000 ps** | 0.282 | 0.140 |

**(ii) Fall Constraint** **(in ns)** [Input slew vs CLK slew].

|  |  |  |
| --- | --- | --- |
|  | **10 ps** | **1000 ps** |
| **10 ps** | 0.11 | 0.191 |
| **1000 ps** | 0.28 | 0.353 |

1. **Hold Time Table:**

**(i) Rise Constraint** **(in ns)** [Input slew vs CLK slew].

|  |  |  |
| --- | --- | --- |
|  | **10 ps** | **1000 ps** |
| **10 ps** | -0.069 | -0.172 |
| **1000 ps** | -0.228 | -0.334 |

**(ii) Fall Constraint** **(in ns)** [Input slew vs CLK slew].

|  |  |  |
| --- | --- | --- |
|  | **10 ps** | **1000 ps** |
| **10 ps** | -0.062 | 0.01 |
| **1000 ps** | -0.212 | -0.133 |

1. **Transition Time Table (for Q output, CLK will have minimum slew of 10 ps):** (please strictly consider 20% and 80% of VDD for transition time)

**(i) Output Rise Transitions** **(in ns)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | 21.15e-3 | 21.15e-3 | 21.1e-3 |
| **10 fF** | 71.4e-3 | 71.4e-3 | 71.4e-3 |
| **100 fF** | 592.2e-3 | 592.2e-3 | 592.2e-3 |

**(ii) Output Fall Transitions** **(in ns)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | 18.46e-3 | 18.50e-3 | 19.4e-3 |
| **10 fF** | 75.96e-3 | 75.98e-3 | 76.4e-3 |
| **100 fF** | 641.3e-3 | 641.3e-3 | 641.3e-3 |

1. **CLK-to-Q Delay Time Table**: (delay between clock transition and data transition. Use 50% of CLK to 50% of output to simulate propagation delay).

**(i) Cell Rise Delay (in ns)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | 202.48e-3 | 220.47e-3 | 374.8e-3 |
| **10 fF** | 249.29e-3 | 267.28e-3 | 421.6e-3 |
| **100 fF** | 608.8e-3 | 626.8e-3 | 781.2e-3 |

**(ii) Cell Fall Delay (in ns)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | 133.33e-3 | 150.97e-3 | 269.3e-3 |
| **10 fF** | 188.32e-3 | 206.02e-3 | 324.8e-e3 |
| **100 fF** | 625.5e-3 | 643.2e-3 | 762.3e-3 |

1. **Static Power (all possible input combinations of CLK and D).**

|  |  |
| --- | --- |
| **Condition (CLK, D)** | **Power (nW)** |
| 00 | 380.91e-3 |
| 01 | 380.95e-3 |
| 10 | 490.58e-3 |
| 11 | 490.59e-3 |

1. **Dynamic Power Table: (CLK will have minimum slew of 10 ps)**

**(i) Rise Power (in nW)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | 115.83e3 | 84.32e3 | 30.13e3 |
| **10 fF** | 198.62e3 | 143.17e3 | 56.03e3 |
| **100 fF** | 232.94e3 | 195.45e3 | 142.36e3 |

**(ii) Fall Power (in nW)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | 112.37e3 | 69.24e3 | 20.52e3 |
| **10 fF** | 108.85e3 | 76.71e3 | 20.33e3 |
| **100 fF** | 46.39e3 | 42.29e3 | 18.65e3 |