ECE 526L Spring 2021

Lab 10

Serial protocol

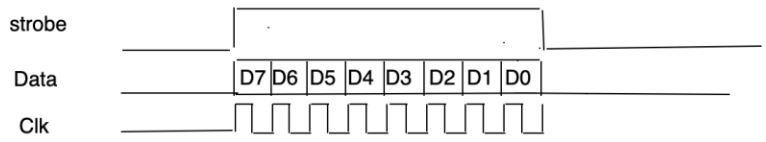
In this experiment, you will create a module that sends a byte serially and receives it in loopback.

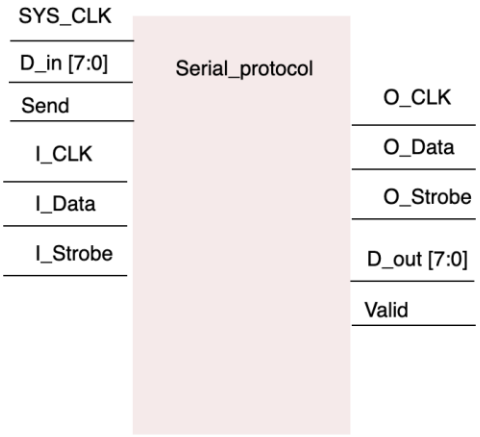
Create the serial module based on the symbol and description below:

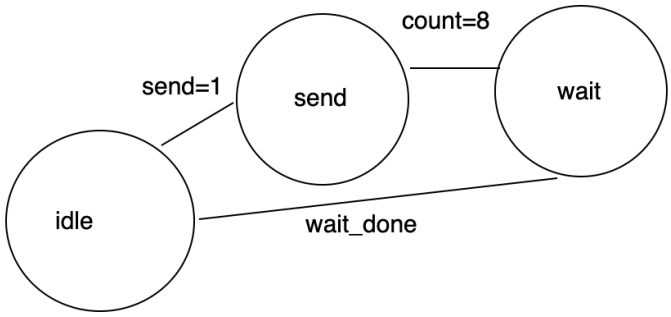
- Your module receives a byte of data and if send is asserted sends it one bit at a time at each posedge of O_clk
- For simplicity initially you can assume O_clk is the same as SYS_Clk, for extra credit make O_clk half freq od SYS_clk
- During transmission Strobe is high and other times it's low
- You should wait for 8 bit times before sending next byte
- On the receive side sample the incoming bits at negedge of I_clk
- You should use state machines for both receive and transmit functions.
- When byte is fully received you should assert valid for 1 clock

You should create a testbench to test your design:

- Your test bench should fully test the transmit and receive scenarios and show you can transmit a given byte and receive the exact byte back


strobe
Data
D7
D6
D5
D4
D3
D2
D1
D0
Clk


SYS_CLK
D_in [7:0]
Send
I_CLK
I_Data
I_Strobe
Serial_protocol
O_CLK
O_Data
O_Strobe
D_out [7:0]
Valid


count=8
send=1
send
wait
idle
wait_done