ECE 526L Spring 2021

Lab 9

Parameterized Synchronous FIFO

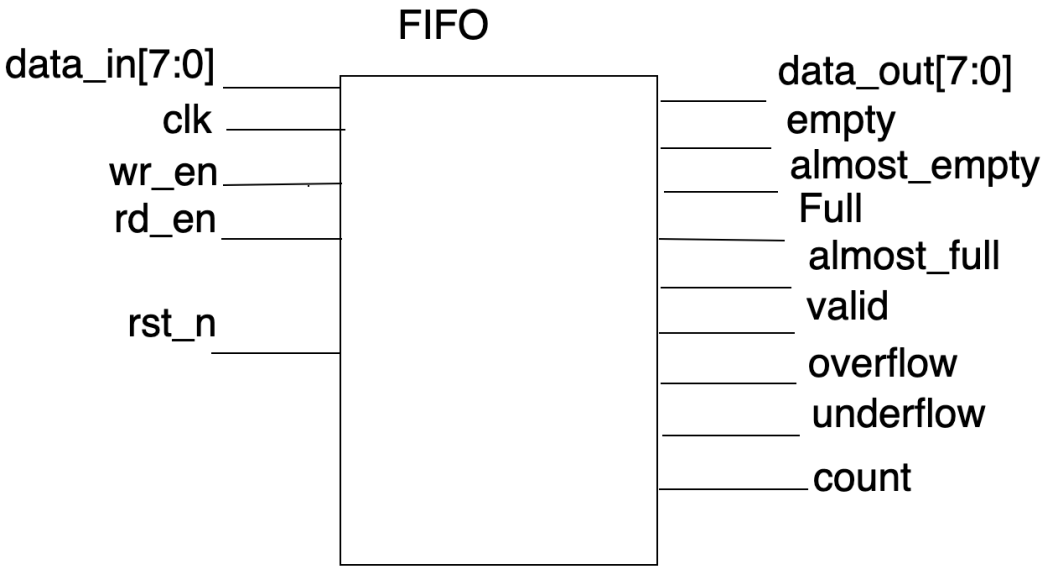
In this experiment, you will model a parameterized synchronous FIFO.

Create a FIFO module based on the symbol and description below:

- Your FIFO's data width and depth should be parameterized, for the test cases, use width 8 and depth 32.
- You would use the same clock for read and write
- provide empty/full and almost empty/ almost full flags, for the almost flags make it a parameter, for the test case use 2.
- You should use read/write counter to keep track of data locations, provide count of the FIFO as an output, this is different than write/read counters.
- Provide a valid signal on successful read
- Provide overflow/underflow flags
- Design can't be empty and full at the same time, same with similar flags
- Using an ifdef create two versions, first word fall through, and normal

You should create a testbench to test your design:

- Your test should cover all the flag behaviors.
- Your test should demonstrate write and read to all locations.
- You should show a simultaneous write and read in the middle, that shows what you read is different than what you just wrote.
- show that count and valid are behaving correctly.
- You should do a separate test for the first word fall through case and compare how it is different.


FIFO
data_in[7:0]
clk
wr_en
rd_en
rst_n
data_out[7:0]
empty
almost_empty
Full
almost_full
valid
overflow
underflow
count