**Experiment #10**

**Serial protocol**

Laboratory Report

Prepared for: ECE 526/L – Digital Design with Verilog and System Verilog Lab

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**Introduction:**

The goal of this experiment is to create a module of Serial protocol using behavioral model that can be used for width and depth. Here instead of describing the actual hardware implementation of the circuit, the behavior of the input and output is used to create the model.

**Methodology:**

Two files were created using Verilog with names serial.v, and serial\_tb.v. serial.v for the behavioral description of a Serial protocol, serial\_tb.v consist of the Verilog test bench of Serial protocol.

serial.v and serial\_tb.v programs were simulated using Synopsis VCS after completing the development of the two programs. VCS program was compiled using these 3 steps:

1. The 2 files were compiled using ‘vcs’ command.
2. ‘simv’ command was used to run the simulation.
3. ‘dve’ command was used to display the waveform of the simulation

Two waveform view for signed and unsigned numbers were generated using the DVE graphical interface.

**Analysis of Results:**

At 20ns Send=1; so the data in D\_in starts transmiting. So at 256ns data transmission starts, 1 bit at each negedge and the strobe is 1. Also at the receiving side at negedge when strobe is 1 the data bit-by-bit was written to the output.

**A picture containing graphical user interface

Description automatically generated**

So after 8 complete cycle i.e. 30ns to 110ns of CLK the 8 bit data was receivedat the receiver side. Also at that time valid=1;

Graphical user interface

Description automatically generated

Also the D\_in at 40ns was changed but until the earlier is not received by the receiver side the new data was not sent.

Graphical user interface

Description automatically generated

**Conclusion:**

Here we can conclude that until the earlier is not received by the receiver side the new data was not sent. During transmission Strobe is high and other times it’s low. On the receive side sample the incoming bits at negedge of clk. When byte is fully received you should assert valid for 1 clock. Also here we have determine that how FSM is implemented.

I hereby attest that this lab report is entirely my own work. I have not copied either code or text from anyone, nor have I allowed or will I allow anyone to copy my work.

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Name (signed) \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Date \_\_\_\_05/14/2021\_\_\_\_