**Experiment #2**

**Change in Waveform due to delay**

Laboratory Report

Prepared for: ECE 526/L – Digital Design with Verilog and System Verilog Lab

Prepared by:

Jaymish Patel

**Introduction:**

The goal of this experiment is to become familiar how the delays change the waveform. To learn this initially the circuit was simulated without delay and then it was simulated with the delays. For simulation, Synopsis VCS was used.

**Methodology:**

Few files were created using Verilog with names lab2.v, lab2\_1.v, lab2\_2.v, lab2\_3.v and lab\_tb.v. lab2.v consists of Verilog circuit description and was created using the structural description of the circuit given in the lab manual for case 1 using the gate-level modeling with all delays set to 0 ns. lab2\_1.v consists of Verilog circuit description and was created using the structural description of the circuit given in the lab manual for case 1 using the gate-level modeling with all delays as defined in the lab manual. lab2\_2.v consists of Verilog circuit description and was created using the structural description of the circuit given in the lab manual for case 2 using the gate-level modeling with all delays set to 0 ns. lab2\_1.v consists of Verilog circuit description and was created using the structural description of the circuit given in the lab manual for case 2 using the gate-level modeling with all delays as defined in the lab manual. lab\_tb.v consist of the Verilog test bench that contains all the possible combinations of in1 and in2

All the inputs combination are used for the test of the desine. In lab2.v there are 2 inputs namely in1 and in2 and there is one output, out1. For these 2 inputs, there are 2 possible values thus making up total of , so total 4 combinations, for the exhaustive test all the combinations are selected for this test bench. In compliance with the time scale directive specifically stated in the module, time delays of 15 ns were used for all test values for simulation purposes.

Those programs were simulated using Synopsis VCS after completing the development of the two programs. VCS program was compiled using these 3 steps:

1. The 2 files were compiled using ‘vcs’ command.
2. ‘smv’ command was used to run the simulation.
3. ‘dve’ command was used to display the waveform of the simulation

A waveform view of top-level signals consisting of in1, in2 input ports, A1,A1,O1 wires and out1 output ports has been created using the DVE graphical interface. For the purpose of gate level analysis and overall analysis of circuit behavior, the waveform was used.

**Analysis of Results:**

Analyzing the waveform produced from the simulation of case 1 for with and without delay, it is possible to determine that initially output was available instantly but with delay the output delays with 10.5ns also for case 2, initially output was available instantly but with delay the output delays with 11.5ns. A picture containing graphical user interface

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**Conclusion:**

The difference of delay of output due to the delay in the circuit was discovered by conducting this experiment. The basic principle of delay in the digital circuit was studied. The exhaustive test stimulus helps to validate all the conceptual functionality of the module concept. It also discusses the usage of “.” operator within the test node.

Here to determine the delays between the wires, input and output the graphical waveform was helpful.

**Additional Question:**

For the case-1 with delay the critical path (longest delay) of the design is

in1-NT-A2-out1

int1-NT has delay of 2ns

NT-A2 has delay of 0.5ns

A2-out1 has delay of 8ns

Total delay of 10.5ns

For the case-2 with delay the critical path (longest delay) of the design is

in1-NT-A2-O1-out1

int1-NT has delay of 2.5ns

NT-A2 has delay of 0.5ns

A2-O1 has delay of 2ns

O1-out1 has delay of 6.5ns

Total delay of 11.5ns

I hereby attest that this lab report is entirely my own work. I have not copied either code or text from anyone, nor have I allowed or will I allow anyone to copy my work.

Name (printed) \_\_\_\_\_Jaymish Raju Patel\_\_\_\_\_\_\_\_\_

Name (signed) \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Date \_\_\_\_02/09/2021\_\_\_\_