**Experiment #3**

**Model an edge triggered flip-flop**

Laboratory Report

Prepared for: ECE 526/L – Digital Design with Verilog and System Verilog Lab

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**Introduction:**

The goal of this experiment is to design a module and reuse that module whenever needed. For this we will design a module of SR flip-flop and then reuse it in the positive edge triggered D flipflop with clear.

**Methodology:**

Three files were created using Verilog with names lab3.v, lab3\_1.v and lab3\_1\_tb.v. lab3.v consists of Verilog circuit description of the SR flipflop. Lab3\_1.v consist Verilog circuit description of the D flipflop by including lab3.v in this file and reusing the the SR latch module. Lab3\_1\_tb.v consist of the Verilog test bench.

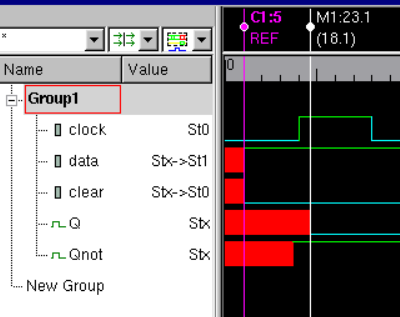
Those two programs were simulated using Synopsis VCS after completing the development of the two programs. VCS program was compiled using these 3 steps:

1. The 2 files were compiled using ‘vcs’ command.
2. ‘smv’ command was used to run the simulation.
3. ‘dve’ command was used to display the waveform of the simulation

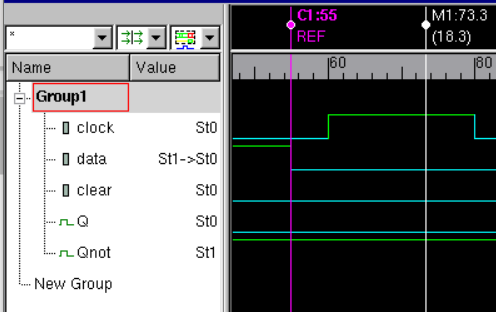
A waveform view of top-level signals consisting of Data, Clear, Clock input ports and Q,Qnot output ports has been created using the DVE graphical interface. For the purpose of gate level analysis and overall analysis of circuit behavior, the waveform was used.

**Analysis of Results:**

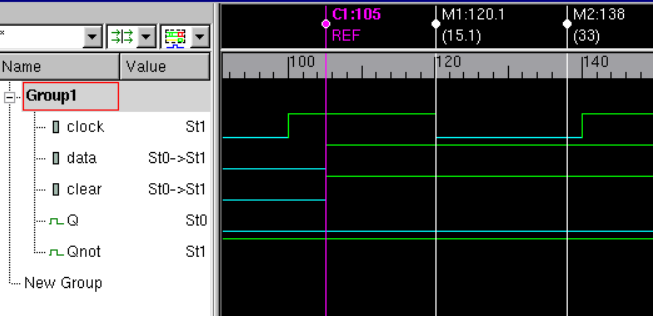
Analyzing the waveform produced from the simulation, it is possible to consider some instances of output signal effects with respect to certain conditions of input signals. The result of analysis is summarized here. At 5ns we get data=1 and clear =0, we get output at 23.1ns as Q=0 and Qnot=1.



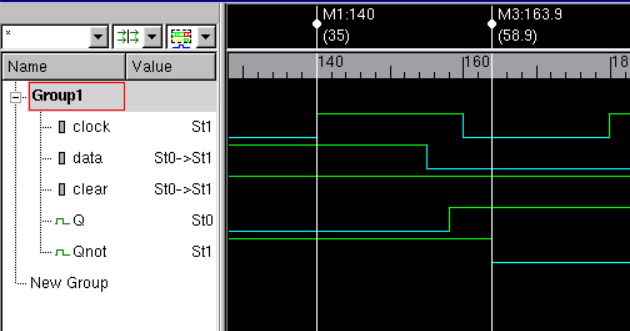
Also at 55ns data goes to 0 but clear is 0 so we get the same output at 73.3ns. So here we can analyze that when clear=0 the output will be Q=0 and Qnot=1 regardless of the inputs of data and clock.



Now clear=1 and data=1 at 105ns but there is no change in output as there is no clock transition. At 120.1ns there is not posedge so the output is repeated at 138ns.

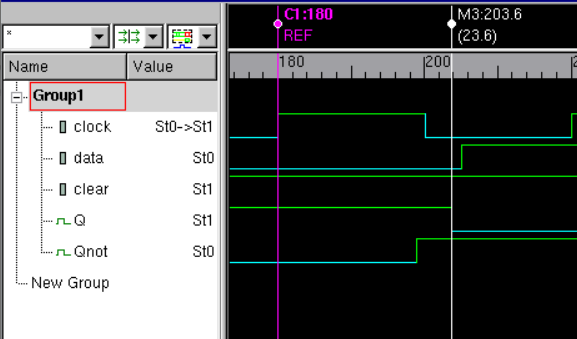


Now at 140ns there is a posedge at that time the data=1 and clear =1 so at 163.9ns we get Q=1 and Qnot=0



Now at 160 ns there is a not posedge so the output are repeated as they were at the last posedge transition.

Now at 180ns there is a posedge at that time the data=0 and clear=1 so at 203.6 ns the output is propagated as Q=0 and Qnot=1.



**Conclusion:**

So from the above analysis we can determine that the designed D flipflop is the positive edge triggered and when the clear=0 regardless of the other inputs we get the out put as Q=0 and Qnot=1. If there is a not posedge and clear=1 then the last output is repeated regardless of the data input. If there is posedge, clear=1 and data=0 then the output changes to Q=0 and Qnot=1 and if there is posedge, clear=1 and data=1 then the output changes to Q=1 and Qnot=0

**Additional Question:**

Critical Path.

**Diagram, schematic

Description automatically generated**

The longest path is calculate from the input data as data is propagated to output in this circuit.

data→not5→not6→nand4→nand3→nand6→nand5→q

total time to propagate output here is 3.5+3.5+5.8+5.8+5.8+4.8=**29.2ns**

data→not5→not6→nand4→nand1→nand2→nand5→q

total time to propagate output here is 3.5+3.5+5.8+4.5+6+4.8=**28.1ns**

data→not5→not6→nand4→nand1→nand2→nand3→nand6→nand5→q

total time to propagate output here is 3.5+3.5+5.8+4.5+6+5.8+5.8+4.8=**39.7ns**

So the critical path is:

data→not5→not6→nand4→nand1→nand2→nand3→nand6→nand5→q

with 39.7ns

the maximum operating frequency for this circuit is f=. Here T=39.7ns

f= = =

I hereby attest that this lab report is entirely my own work. I have not copied either code or text from anyone, nor have I allowed or will I allow anyone to copy my work.

Name (printed) \_\_\_\_\_Jaymish Raju Patel\_\_\_\_\_\_\_\_\_

Name (signed) \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Date \_\_\_\_02/19/2021\_\_\_\_