**Experiment #4**

**Model 8-bit register**

Laboratory Report

Prepared for: ECE 526/L – Digital Design with Verilog and System Verilog Lab

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**Introduction:**

The goal of this experiment is to design a module and reuse that module whenever needed. For this we will design a module of 8-bit register by using D-ff and a 2:1 mux.

**Methodology:**

Five files were created using Verilog with names register.v, mux2.v, dff.v, sr.v and reg\_tb.v. sr.v consists of Verilog circuit description of the SR flipflop. dff.v consist Verilog circuit description of the D flipflop by including sr.v in this file and reusing the the SR latch module. mux2.v contains the circuit description of the 2:1 mux. register.v contains the circuit description of the 8-bit register by including dff.v and mux2.v in this file and reusing the the D latch module and mux2 module. reg\_tb.v consist of the Verilog test bench.

Register.v and reg\_tb.v programs were simulated using Synopsis VCS after completing the development of the two programs. VCS program was compiled using these 3 steps:

1. The 2 files were compiled using ‘vcs’ command.
2. ‘smv’ command was used to run the simulation.
3. ‘dve’ command was used to display the waveform of the simulation

A waveform view of top-level signals consisting of DATA-data input RST, CLK, ENA input ports and R-data output has been created using the DVE graphical interface. For the purpose of gate level analysis and overall analysis of circuit behavior, the waveform was used.

**Analysis of Results:**

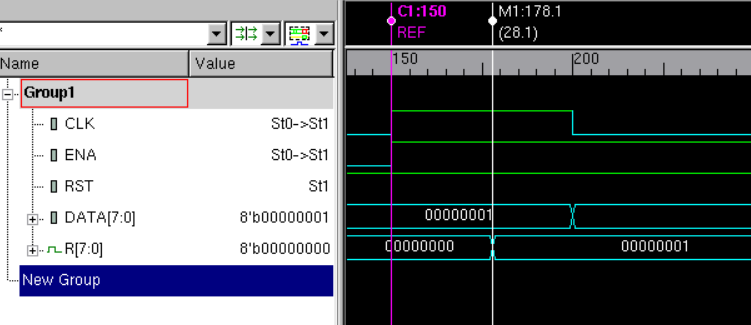
Analyzing the waveform produced from the simulation, it is possible to consider some instances of output signal effects with respect to certain conditions of input signals. The result of analysis is summarized here. At 50ns DATA=00000001 and RST =0, we get output at 68.1ns as R=00000000 regardless of CLK and ENA. Similar output is observed at 518.1ns due to RST=0 at 500ns

Graphical user interface

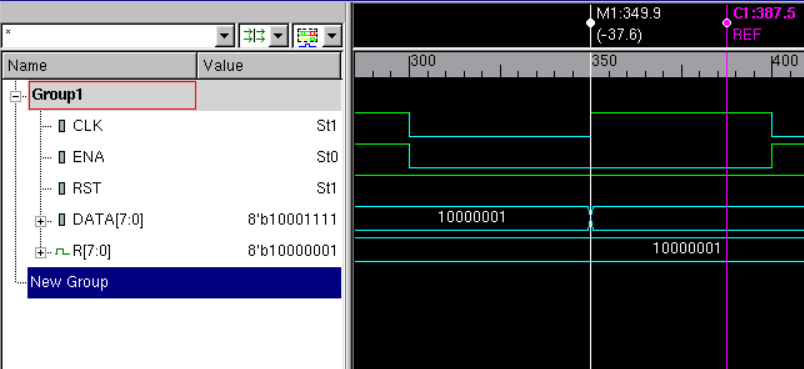
Description automatically generatedGraphical user interface, application

Description automatically generated

Also at 150ns DATA=1, ENA goes to 1 and also at the same time clock is 1 so we get R=00000001 at 178.1ns



Now DATA=10001111 and CLK=1 at 350ns there is no change in output as ENA=0. At 350ns ENA=0 so the output is repeated.



**Conclusion:**

So, from the above analysis we can determine that the designed 8-bit register resets when RST=0. The content of the data are clocked inti the register when ENA is asserted. And the content os the register is preserved and the contents of the data bus are ignored when the register is clocked with ENA deasserted.

I hereby attest that this lab report is entirely my own work. I have not copied either code or text from anyone, nor have I allowed or will I allow anyone to copy my work.

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Name (signed) \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Date \_\_\_\_02/27/2021\_\_\_\_