**Experiment #6**

**Scalable multiplexer**

Laboratory Report

Prepared for: ECE 526/L – Digital Design with Verilog and System Verilog Lab

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**Introduction:**

The goal of this experiment is to create a module of scalable multiplexer using behavioral model which functions asa scalable multiplexer. Here instead of describing the actual hardware implementation of the circuit, the behavior of the input and output is used to create the model.

**Methodology:**

Two files were created using Verilog with names mux.v for the behavioral description of the scalable multiplexer, and mux\_tb.v consist of the Verilog test bench.

mux.v and mux\_tb.v programs were simulated using Synopsis VCS after completing the development of the two programs. VCS program was compiled using these 3 steps:

1. The 2 files were compiled using ‘vcs’ command.
2. ‘smv’ command was used to run the simulation.
3. ‘dve’ command was used to display the waveform of the simulation

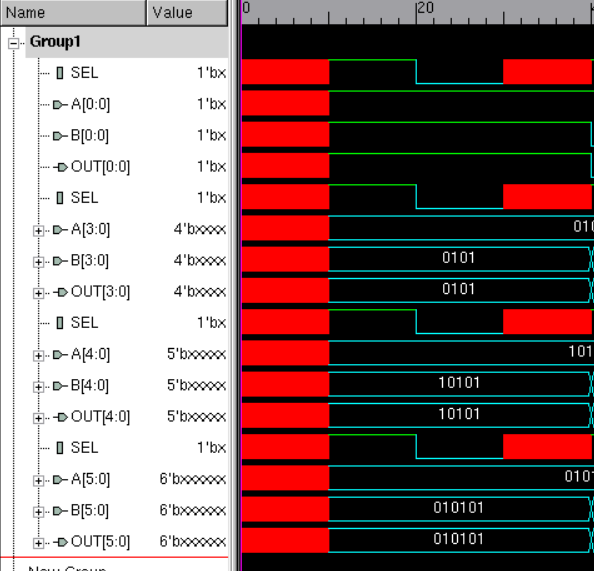
A waveform view of top-level signals consisting of DATA-data input RST, CLK, ENA, LOAD input ports and CNT-data output has been created using the DVE graphical interface.

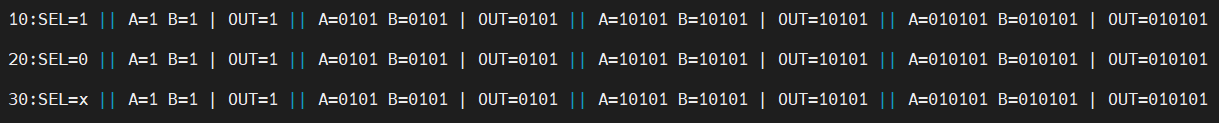
**Analysis of Results:**

Analyzing the waveform produced from the simulation, it is possible to consider some instances of output signal effects with respect to certain conditions of input signals. The result of analysis is summarized here. SEL, A, B and output are in binary.

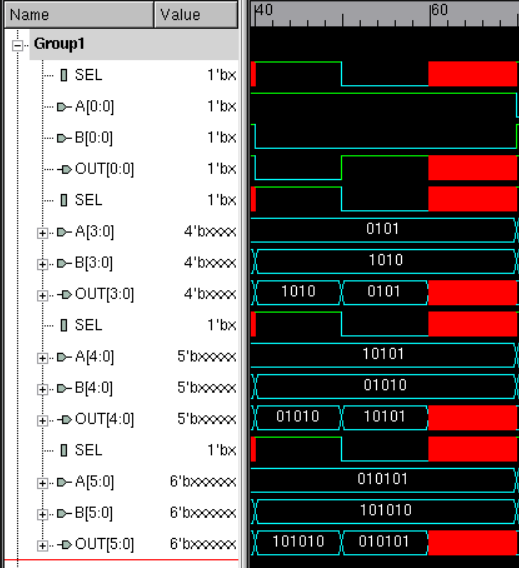
As this multiplexer is scalable there are four instances of mux that has different value of parameter SIZE. First instance has no value of parameter so by default it is assigned to 1. Then 2nd instance has parameter value of 4 so the mux will have input and output of 4 bits. Then 3rd instance has parameter value of 5 so the mux will have input and output of 5 bits. Then 4th instance has parameter value of 6 so the mux will have input and output of 6 bits.

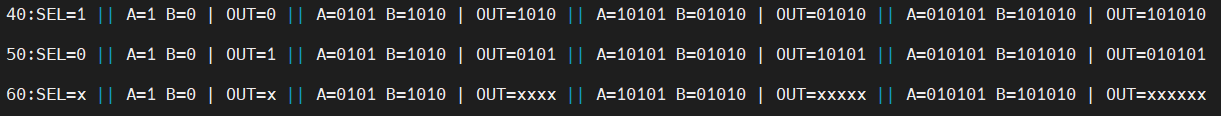
* Initially A and B both are same so regardless of the value of SEL we get output same as A or B.



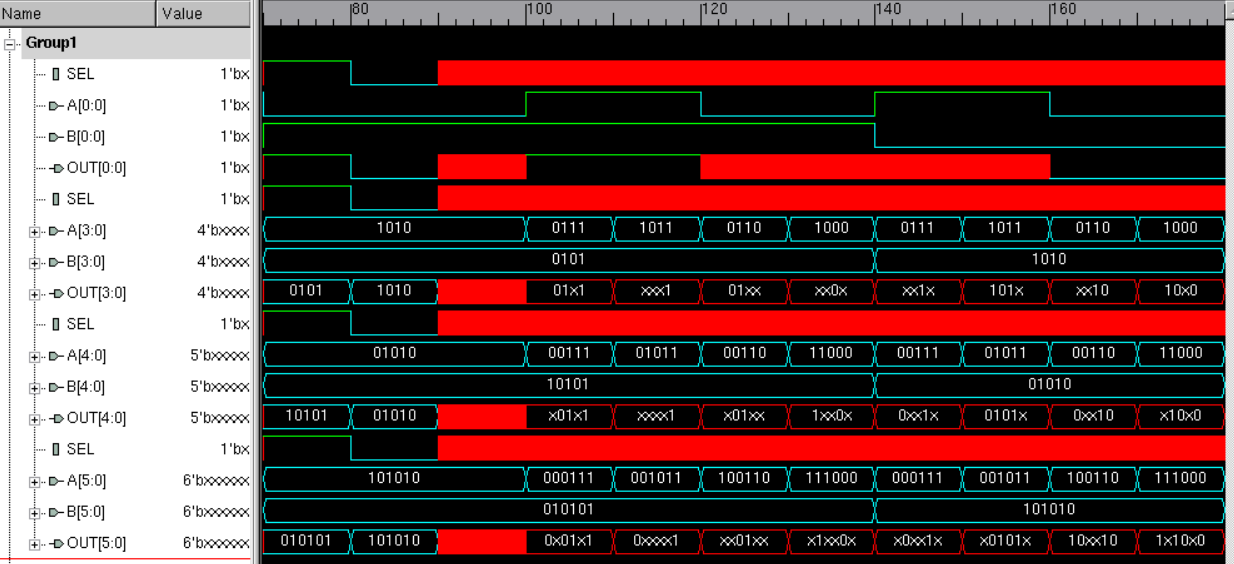


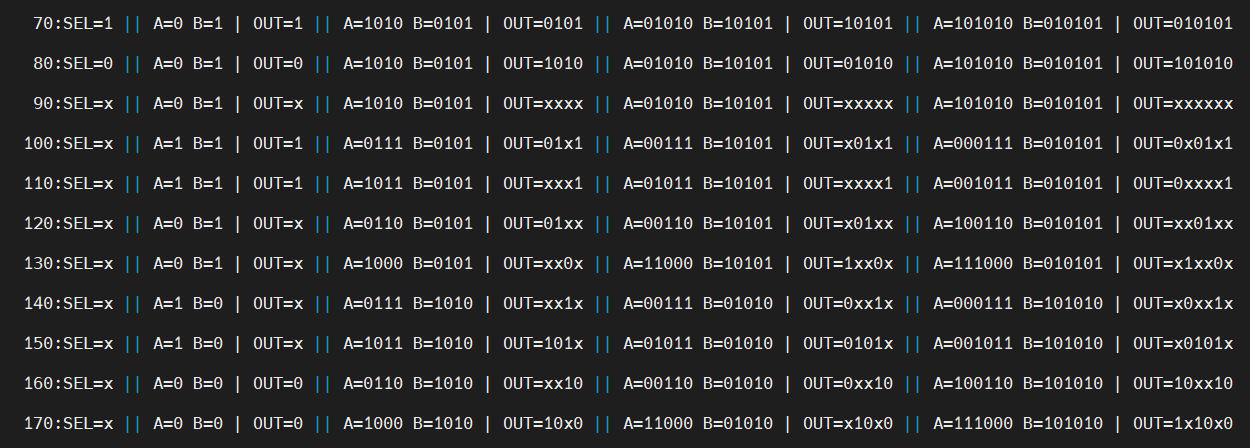
* Now A and B are both totally different, no bit same, so when SEL=0 we get value of A, when SEL=1 we get value of B and when SEL=x we get all bit of output as x.





* Now A and B are different but some bits are same in the input so when SEL=0 we get out put as A when SEL =1 we get output as B and when SEL=x and bit of A and B are same, output bit will be same as the input bit nut when SEL=x and bit of A and B are different we get X as output bit





**Conclusion:**

So, from the above analysis we can determine that input A will be selected when SEL = 0 and input B when SEL = 1. When SEL is unknown, multiplexers will resolve any bits for which A and B are the same. Any bits in conflict should result in x outputs.

I hereby attest that this lab report is entirely my own work. I have not copied either code or text from anyone, nor have I allowed or will I allow anyone to copy my work.

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Name (signed) \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Date \_\_\_\_03/27/2021\_\_\_\_