**Experiment #7**

**Register File Models**

Laboratory Report

Prepared for: ECE 526/L – Digital Design with Verilog and System Verilog Lab

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**Introduction:**

The goal of this experiment is to create a module of RAM and ROM using behavioral model and to use the bidirectional port. Here instead of describing the actual hardware implementation of the circuit, the behavior of the input and output is used to create the model.

**Methodology:**

Four files were created using Verilog with names ram.v, rom.v, ram\_tb.v, and rom\_tb.v. ram.v for the behavioral description of a RAM, rom.v for the behavioral description of a ROM, ram\_tb.v consist of the Verilog test bench of ram, rom\_tb.v consist of the Verilog test bench to test ROM.

ram.v rom.v and rom\_tb.sv programs were simulated and ram.v and ram\_tb were simulated using Synopsis VCS after completing the development of the two programs. VCS program was compiled using these 3 steps:

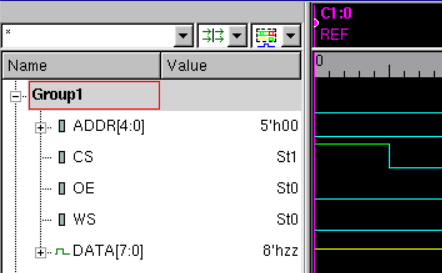
1. The 2 files were compiled using ‘vcs’ command.
2. ‘simv’ command was used to run the simulation.
3. ‘dve’ command was used to display the waveform of the simulation

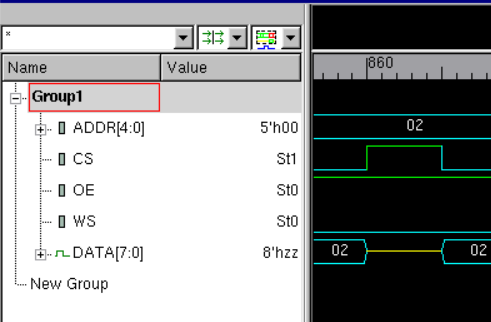
Two waveform view for RAM and ROM signals using the DVE graphical interface.

**Analysis of Results:**

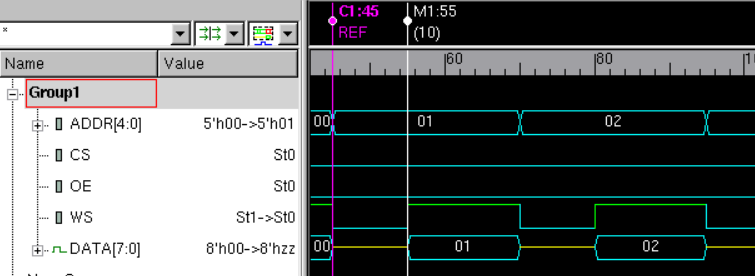
For Ram:

Whenever the chip select signal, CS, is high, OE and WS are ignored and the data bus remains in high impedance state.

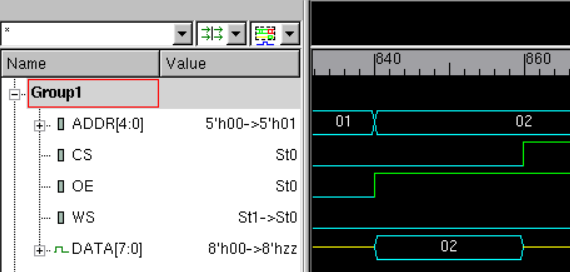




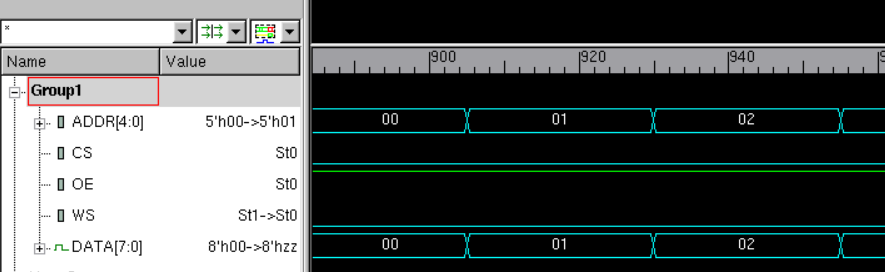
Data is inserted to the memory only at the rising edge of the write strobe, WS. At 55ns there is a rising edge and the data is inserted to the memory.



When OE is high the data in the memory at the address specified is placed on the databus.

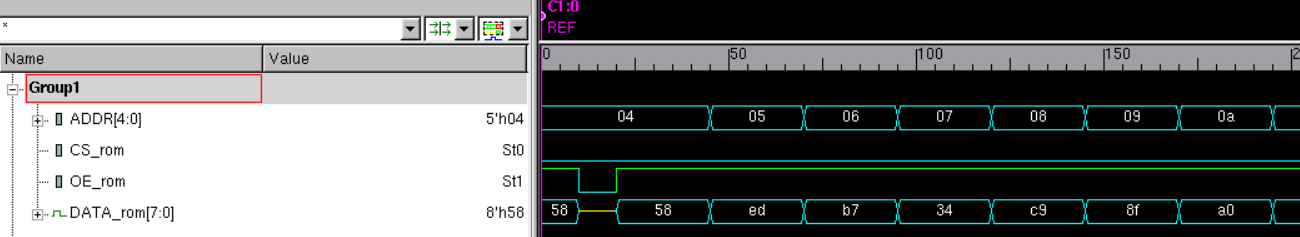


As long as OE remains high, the contents of the newly specified address are placed on the data bus.

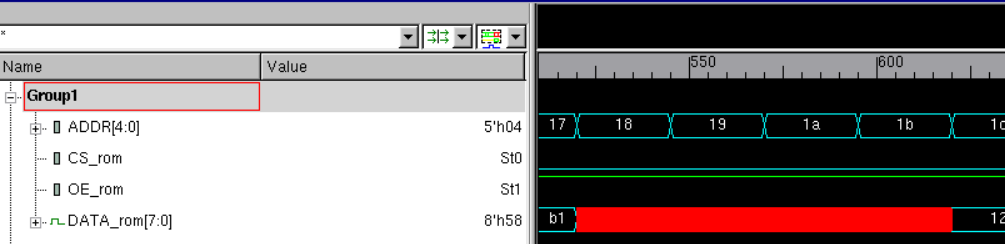


For ROM:

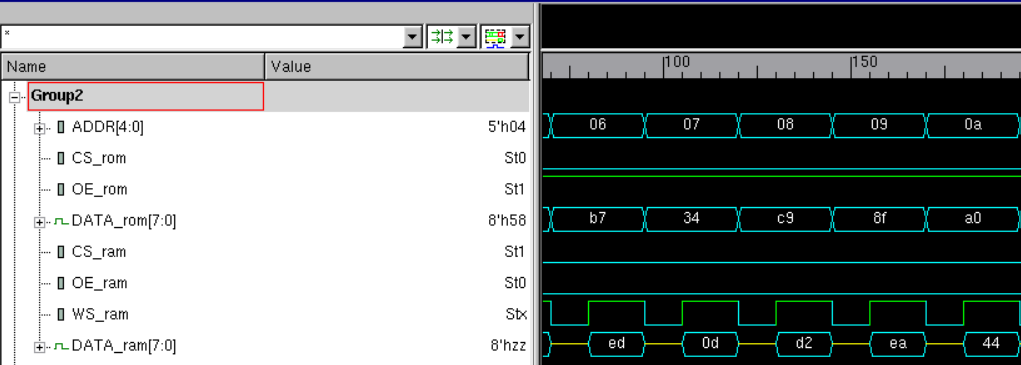
Here all the data is inputted to the memory of the rom using $readmemh. Those data is obtained from the memory at the specified address when OE is high.



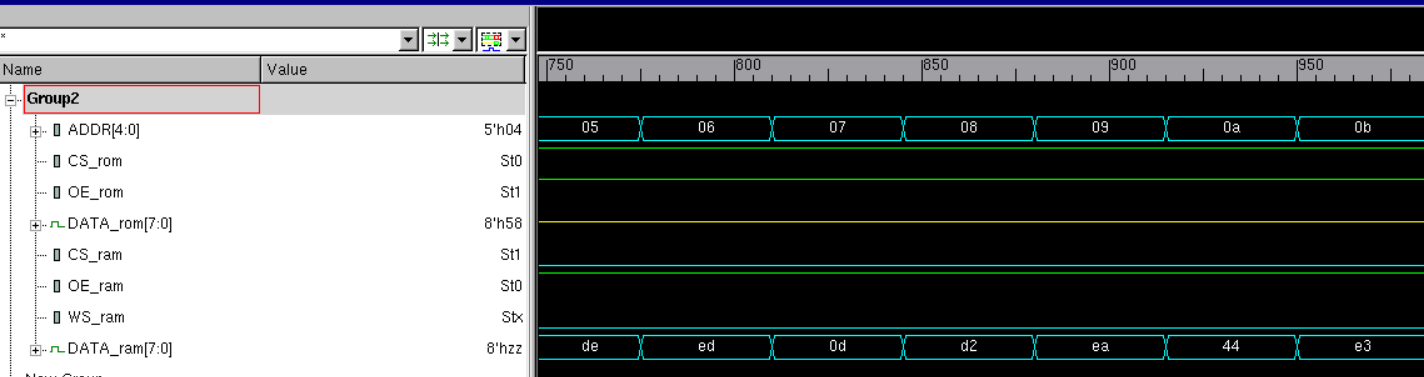
The unspecified locations remains undefine.



The test bench reads the data from the rom and then scrambles the data and then stores the scrambled data in the ram.



Demostration of the scrambled data stored in RAM.



**Conclusion:**

The configuration and verification of a memory file were successfully completed in this laboratory experiment.The main goal of this project was to design a RAM and ROM model and use it to access memory to read and write data, also it was to understand how to use and incorporate a bi-directional port to drive data in and out of it. The aim of the new system task $readmemh for initializing memory files was discovered.

I hereby attest that this lab report is entirely my own work. I have not copied either code or text from anyone, nor have I allowed or will I allow anyone to copy my work.

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Name (signed) \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Date \_\_\_\_04/11/2021\_\_\_\_