**Experiment #8**

**Arithmetic-Logic Unit Modeling**

Laboratory Report

Prepared for: ECE 526/L – Digital Design with Verilog and System Verilog Lab

Prepared by:

Jaymish Patel

**Introduction:**

The goal of this experiment is to create a module of ALU using behavioral model that can be used for signed and unsigned numbers. Here instead of describing the actual hardware implementation of the circuit, the behavior of the input and output is used to create the model.

**Methodology:**

Three files were created using Verilog with names alu.sv, alu\_tb.v, and alu\_tb1.v. alu.v for the behavioral description of a ALU for signed and unsigned using ifdef, alu\_tb.v consist of the Verilog test bench of alu for signed number, alu\_tb1.v consist of the Verilog test bench of alu for unsigned numbers.

alu.sv alu\_tb.v and alu\_tb1.v programs were simulated using Synopsis VCS after completing the development of the two programs. VCS program was compiled using these 3 steps:

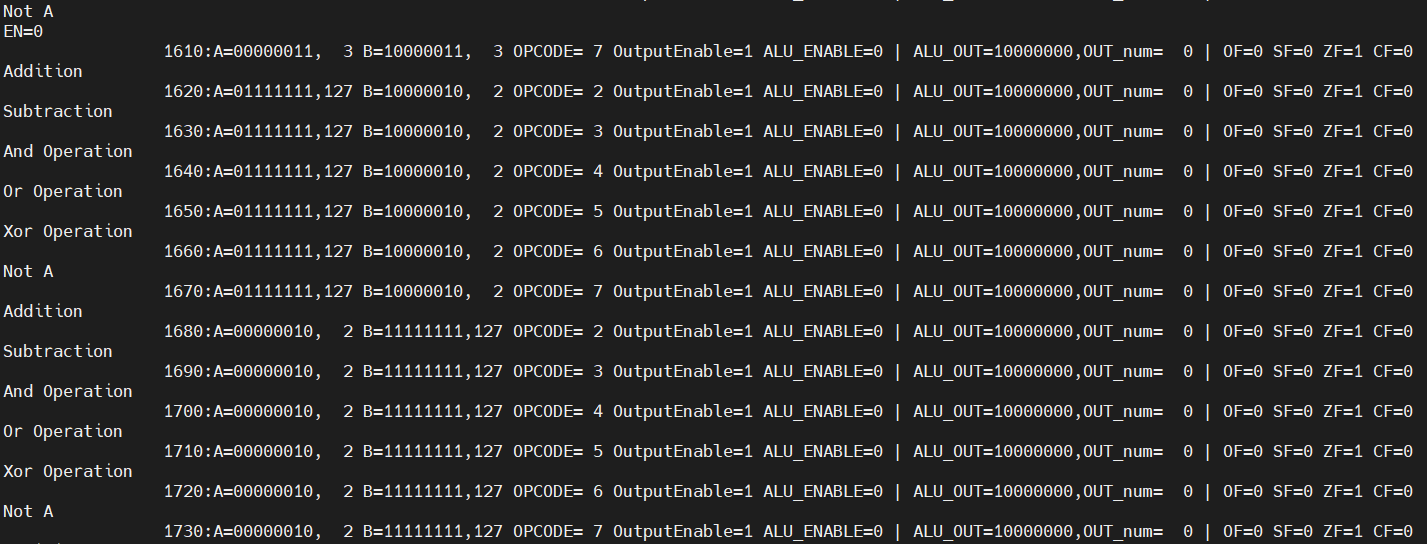
1. The 2 files were compiled using ‘vcs’ command.
2. ‘simv’ command was used to run the simulation.
3. ‘dve’ command was used to display the waveform of the simulation

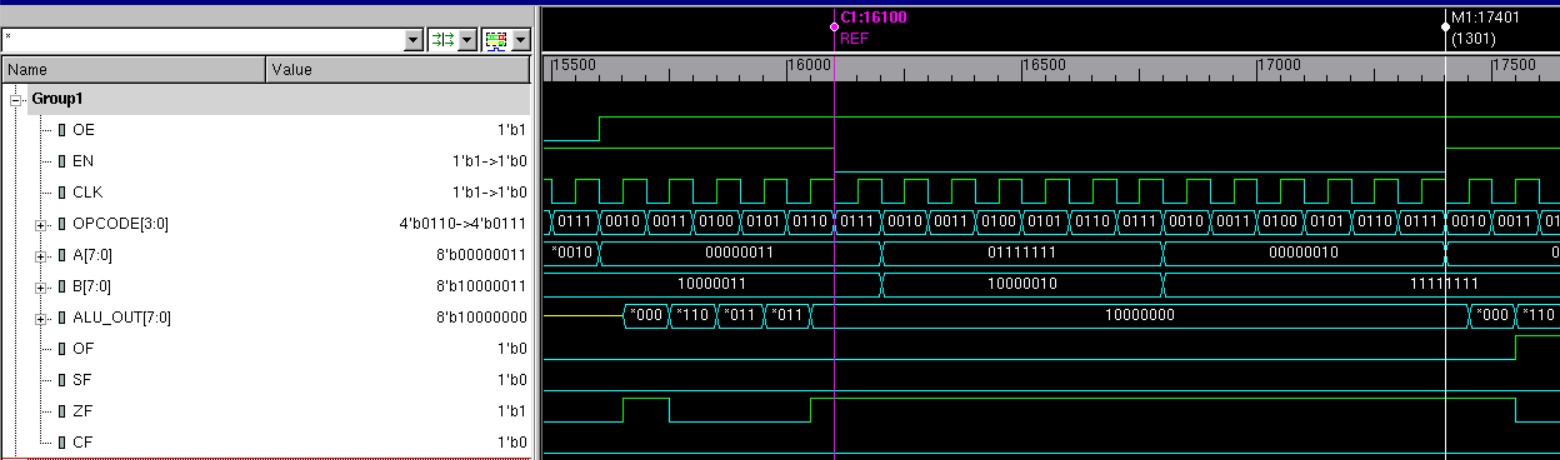
Two waveform view for signed and unsigned numbers were generated using the DVE graphical interface.

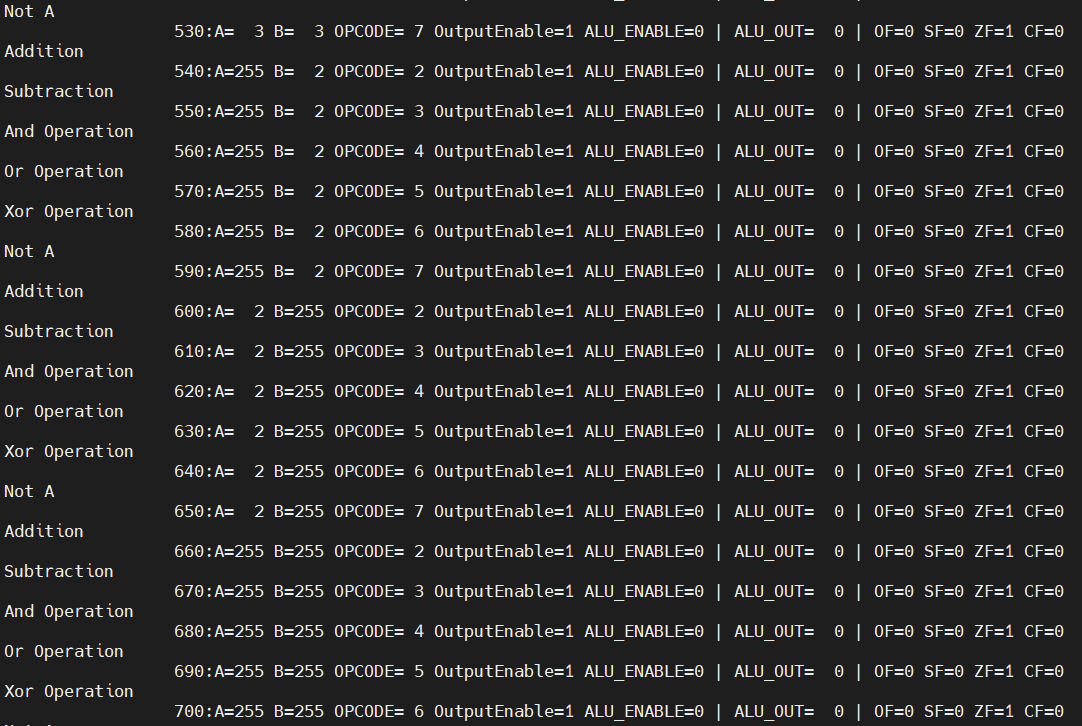
**Analysis of Results:**

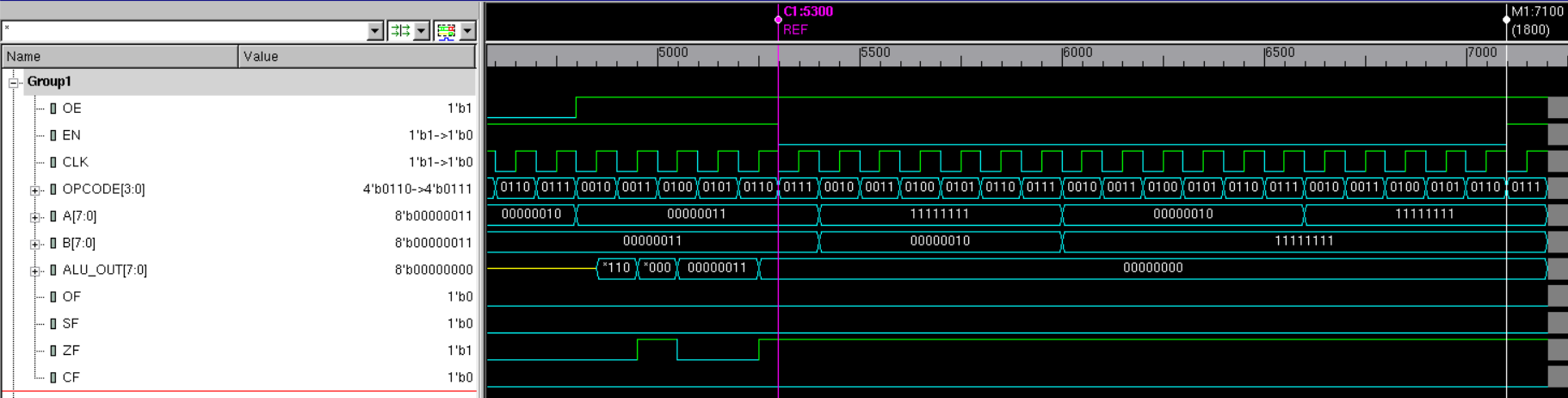
For signed numbers and unsigned numbers:

If EN is logic 0, the ALU will maintain its previous state.

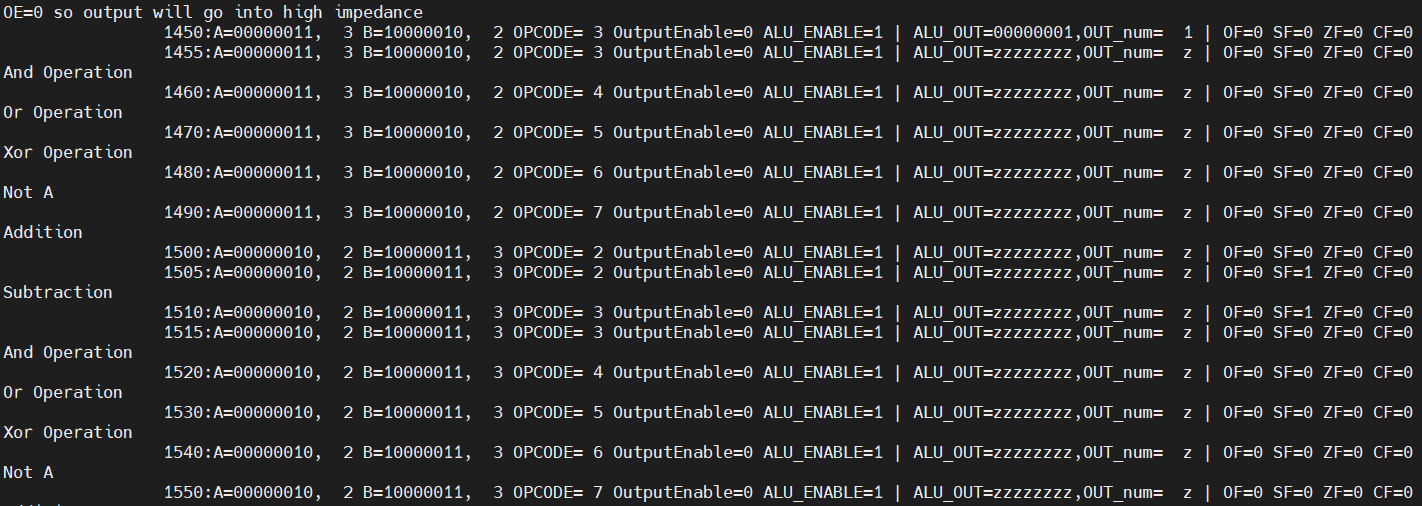


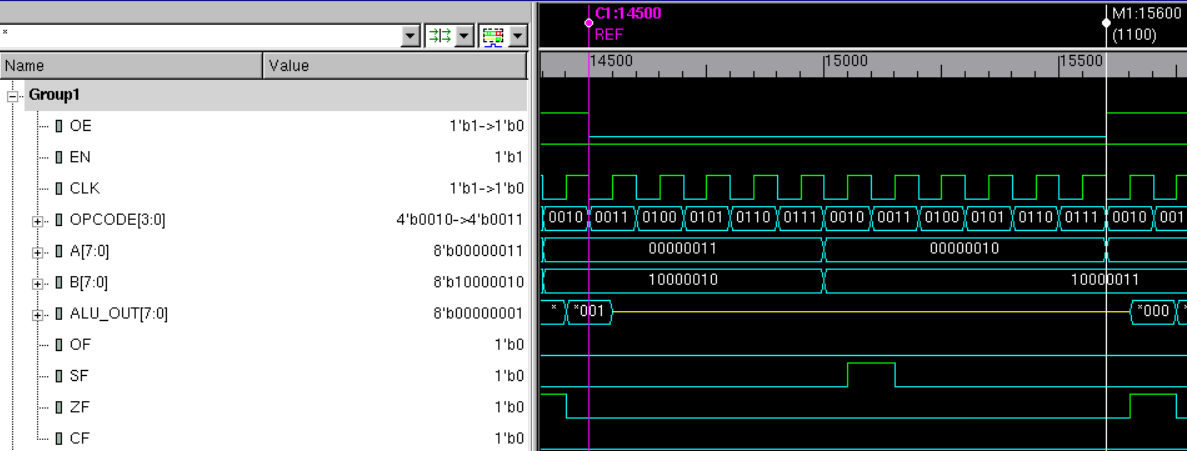


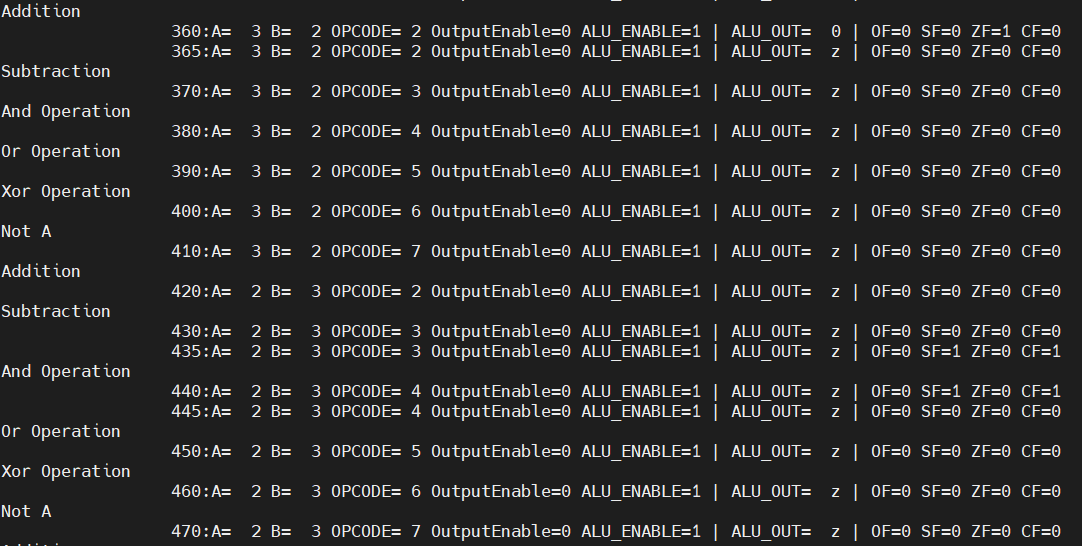


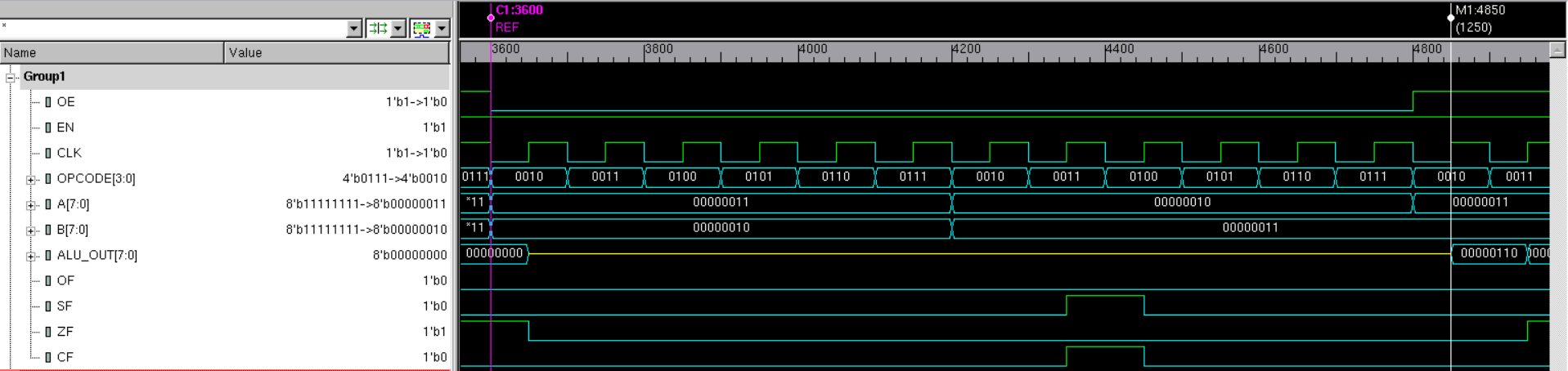


If OE is logic 0, the data outputs must all go to high impedance mode.



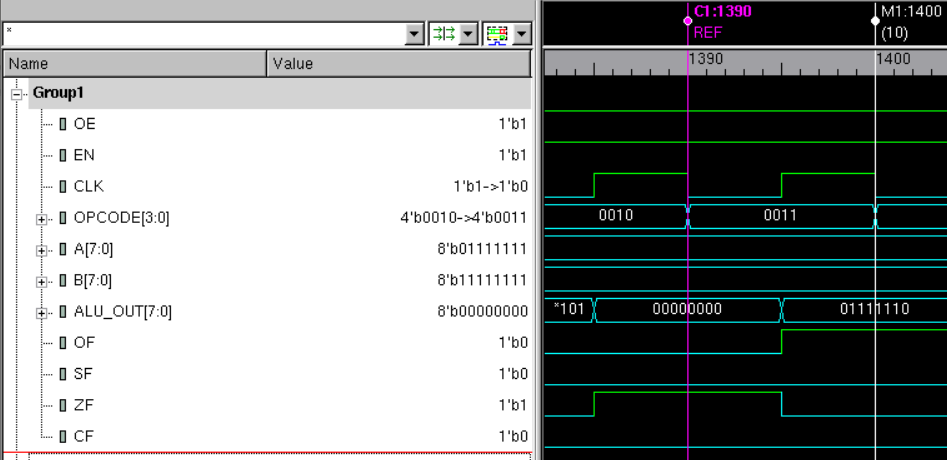






OverFlow condition:

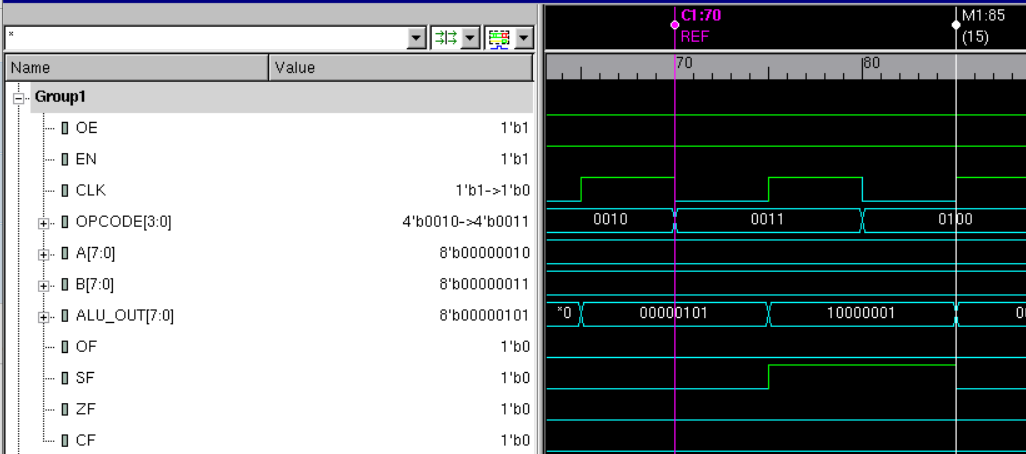
At 1390 ns OPCODE=0011 so it will do subtraction A=01111111 and B=11111111, so A=+127 and B=-127 output=127-(-127) = 254 so this will be a overflow condition.



SignFlag condition:

At 70ns A=00000010 and B=00000011 so A=2 and B=3 and opcode=0011 so subtraction

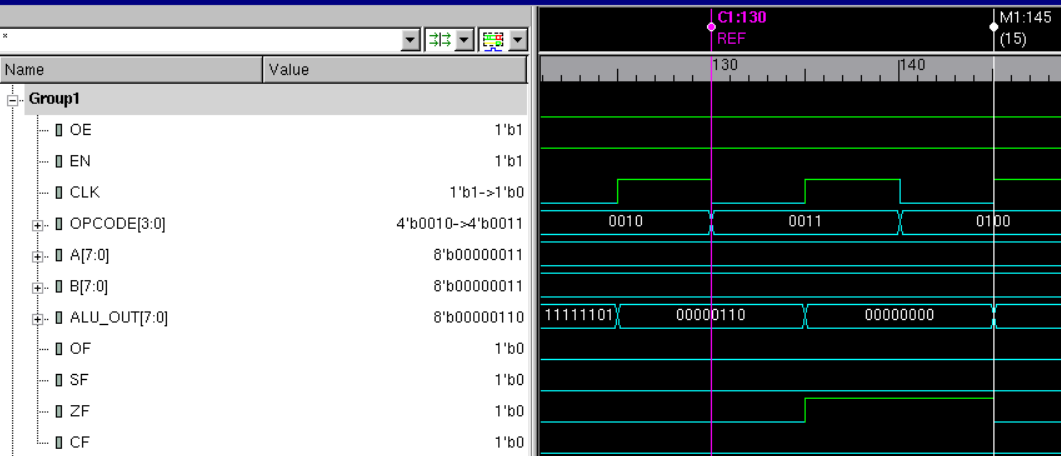
Output=2-3=-1



Zero Flag:

At 130ns A=00000011 and B=00000011 so A=3 and B=3 and opcode=0011 so subtraction

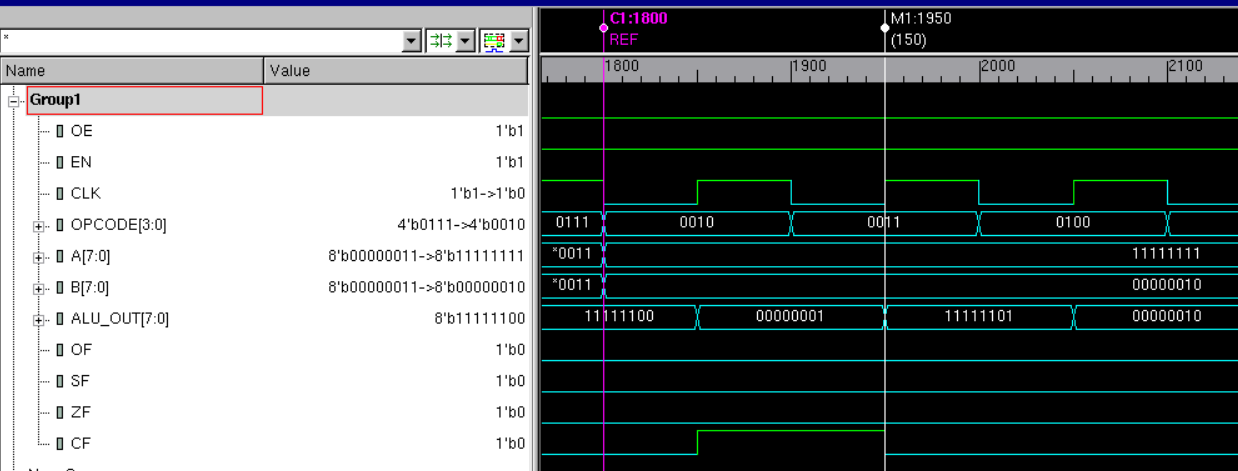
Output=3-3=0



Carry Flag:

At 180ns A=11111111 and B=00000010 so A=255 and B=2 and opcode=0010 so addition

Output=255+2=257



**Conclusion:**

Here we can conclude that The Zero flag is set when the result is all zeros for any ALU operation, The Negative flag is set when the MSB of the ALU output is logic one, for signed numbers, Carry is set when an addition or subtraction results in a carry out of the MSB position for unsigned numbers, Overflow is set when a signed operation was too big for the ALU.

I hereby attest that this lab report is entirely my own work. I have not copied either code or text from anyone, nor have I allowed or will I allow anyone to copy my work.

Name (printed) \_\_\_\_\_Jaymish Raju Patel\_\_\_\_\_\_\_\_\_

Name (signed) \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Date \_\_\_\_04/21/2021\_\_\_\_