**Experiment #9**

**Parameterized Synchronous FIFO**

Laboratory Report

Prepared for: ECE 526/L – Digital Design with Verilog and System Verilog Lab

Prepared by:

Jaymish Patel

**Introduction:**

The goal of this experiment is to create a module of FIFO using behavioral model that can be used for width and depth. Here instead of describing the actual hardware implementation of the circuit, the behavior of the input and output is used to create the model.

**Methodology:**

Two files were created using Verilog with names fifo.sv, and fifo\_tb.v. fifo.v for the behavioral description of a FIFO using ifdef, fifo\_tb.v consist of the Verilog test bench of Parameterized Synchronous FIFO.

fifo.sv and fifo\_tb.v programs were simulated using Synopsis VCS after completing the development of the two programs. VCS program was compiled using these 3 steps:

1. The 2 files were compiled using ‘vcs’ command.
2. ‘simv’ command was used to run the simulation.
3. ‘dve’ command was used to display the waveform of the simulation

Two waveform view for signed and unsigned numbers were generated using the DVE graphical interface.

**Analysis of Results:**

Writing data at all the locations from 20ns to 680ns.

When wr\_en is 1:

Background pattern

Description automatically generated

reading data from all the locations from 700ns to 1330ns.

When rd\_en is 1:

A picture containing timeline

Description automatically generated

At 610ns wr\_en is 1 and the element is added and the counter goes to 30 that is 2 less then total fifo size so almost\_full is 1.

At 650ns wr\_en is 1 and the element is added and the counter goes to 32 that is the total fifo size so full is 1.

At 670ns wr\_en is 1 and the counter is already 32 so overflow is 1 and the data\_in in neglected.

Graphical user interface

Description automatically generated

At 610ns rd\_en is 1 and the counter goes to 2 so almost\_empty is 1.

At 650ns rd\_en is 1 and the counter goes to 0 so empty is 1.

At 670ns rd\_en is 1 and the counter is already 0 so underflow is 1.

Graphical user interface

Description automatically generated

At 3340ns there is a write operation in between the reading operation. So 168 is inserted to the top.

Graphical user interface

Description automatically generated

At 3950ns 168 is obtained in the memory.

Graphical user interface

Description automatically generated

In normal case the first output is available after the 1st read operation.

A picture containing graphical user interface

Description automatically generated

In first word fall through the first output is available as soon as there is an element available in the memory.

Graphical user interface

Description automatically generated

**Conclusion:**

Here we can conclude that in normal case the first output is available after the 1st read operation but in first word fall through the first output is available as soon as there is an element available in the memory. The data inserted first is obtained first at the output.

I hereby attest that this lab report is entirely my own work. I have not copied either code or text from anyone, nor have I allowed or will I allow anyone to copy my work.

Name (printed) \_\_\_\_\_Jaymish Raju Patel\_\_\_\_\_\_\_\_\_

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