CP304: PROCESSOR ARCHITECTURES
CREDITS = 3 (L=3, T=0, P=0)

Course Objective:
To impart undestading of recent microprocessor architectures and develop capability of designing processor based systems.

Teaching and Assessment Scheme:

Teaching Scheme			Credits	Marks Distribution				Total Marks
				Theory		Practical		
L	T	P	C	ESE	CE	ESE	CE	
3	0	0	3	70	30	0	0	100

Course Contents:

Unit No.	Topics	Teaching Hours
1	**Intel 8086/8088 Architecture:** 8086/8088 Microprocessor MIN MODE Architecture, Pin Configuration, Programming Model, Memory Segmentation, Study of 8284 Clock Generator, Operating Modes, Timing diagrams for Read and Write operations, Interrupts, 8086 under Max Mode, 8288 Bus Controller.	09
2	**Instruction Set and Programming:** Instruction Set of 8086, Addressing Modes, Assembly Language Programming, Mixed Language Programming with C Language and Assembly Language.	06
3	**System designing with 8086:** Memory Interfacing: SRAM, ROM and DRAM, Applicationsof the Peripheral Controllers namely 8255PPI,8259PIC, Numeric Co-Processor 8087.	06
4	**Instruction level Parallelism**: Pipelining, basic concepts; Hazards, types of hazards, ways to overcome the hazards. Super-scaling, instruction issue policies, anti and output dependenecies, instruction commit and retire, Multithreading, Interleaved, Blocked, Simultaneous and Chip Multithreading**.** Architecture of Very Long Instruction Word (VLIW) processors.	09

Unit No.	Topics	Teaching Hours
5	**Pentium and Multi-Core Architectures:**:	
	Block Diagram, Signal Interfaces, Bus Cycles,Programming Model, Operating Modes, Address Translation, Mechanism in Protected Mode, Memory Management,Protection Mechanism,Superscalar Operation, Integer & FloatingPoint Pipeline Stages, Branch Prediction, Cache Organization, Multicore organizations, Case studies from recent processors.	09
6	**ARM Architecture:**	
	RISC Characteristics, Architecture inheritance, ARM programmer's model, ARM development tools, ARM organization and implementation, Instruction set: Data processing, Datatransfer, Control flow. Addressing modes. Writing simpleassembly language programs. Pipelining, Brief introduction to exceptions and interrupts handling.	06
	TOTAL	**45**

List of References:

1. Douglas Hall, "*Microprocessor and Interfacing*", Tata McGraw Hill.
2. Liu & Gibson, "*Microcomputer Systems: 8086/8088 family Architecture*", Programming and Design,PHI Publication.
3. Tom Shanley& Don Anderson, "*Pentium Processor System*",Architecture,AddisonWesley.
4. Daniel Tabak, "*Advanced Microprocessor*", Tata McGraw Hill.
5. Barry B. Brey, "*Intel Microprocessors*", Pearson Education.
6. William Stallings, "*Computer Organization and Architecture*" Pearson.
7. Kai Hwang & Naresh Jotwani, "*Advanced Computer Architecture*", Tata McGraw Hill.
8. Hamacher, Vranesic, Zaky, "*Computer Organization*", McGraw Hill.
9. Steve Furber, ARM system on chip architecture, Pearson.

Course Outcomes (COs): At the end of this course students will be able to

1. Understand the architecture and programming of 8086 microprocessor
2. Interface various peripherals with 8086 microprocessor
3. Understand the architectures of Pipelined and Superscalar Processors
4. Differentiate the multithreaded and multi-core architectures
5. Understand ARM architecture
6. Design Microprocessor based systems for various applications.