Jay Nathan

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Objective: Pursuing an MS in Computer Engineering in VLSI/IC Design with focus on low-power architectures, chip fabrication, and neuromorphic accelerators. Interested in research bridging RTL design, CAD flows, and AI/ML hardware co-design.

Education:

University of Illinois, Urbana-Champaign December 2025

(Bachelor of Science in Electrical Engineering with Minor in Computer Science)

Relevant Coursework:

- **Hardware:** Computer Organization & Design, Digital Systems, Digital IC Design, VLSI System Design, IC Device Theory and Fabrication, Semiconductor Devices, Digital Signal Processing, Analog Signal Processing, Electronic Circuits
- **Software:** Operating Systems, Data Structures & Algorithms, Computer Systems & Programming
- **AI/ML:** Artificial Intelligence, Sensor Fusion, Applied Machine Learning, Deep Learning for Computer Vision Systems

Work Experience:

Researcher:

Autonomous & Unmanned Vehicle Systems Laboratory **(AUVSL), UIUC** **May 2023 - 2025**

Center for Autonomous Construction and Manufacturing at Scale, **UIUC** **May 2023 - 2025**

- Worked with the team to design and implement outdoor robot localization solution leveraging Ultrawide-Band Antennas by **Writing Python & C++ packages**, deployed on the Clearpath Husky & Jackal platforms.
- **Developed PyTorch scripts** to tune Adaptive Neural Fuzzy Inference System parameters, worked on a **custom Unscented Kalman Filter (UKF)** for sensor fusion with UWB, IMU, and wheel encoders, to reduce drift
- Utilized Python to write localization software and scripts **utilizing popular libraries to analyze and process sensor data**.

HARDWARE SYSTEMS PROJECT EXPERIENCE

Advanced VLSI System Design Project (ECE 427): Aug 2025

(Sponsored by TSMC, MUSE semiconductor and UIUC Grainger School)

Designed, implemented and fabricated, a RISC-V System-on-Chip (SoC) with hardware-accelerated AES-128 encryption and LZ77/DEFLATE compression in ECE 427 at UIUC. Contributed RTL design for accelerators, integrated custom instruction-set extensions into a 32-bit RISC-V core, and developed mixed analog/digital I/O subsystems within 1 mm^2/50 mW constraints. This platform is extended with custom Instruction Set In-line Processing (ISIP) blocks to achieve significant performance improvements for security and data efficiency in IoT and edge inference applications. This project is sponsored and selected by **TSMC** for fabrication, validating technical rigor and real-world relevance for secure, low-power IoT and edge computing applications.

Senior Research Project & Senior Thesis (ECE 496 + ECE 499): Jan 2025 - May 2025

Currently designing a hardware accelerator for a neuromorphic processor under Professor Anu Aggarwal at UIUC's Grainger College of Engineering. Focused on low-power architectures to accelerate AI/ML workloads such as gradient descent, matrix

multiplication, and sparse linear algebra, with responsibilities spanning design, architectural exploration, and optimization for parallelism and energy efficiency.

RV32IM N-Way Superscalar Out-of-Order Explicit Register Renaming-Based CPU (ECE 411) May 2024

- Designed & verified from scratch an out-of-order N-way parameterizable processor for RISC-V 32-bit ISA with M-extension, achieving IPC of 0.51 on standard benchmark taking 21.7 mW of power at clock frequency 325 MHz.
- Implemented speculative branching with branch prediction overriding, & perceptron and Gshare branch predictors.
- Implemented cache features including next-line & stride prefetchers, post-commit store buffer with write coalescing.
- Integrated Synopsys IPs including sequential divider and wrote Dadda advanced multiplier and shift-add multiplier.
- Wrote full processor in SystemVerilog, simulated with Synopsys VCS, debugged with Synopsys DC, Verdi, Spike, RVFI, Lint, Functional Coverage, Used Python to generate test programs, built toolchains with bash, GNU make.

Bitsliced RV32I CPU in Cadence Virtuoso (ECE 425 and ECE 482) Apr 2025

- Authored FreePDK 45nm standard library (logic, muxes, flip-flops) with schematic, layout, and Liberty timing views.
- Manually laid out in Virtuoso a complete 32-bit RISC-V RV32I pipeline using a bitsliced methodology in a hierarchical library, complete with ALU, write-low/read-high register file, barrel-shifter, and cascaded comparator.
- Verified extracted netlist with SystemVerilog harness, passing reference, and self-written RV32I assembly suites.
- Wrote Tcl scripts for Innovus to make 2nd processor in addition to the manual layout to automate the layout process & minimize area for the entire processor, including floorplanning, placement, routing, & DRC/LVS checks.

IC Fabrication – (ECE 340 and ECE 444) Course-Based Project at UIUC Dec 2024

- Independently processed a silicon wafer from start to finish in an industrial cleanroom environment, performing every step—from RCA cleaning and oxidation to photolithography, etching, doping, and final metal lift-off.
- Utilized a five-mask sequence to fabricate complex devices (MOSFETs, BJTs, diodes, logic gates).

AI/ML PROJECT EXPERIENCE

Machine Learning & AI Research – CACMS & AUVSL Jan 2024 – May 2025

- Researched and adapted the **MOSTS trajectory-smoothing algorithm** for multi-robot navigation, improving stability and reducing path error.
- Built automated pipelines to generate and preprocess **4,000+ synthetic terrain images** (snow, mud, rocky) with diffusion models, rotation/cropping, and **HDF5 dataset packaging with labels/timestamps**.
- Developed and trained **CNN models (EfficientNet-B0, MobileNetV3)**, achieving **99.3% accuracy** and **95.8% recall on snow terrain**, with performance on external datasets.
- Implemented an **Unscented Kalman Filter** for real-time sensor fusion (UWB + IMU + encoder), and optimized model deployment by exporting to **ONNX Runtime with DirectML**, reducing inference latency from **16.3 ms → 7.1 ms (~2.3× faster)** for **140 FPS real-time performance**
- My early research trajectory was shaped under the guidance of the late Professor William Robert "Bob" Norris at these laboratories, where I first engaged in AI/ML research for autonomous systems. His mentorship instilled the research curiosity that continues to guide my work.

Artificial Intelligence Algorithms & Applications (CS 440) Apr 2024

- Implemented **Naive Bayes classifier** for text classification with smoothing and feature selection.
- Developed *search algorithms (DFS, BFS, A, UCS)** for pathfinding and planning.
- Built **HMM-based part-of-speech tagger** using Viterbi decoding, improving sequence labeling accuracy.
- Designed a hardware-accelerated Deep Neural Network for AMD PYNQ-Z2 FPGA using Xilinx Vivado HLS.
- Designed **Q-learning reinforcement learning agent** in Python/PyTorch for Atari-style environments.

Applied Machine Learning Systems (CS 441) **Apr 2024**

- Applied ML techniques to **classification, regression, clustering, and graphical models** across vision and language domains.
- Implemented **logistic regression and SVM classifiers** with regularization and cross-validation.
- Designed and trained **CNNs in PyTorch/TensorFlow**, achieving ~79% accuracy on CIFAR-10–like datasets.
- Applied **gradient descent optimization** (SGD, momentum, learning rate scheduling) for faster convergence.
- Explored **advanced ML techniques**, including **Mean Field methods, Variational Auto-Encoders (VAEs), and Hidden Markov Models (HMMs).**

SOFTWARE PROJECT EXPERIENCE

Unix-Like Operating System **Dec 2023**

- Engineered a UNIX-like, single-core kernel for 32-bit hardware fully from scratch using C and x86 Assembly.
- Implemented a paging-only virtual memory system, writable file system, software context switching, terminal switching, and hardware interrupts and exception handling.
- Developed device drivers for keyboard, mouse, real-time clock, & built interactive shell for executing system calls.
- Used advanced GDB techniques to efficiently debug and resolve system-level issues.
- Emulated and tested the OS in a QEMU virtual environment, ensuring safe and efficient debugging.

Technical Skills:

Languages: C++, C, C#, Python, Java, Matlab, x86 Assembly, RISC-V ISIP, System Verilog

Hardware: (Board Bringup/Programming):
AMD/Xilinx FPGA (VIVADO environments), Intel/Altera Stratix FPGA/SoC series (RISC-V CPU designs)
Tools/Environments: CUDA, DOCA, GDB, Linux, Bash/Shell, TCL, Git, Docker, Jenkins, Make, Vim, QEMU, Anaconda/Jupyter, Docker,Github/Gitlab, LaTeX
Libraries: Tensorflow, Keras, PyTorch, NumPy, SciPy, Scikit-Learn, OpenCV, Pandas
EDA/RTL DV: SystemVerilog, SV Coverage, Intel Quartus, AMD Xilinx, Chisel, HLS, PyRTL, Veryl, Synopsys DC & VCS, Verdi, Spyglass, ModelSim/QuestaSim, Verilator, Chipyard, Cadence Virtuoso & Innovus, Cocotb, Gem5, UVM
Interfaces & Test Methodologies: AXI, UART, SPI, I2C, I2S, CAN, JTAG, ATPG, BIST, ATE, TCP/IP
Other: ROS ½, RViz, Gazebo, RPi, Arduino, Simulink, Unity, Eagle CAD, Autodesk Inventor, SolidWorks

References:

- Professor Anu Aggarwal **(ECE Department, The Grainger College of Engineering, UIUC**)
- **Paul J Froeter (ECE Department/Nanotechnology Lab, The Grainger College of Engineering, UIUC)**
- **I-Chen Sang, Post Doc Research Assistant, CACMS, The Grainger College of Engineering UIUC)**
- **Hsiao-Yu Chen, Ph.D candidate CACMS, The Grainger College of Engineering UIUC)**
- **Rajiv Sharma (Industry mentor) LPU (Language Processing Unit ASIC) Senior Engineering Lead at GROQ**

Appendix A

UIUC BSEE Major & CS Minor List of Courses Taken

Math Courses:

- **MATH 213:** Introduction to Discrete Math
- **MATH 257:** Linear Algebra w/ Computational Applications

Physics Courses:

- **PHYS 212:** Electricity & Magnetism
- **PHYS 213:** Thermal Physics
- **PHYS 214:** Quantum Physics

Computer Science Minor Core Courses:

- **CS 101:** Intro to Computing
- **CS 225:** Data Structures
- **CS 441:** Applied Machine Learning

Electrical Computer Engineering Core Courses:

- **ECE 110:** Introduction to Electronics
- **ECE 120:** Introduction to Computing
- **ECE 210:** Analog Signal Processing
- **ECE 220:** Computer Systems & Programming
- **ECE 310:** Digital Signal Processing:
- **ECE 313/314:** Probability w/ Engineering Applications; Probability in Engineering Lab
- **ECE 329:** Fields & Waves
- **ECE 340:** Semiconductor Devices
- **ECE 342/343:** Electronic Circuits; Electronic Circuits Lab
- **ECE 385:** Digital Systems Laboratory
- **ECE 391:** Computer Systems Engineering

ECE Graduate Level Courses:

- **ECE 411:** Computer Organization & Design
- **ECE 425:** Introduction to VLSI System Design
- **ECE 427:** Advanced VLSI System Design
- **ECE 482:** Digital IC Design
- **ECE 448/CS 440:** Artificial Intelligence
- **ECE 444:** IC Device Theory & Fabrication
- **ECE 496:** Senior Research Project **(Neuromorphic VLSI Chip Design)**
- **ECE 499:** Senior Thesis **(Neuromorphic VLSI design)**
- **ECE 445:** Senior Design Project Laboratory**(Design and Fabrication of portable Medical Device)**