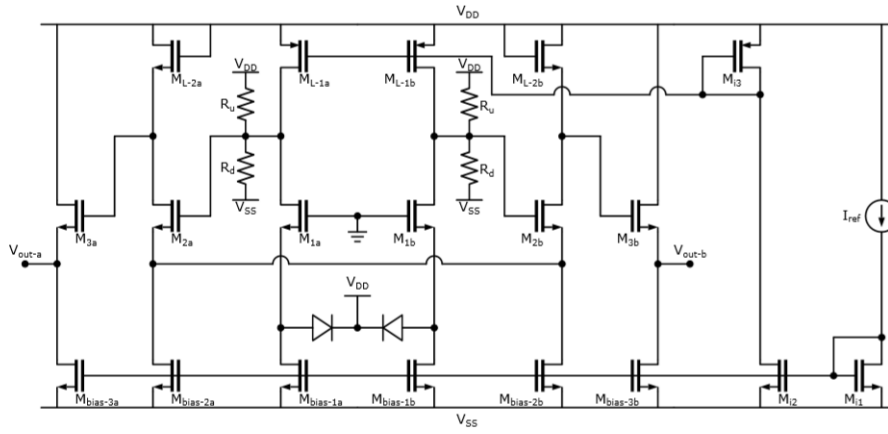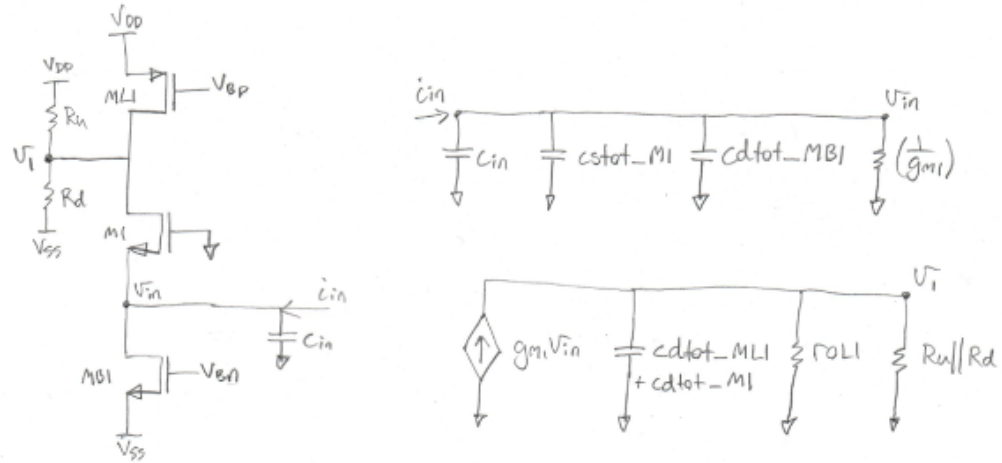# EE214A Design Project

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The amplifier under evaluation has 3 stages: Common Gate (CG), Common Source (CS), and Common Drain (CD). In order to analyze, the circuit is broken down into its 3 stages and key parameters are summarized.

Parameter	Spec
Transresistance gain	42.5k
Output load resistance	20k
Output load capacitance	250fF

Common Gate:

Low Frequency Characteristics	
Transimpedance Gain	R_u parallel R_d
Rin	1/gm1
Rout	high

Common Source:

The source of the common source stage is referenced to virtual, small-signal ground in the DM half circuit.
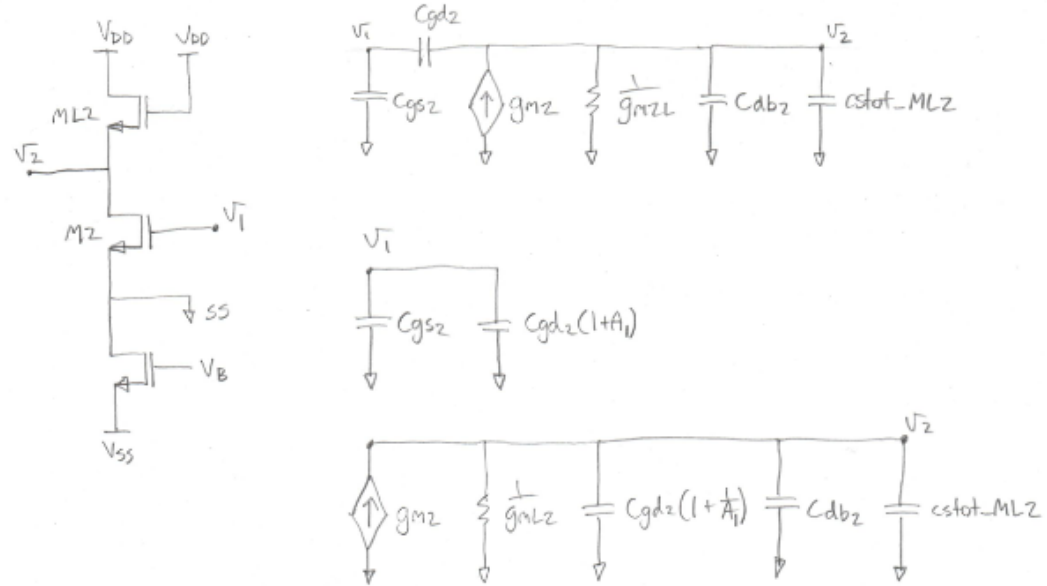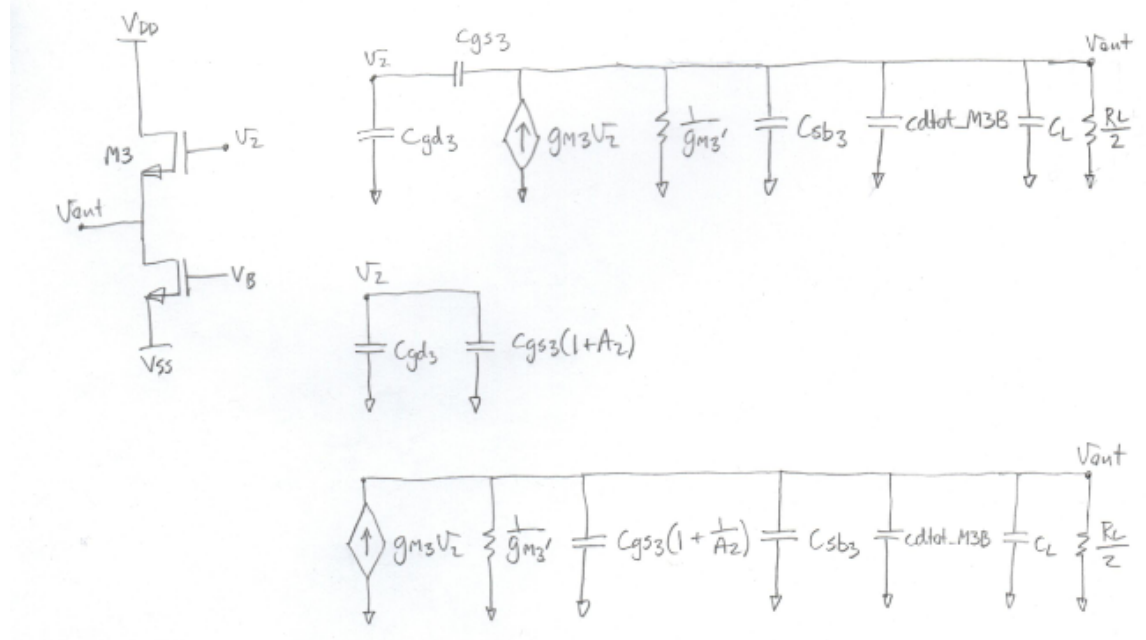

Where:

$$A_1 = \frac{gm_2}{gm_{L2}} \tag{1}$$

Low Frequency Characteristics	
Av	$-gm_2 * R_{L2}$
Rin	inf
Rout	$1/gm_{L2}$

Common Drain:

Where:

$$C_L = 250 fF \tag{2}$$

$$R_L = 20 k\Omega \tag{3}$$

Assuming $R_L/2$ much less than $1/gm3$

$$A_2 \approx -\frac{g_{m3}}{g'_{m3}} \approx -0.84 \tag{4}$$

Low Frequency Characteristics	
Av	approx. 0.84
Rin	inf
Rout	$1/gm_3$'

Low Frequency Transimpedance Gain:

$$\frac{v_{out}}{i_{in}} = (R_u || R_d) * (-\frac{gm_2}{gm_{L2}}) * 0.84 \tag{5}$$

TIA Amp Small-Signal Model
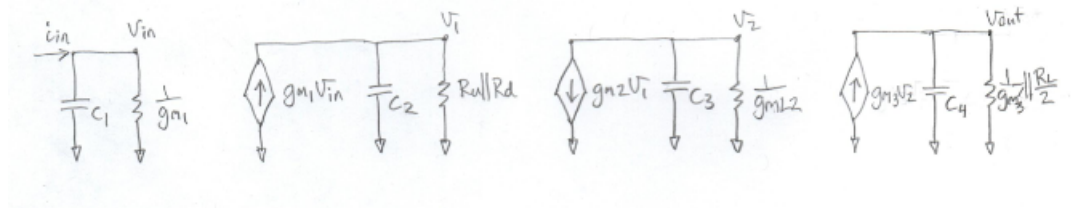
ZVTC bandwidth (conservative approximation)

$$b1 = \frac{1}{g_{m1}} * C_1 + (R_u || R_d) * C_2 + gm_{L2} * C_3 + (gm_3' || R_L/2) * C_4 \tag{6}$$

where

$$C_1 = 100fF + cstot\_M1 + cdtot\_MB1 \tag{7}$$

$$C_2 = cdtot\_ML1 + cdtot\_M1 + C_{gs2} + (1 + A_1) * C_{gd2} \tag{8}$$

$$C_3 = (1+1/A_1)*C_{gd2}+C_{db2}+cstot\_ML2+C_{gd3}+(1+A_2)*C_{gs3} \tag{9}$$

$$C_4 = (1 + 1/A_2) * C_{gs3} + C_{sb3} + cdtot\_M3B + 500fF \tag{10}$$

Where:

$$A_1 = \frac{gm_2}{gm_{L2}} \tag{11}$$

$$A_2 \approx -\frac{g_{m3}}{g_{m3}'} \approx -0.84 \tag{12}$$