Introduction

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| **Parameter** | **Specification** |
| Operating temperature | 25 °C |
| VDD / VSS | ±2.5 V |
| RIN half circuit | Inf |
| CIN half-circuit | 100 fF |
| ROUT half circuit | 10 kΩ |
| COUT half-circuit | 500 fF |
| CM output voltage | ±0.5 V |
| Power dissipation | ≤2 mW |
| Small-signal transresistance gain | ≥40 kΩ |
| Freq resp characteristics | 1 domant pole |
| -3 dB bandwidth | ≥75 MHz |
| Figure of Merit FOM | ≥(40 x 75)/2 = 1,500 kΩ MHz/mW |
| **Additional Design Parameters** | **Specification** |
| L current mirror | ≥ 2 um |
| Vov,min | 150 mV |
| Size increments | 0.2 um |
| Max current mirror ratio | 20 |

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| **Schematic** | **SS model** |
| Common Gate (simple) |  |
| Common Source (simple) |  |
| Common Drain (simple) |  |

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| **stage** | **gain** | **units** |
| CG | RU||RD | V/A |
| CS | -A1 = Vov2L/Vov2 | V/V |
| CD | -A2 | V/V |

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| **Req** | | | | |
| RIN | | R1 | inf |  |
| CG | RCG,IN | 1/gm1’ | 0.84\*(Vov1/2ID1) |
| RCG,OUT | R2 | ro1||RU||RD | 20/ID1||RU||RD |
| CS | RCS,IN | inf | Inf |
| RCS,OUT | R3 | 2ro2||(1/gm2L’) | 2ro2||0.84\*(A2\*Vov2/2ID2) |
| CD | RCD,IN | Inf | inf |
| RCD,OUT | R4 | 2ro3||(1/gm3’) | 2ro3||0.84\*Vov3/2ID3) |
| ROUT | | 10 kΩ |  |

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| **Ceq** | | | | |
| CIN | | C1 | 100 fF |  |
| CG | CCG,IN | Cgs1 + Csb1 |  |
| CCG,OUT | C2 | Cgd1 + Cdb1 |  |
| CS | CCS,IN | Cgs2 + Cgb2 + (1+A1)Cgd2 |  |
| CCS,OUT | C3 | (1+1/A1)Cgd2+ Cdb2 |  |
| CD | CCD,IN | Cgd3 + Cgb3 + (1+A2)Cgs3 |  |
| CCD,OUT | C4 | (1+1/A2)Cgs3 + Csb3 |  |
| COUT | | 500 fF |  |

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| **A** | **equation** | **pole location** | **gain** |
| i1/iin | 1 / (1+sR1C1) | P2 = -1/R1C1 | 1 |
| v1/i1 | R2 / (1+sR2C2) | P2 = -1/R2C2 | R2 |
| v2/v1 | -A2 R3 / (1+sR3C3) | P3 = -1/R3C3 | Vov2L/Vov2 |
| vo/v2 | gm3 R4 / (1+gm3 R4+sR4C4) | P4 = -(1+gm3 R4)/R4C4 | gm3 R4/(1+gm3 R4) |

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| **Stage** | **Input variables** |
| CG | Vov1 |
| ID1 |
| RU||RD |
| CS | Vov2 |
| ID2 |
| A1 |
| CD | Vov3 |
| ID3 |

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| **Power Consumption** | |
| VSUPPLY | VDD - VSS |
| Power I\_ref | I\_ref\*VSUPPLY |
| Power Resistor | 2\*(RU + RD)\*VSUPPLY |
| ID,Total | 2\*(ID1 + ID2 + ID2) |
| ratio\_1 | ID1 / ID3 |
| ratio\_2 | ID2 / ID,Total |
| ID1 | ID,Total [ (ratio\_1)\*(1 - ratio\_2) ] / [ 1 + ratio\_1 ] |
| ID2 | ID,Total ratio\_2 |
| ID3 | ID,Total [ (1 – ratio\_2) / (1 + ratio\_1) ] |
| RL,CG | RU||RD |
| RU | RL,CG ( 5 / (2.5+V1) ) |
| RD | RL,CG ( 5 / (2.5 -V1) ) |

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| **Pole Locations** | |
| P1 |  |
| Vov1 |  |
| Vov1 |  |
| Id\_1 |  |
| Id\_2 |  |
| Id\_3 |  |
| A2 = (VovL2 / Vov2) |  |
| R = RU||RD |  |

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| **Equations** | | |
| 1/gmL2 | VovL2/(2Id) | (A2\*Vov2)/(2Id) |
| Vov1 |  |  |
| Vov1 |  |  |
| Id\_1 |  |  |
| Id\_2 |  |  |
| Id\_3 |  |  |
| A2 = (VovL2 / Vov2) |  |  |
| R = RU||RD |  |  |

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| **HSpice .op outputs** | |
| cgs | Cgs |
| cgd | Cgd |
| cgtot | Cgs + Cgd + Cgb |
| cdtot | Cgd + Cdb |
| cstot | Cgs + Csb |
| cbtot | Cgb + Csb +Cdb |
| **Other way** | |
| Cgs | cgs |
| Cgd | cgd |
| Cgb | cgtot – cgs – cgd |
| Csb | cstot – cgs |
| Cdb | cdtot – cgd |

Common Drain:

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