EE214A 2019 Project Report

Differential Transimpedance Amplifier Design

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Design Overview:

The topology of the transimpedance amplifier (TIA) is fixed and the design is driven by gain, bandwidth, and power constraints as well as biasing and output CM voltage considerations.

The specification of the application shown in table 1 and a comparison of the specified performance compared with the achieved design performance is presented in table 2.

Table 1. Design Constraints

|  |  |
| --- | --- |
| **Parameter** | **Specification** |
| Operating temperature | 25 °C |
| VDD / VSS | ±2.5 V |
| RIN half circuit | Inf |
| CIN half-circuit | 100 fF |
| ROUT half circuit | 10 kΩ |
| COUT half-circuit | 500 fF |

Table 2. Specifications and Achieved Design Performance

|  |  |  |  |
| --- | --- | --- | --- |
| **Parameter** | **Specification** | **Design Performance** | **Agreement** |
| CM output voltage | ±0.5 V | -0.499 V | Meets spec |
| Power dissipation | ≤2 mW | 1.59 mW | Meets spec |
| Small-signal transresistance gain | ≥40 kΩ | 40.07 | Meets spec |
| Freq resp characteristics | 1 domant pole | Dominant pole freq ~= ½ of next 3 poles. Roll-off never levels off at 20dB. | Does not meet spec |
| -3 dB bandwidth | ≥75 MHz | 76.9 MHz | Meets spec |
| Figure of Merit FOM | ≥(40 x 75)/2 = 1,500 kΩ MHz/mW | 1939 | Meets spec |
| **Additional Design Parameters** | **Specification** | **Design performance** | **Agreement** |
| L current mirror | ≥ 2 um | L = 2u for current mirrors | Meet spec |
| Vov,min | 150 mV | Vov’s > 0.2v | Meets spec |
| Size increments | 0.2 um | yes | Meets spec |
| Max current mirror ratio | 20 | 3.1 | Meets spec |

Design Outcome

To avoid redundancy between the A and the B side of the amplifier shown in figure 1, the component values, voltages, and currents are presented on a simplified half circuit in figure 2.

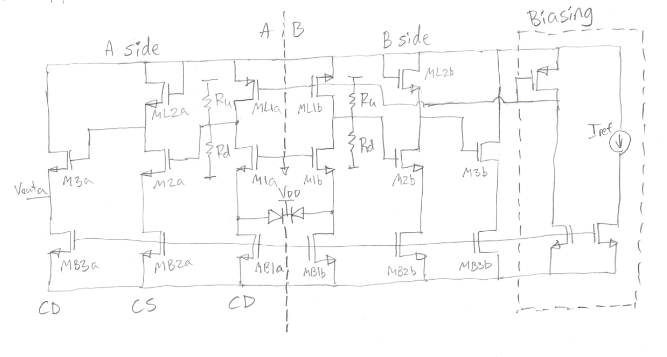


Figure 1

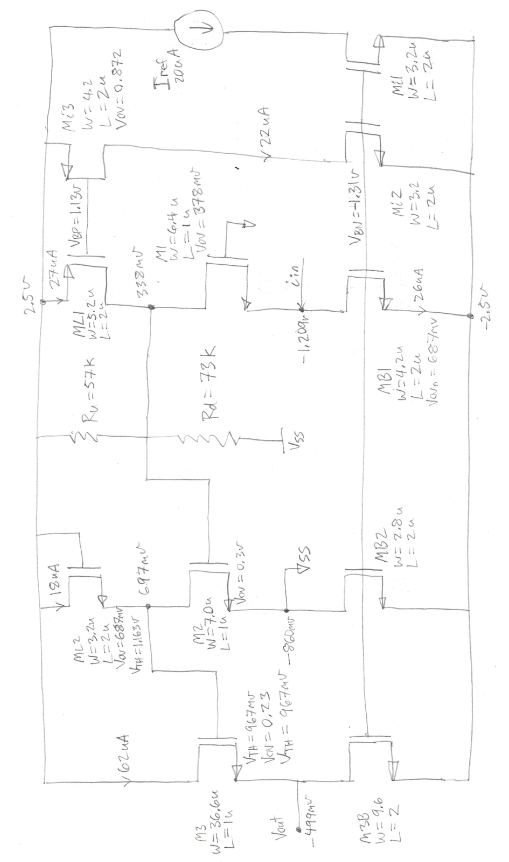


Figure 2

The Transient response is shown

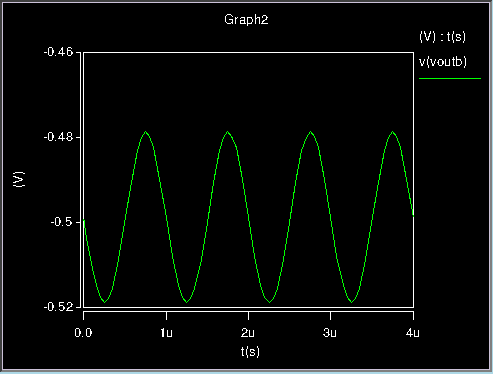
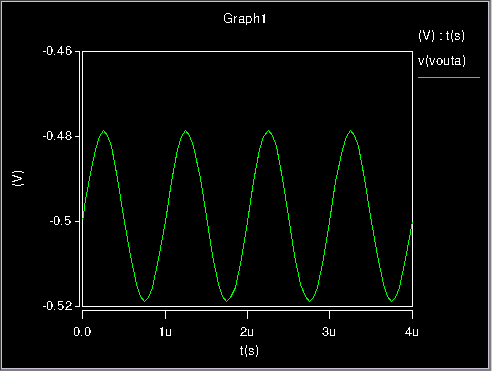


Figure 3. v\_outa Figure 4. v\_outb

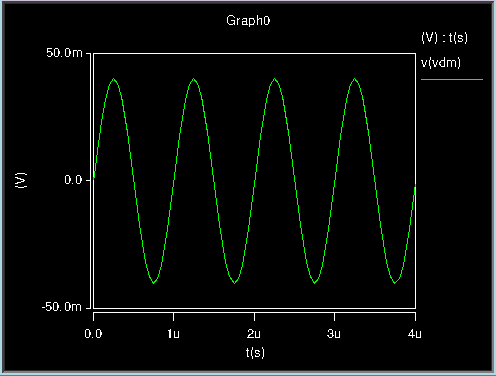
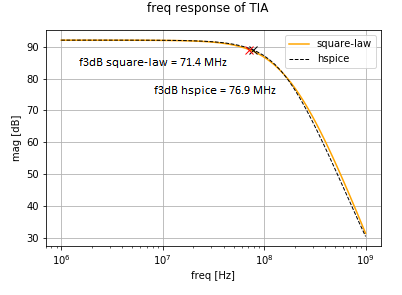
 

Figure 5. v\_out\_dm Figure 6. Freq response

**Design Methodology**

General overview:

1. Break down into stages and do hand calculations to get general intuition
   1. Identify need for optimization code
2. Python simulation
   1. Simulate stages independently
      1. Rin, Rout, Cin, Cout
      2. Gain
      3. Power consumption
      4. Biasing considerations
   2. Calculate total gain and BW
      1. 4 pole model
      2. DC gain
3. Sweep parameters and identify the dominant optimum
   1. Found an optimum between gain and bandwidth that seemed far too good to be true. Tried it in Hspice and the CM output voltage came out too low because M3 and ML2 are in body effect increasing their Vth and decreasing the voltage headroom for Vov3 and VovL2.
   2. Added constraint to the code and found optimum which only gets 2 V/V of gain from the CS stage, 0.7 V/V from the CD stage and most of the gain comes from the CG stage. This in turn increases the

Single-stage hand calculations:

The full small signal models and derivations can be found in Appendix A. The key results are shown below

|  |  |  |
| --- | --- | --- |
| **stage** | **DC gain** | **units** |
| CG | ro1||RU||RD | V/A |
| CS | -0.84\*Vov2L/Vov2 | V/V |
| CD | gm3 RCD,OUT | V/V |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Req** | | | | | **Approximate** |
| RIN | | R1 | inf |  | |
| CG | RCG,IN | (ro1 + 2RU||RD) / gm1’(ro + RU||RD) | 1 / gm1’ | |
| RCG,OUT | R2 | ro1||RU||RD | RU||RD | |
| CS | RCS,IN | Inf | Inf | |
| RCS,OUT | R3 | 0.5ro2 / (1 + 0.5gm2L’ro2) | 1 / gm2L | |
| CD | RCD,IN | Inf |  | |
| RCD,OUT | R4 | (1 / gm3’) || 0.5 ro3 || ROUT | 1 / gm3’ | |
| ROUT | | 10 kΩ |  | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Ceq** | | | | |
| CIN | | C1 | 100 fF |  |
| CG | CCG,IN | Cgs1 + Csb1 | Cgs1 + Csb1 + Cgd1B + Cdb1B |
| CCG,OUT | C2 | Cgd1 + Cdb1 | Cgd1 + Cdb1 + Cgd1L + Cdb1L |
| CS | CCS,IN | Cgs2 + (1+A1)Cgd2 | Cgs2 + (1+A1)Cgd2 |
| CCS,OUT | C3 | (1+1/A1)Cgd2 + Cdb2 + Csb2L + Cgs2L |  |
| CD | CCD,IN | Cgd3 + (1+A2)Cgs3 |  |
| CCD,OUT | C4 | (1+1/A2)Cgs3+ Csb3 + Cgd3B + Cdb3B + COUT |  |
| COUT | | 500 fF |  |

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **equation** | **pole location** | **gain** |
| i1/iin | 1 / (1+sR1C1) | P2 = -1 / R1C1 | 1 |
| v1/i1 | RCG,OUT / (1+sR2C2) | P2 = -1 / R2C2 | RCG,OUT |
| v2/v1 | -A1 / (1+sR3C3) | P3 = -1 / R3C3 | 0.84\*Vov2L/Vov2 |
| vo/v2 | -A2 / (1+sR4C4) | P4 = -1 / R4C4 | gm3 R4/(1+gm3 R4) |

Python code:

Sweep class

Tia: CG, CS, CD, PCM, CM:

1. Takes input parameters from sweep class

|  |  |
| --- | --- |
| Vov\_1 | 0.378 |
| Vov\_2 | 0.297 |
| Vov\_3 | 0.229 |
| Vov\_N | 0.687 |
| Vov\_P | 0.870 |
| Ru | 57 |
| Rd | 73 |
| Id\_1 | 26u |
| Id\_2 | 18u |
| Id\_3 | 62u |
| ratio\_1 | 0.42 |
| ratio\_2 | 0.20 |

In order to understand the topology, the amplifier was first broken down into simpler pieces.

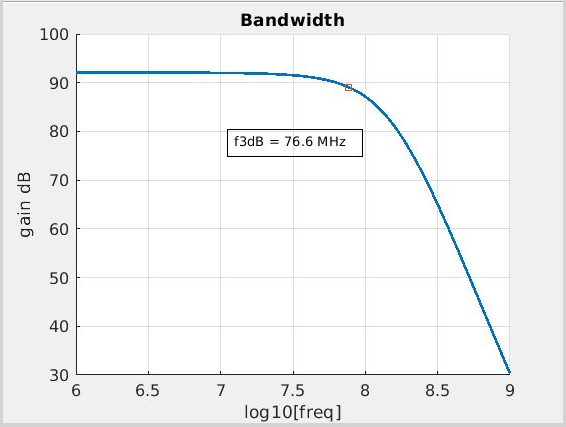
First, the A and B sides are have symmetric component values, voltages and currents and can be analyzed as a half circuit.

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **mosfets** | **M1L** | **M1** | **M1B** | **M2L** | **M2** | **M2B** | **M3** | **M3B** | **Mi1** | **Mi2** | **Mi3** |
| Vov | 0.63 | 0.4 | 0.5 | 0.67 | 0.32 | 0.72 | 0.26 | 0.72 | 0.71 | 0.71 | 0.6 |
| Id | 26 | 26 | 26 | 18 | 18 | 18 | 62 | 62 | 20 | 20 | 20 |
| type | 1 | 6 | 2 | 2 | 1 | 2 | 1 | 2 | 2 | 2 | 6 |
| WL | 2.6 | 6.4 | 4.2 | 1.6 | 7 | 1.4 | 36.6 | 4.8 | 1.6 | 1.6 | 2.2 |
| W | 5.2 | 6.4 | 4.2 | 3.2 | 7 | 2.8 | 36.6 | 9.6 | 3.2 | 3.2 | 4.4 |
| L[um] | 2 | 1 | 1 | 2 | 1 | 2 | 1 | 2 | 2 | 2 | 2 |
| gm | 0.08 | 0.13 | 0.1 | 0.05 | 0.11 | 0.05 | 0.48 | 0.17 | 0.06 | 0.06 | 0.07 |
| gmp | 0.1 | 0.15 | 0.13 | 0.06 | 0.13 | 0.06 | 0.57 | 0.21 | 0.07 | 0.07 | 0.08 |
| ro | 384.62 | 384.62 | 384.62 | 555.56 | 555.56 | 555.56 | 161.29 | 161.29 | 500 | 500 | 500 |
| cgs | 10.57 | 22.83 | 14.98 | 11.41 | 14.23 | 9.99 | 74.41 | 34.24 | 11.41 | 11.41 | 15.69 |
| cgd | 2.63 | 3.26 | 2.14 | 1.63 | 3.54 | 1.43 | 18.48 | 4.89 | 1.63 | 1.63 | 2.24 |
| csb | 7.16 | 10.1 | 6.36 | 5.56 | 8.6 | 5.24 | 32.28 | 10.68 | 5.56 | 5.56 | 7.6 |

|  |  |  |  |
| --- | --- | --- | --- |
|  | CG | CS | CD |
| |Gain| | 30.72 [kV/A] | -1.70 [V/V] | 0.70 [V/V] |
| Rin | 10.9 kΩ | inf | Inf |
| Rout | 30.7 kΩ | 14.7 kΩ | 1.46 kΩ |
| Cin | 124 fF | 14 fF | 18 fF |
| Cout | 18 fF | 23 fF | 545 fF |

|  |  |  |  |
| --- | --- | --- | --- |
| Pole | R | C | Pole freq [MHz] |
| P1 | 10.9 kΩ | 124 fF | 117.3 |
| P2 | 30.7 kΩ | 32 fF | 162.3 |
| P3 | 14.7 kΩ | 42 fF | 261 |
| P4 | 1.47 kΩ | 545 fF | 200 |

Hspice simulated bandwidth



Appendix A. Hand Calculations

|  |  |
| --- | --- |
| **Common Gain** | |
|  |  |

|  |
| --- |
| Common Source |
| Common Drain |

|  |  |
| --- | --- |
| **Stage** | **Input variables** |
| CG | Vov1 |
| ID1 |
| RU||RD |
| CS | Vov2 |
| ID2 |
| A1 |
| CD | Vov3 |
| ID3 |

|  |  |
| --- | --- |
| **Power Consumption** | |
| VSUPPLY | VDD - VSS |
| Power I\_ref | I\_ref\*VSUPPLY |
| Power Resistor | 2\*(RU + RD)\*VSUPPLY |
| ID,Total | 2\*(ID1 + ID2 + ID2) |
| ratio\_1 | ID1 / ID3 |
| ratio\_2 | ID2 / ID,Total |
| ID1 | ID,Total [ (ratio\_1)\*(1 - ratio\_2) ] / [ 1 + ratio\_1 ] |
| ID2 | ID,Total ratio\_2 |
| ID3 | ID,Total [ (1 – ratio\_2) / (1 + ratio\_1) ] |
| RL,CG | RU||RD |
| RU | RL,CG ( 5 / (2.5+V1) ) |
| RD | RL,CG ( 5 / (2.5 -V1) ) |

|  |  |
| --- | --- |
| **Pole Locations** | |
| P1 |  |
| Vov1 |  |
| Vov1 |  |
| Id\_1 |  |
| Id\_2 |  |
| Id\_3 |  |
| A2 = (VovL2 / Vov2) |  |
| R = RU||RD |  |

|  |  |  |
| --- | --- | --- |
| **Equations** | | |
| 1/gmL2 | VovL2/(2Id) | (A2\*Vov2)/(2Id) |
| Vov1 |  |  |
| Vov1 |  |  |
| Id\_1 |  |  |
| Id\_2 |  |  |
| Id\_3 |  |  |
| A2 = (VovL2 / Vov2) |  |  |
| R = RU||RD |  |  |

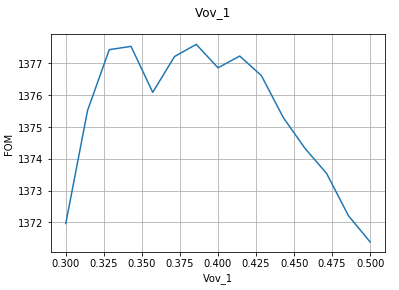
|  |  |
| --- | --- |
| **HSpice .op outputs** | |
| cgs | Cgs |
| cgd | Cgd |
| cgtot | Cgs + Cgd + Cgb |
| cdtot | Cgd + Cdb |
| cstot | Cgs + Csb |
| cbtot | Cgb + Csb +Cdb |
| **Other way** | |
| Cgs | cgs |
| Cgd | cgd |
| Cgb | cgtot – cgs – cgd |
| Csb | cstot – cgs |
| Cdb | cdtot – cgd |
| **Linear equivalences** | |
| Cdb / Cgs | 0.33 |
| Cgd / Cgs | 0.25 |
| gmb /gm | 0.2 |

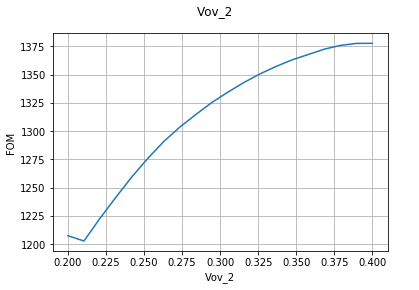
Common Drain:

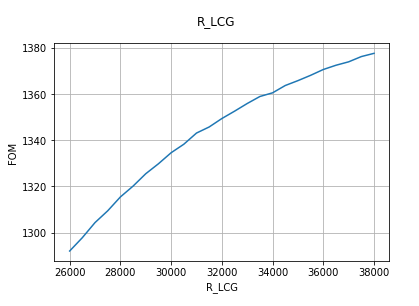
|  |
| --- |
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|  |

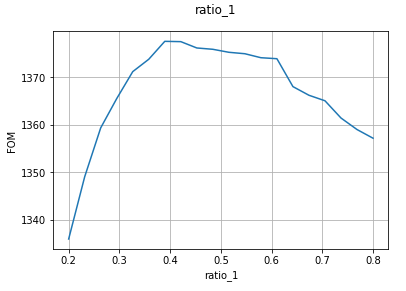
Design Flow:

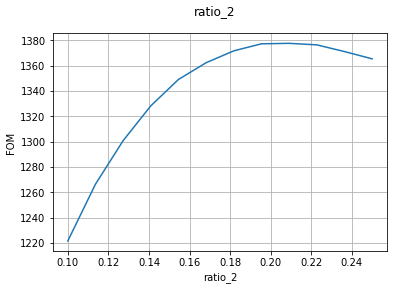
The trouble with this design is the biasing constraints imposed by the output common-mode voltage constraint. Because M3 and M2L are ref to -2.5v, their Vth are increased due to body effect.

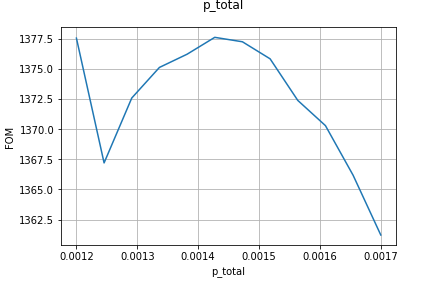












Appendix Caps

Example Hspice code for capacitance characterization of a single mosfet

Hspice netlist for capacitance lookup

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_nmos test netlist:

\* single device characteristics

.include /afs/ir.stanford.edu/class/ee114/hspice/ee114\_hspice.sp

\* MOSFETS

M1 2 1 0 0 nmos114 w=100u l=1u

Vg 1 0 0.9v

Vdd 2 0 5v

.op

.end

pmos test netlist:

\* single device characteristics

.include /afs/ir.stanford.edu/class/ee114/hspice/ee114\_hspice.sp

\* MOSFETS

M1 2 1 0 0 pmos114 w=2u l=1u

Vg 1 0 -0.9v

Vdd 2 0 -0.5v

.op

.end

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Nmos L=1u

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| W [um] | 2 | 5 | 10 | 20 | 50 | 100 |
| cdtot [fF] | 3.45 | 6.18 | 10.72 | 19.80 | 47.04 | 92.45 |
| cgtot [fF] | 5.17 | 12.92 | 25.85 | 51.70 | 129.24 | 258.48 |
| cstot [fF] | 8.67 | 17.17 | 31.33 | 59.67 | 144.67 | 286.33 |
| cbtot [fF] | 7.10 | 10.78 | 16.93 | 29.22 | 66.08 | 127.53 |
| cgs [fF] | 4.07 | 10.17 | 20.33 | 40.67 | 101.67 | 203.33 |
| cgd [fF] | 1.03 | 2.58 | 5.15 | 10.31 | 25.77 | 51.53 |
| cgb [fF] | 0.07 | 0.18 | 0.36 | 0.72 | 1.81 | 3.61 |
| csb [fF] | 4.60 | 7.00 | 11.00 | 19.00 | 43.00 | 83.00 |
| cdb [fF] | 2.42 | 3.60 | 5.57 | 9.49 | 21.28 | 40.92 |
| cgs\_calc | 3.07 | 7.67 | 15.33 | 30.67 | 76.67 | 153.33 |

|  |  |  |
| --- | --- | --- |
|  | x | y |
| cgs | 2.033 | 0 |
| cgd | 0.515 | 0 |
| cgb | 0.036 | 0 |
| csb | 0.8 | 3 |
| cdb | 0.393 | 1.637 |

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_Nmos L=2u

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| W [um] | 2 | 5 | 10 | 20 | 50 | 100 |
| cdtot [fF] | 3.48 | 6.25 | 10.87 | 20.11 | 47.81 | 93.98 |
| cgtot [fF] | 8.34 | 20.85 | 41.70 | 83.39 | 208.48 | 416.96 |
| cstot [fF] | 11.73 | 24.83 | 46.67 | 90.33 | 221.33 | 439.67 |
| cbtot [fF] | 7.17 | 10.96 | 17.29 | 29.94 | 67.89 | 131.14 |
| cgs [fF] | 7.13 | 17.83 | 35.67 | 71.33 | 178.33 | 356.67 |
| cgd [fF] | 1.06 | 2.65 | 5.31 | 10.61 | 26.53 | 53.07 |
| cgb [fF] | 0.14 | 0.36 | 0.72 | 1.44 | 3.61 | 7.22 |
| csb [fF] | 4.60 | 7.00 | 11.00 | 19.00 | 43.00 | 83.00 |
| cdb [fF] | 2.42 | 3.60 | 5.57 | 9.49 | 21.28 | 40.92 |
| cgs\_calc | 6.13 | 15.33 | 30.67 | 61.33 | 153.33 | 306.67 |

|  |  |  |
| --- | --- | --- |
|  | x | y |
| cgs | 3.567 | 0 |
| cgd | 0.531 | 0 |
| cgb | 0.072 | 0 |
| csb | 0.8 | 3 |
| cdb | 0.393 | 1.638 |

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|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| W [um] | 2 | 5 | 10 | 20 | 50 | 100 |
| cdtot [fF] | 4.90 | 9.50 | 17.17 | 32.52 | 78.55 | 155.27 |
| cgtot [fF] | 5.12 | 12.81 | 25.62 | 51.25 | 128.12 | 256.24 |
| cstot [fF] | 8.67 | 18.52 | 34.93 | 67.77 | 166.27 | 330.43 |
| cbtot [fF] | 8.55 | 15.48 | 27.03 | 50.13 | 119.45 | 234.97 |
| cgs [fF] | 4.07 | 10.17 | 20.33 | 40.67 | 101.67 | 203.33 |
| cgd [fF] | 1.00 | 2.51 | 5.02 | 10.03 | 25.08 | 50.15 |
| cgb [fF] | 0.05 | 0.14 | 0.28 | 0.55 | 1.38 | 2.75 |
| csb [fF] | 4.60 | 8.35 | 14.60 | 27.10 | 64.60 | 127.10 |
| cdb [fF] | 3.89 | 6.99 | 12.16 | 22.48 | 53.47 | 105.12 |
| cgs\_calc | 3.07 | 7.67 | 15.33 | 30.67 | 76.67 | 153.33 |

|  |  |  |
| --- | --- | --- |
|  | x | y |
| cgs | 2.033 | 0 |
| cgd | 0.502 | 0 |
| cgb | 0.028 | 0 |
| csb | 1.25 | 2.1 |
| cdb | 1.033 | 1.826 |

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_Pmos L=2u

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| W [um] | 2 | 5 | 10 | 20 | 50 | 100 |
| cdtot [fF] | 4.90 | 9.51 | 17.19 | 32.55 | 78.62 | 155.42 |
| cgtot [fF] | 8.25 | 20.62 | 41.25 | 82.50 | 206.24 | 412.48 |
| cstot [fF] | 11.73 | 26.18 | 50.27 | 98.43 | 242.93 | 483.77 |
| cbtot [fF] | 8.60 | 15.62 | 27.31 | 50.68 | 120.82 | 237.72 |
| cgs [fF] | 7.13 | 17.83 | 35.67 | 71.33 | 178.33 | 356.67 |
| cgd [fF] | 1.01 | 2.52 | 5.03 | 10.06 | 25.15 | 50.31 |
| cgb [fF] | 0.11 | 0.28 | 0.55 | 1.10 | 2.75 | 5.50 |
| csb [fF] | 4.60 | 8.35 | 14.60 | 27.10 | 64.60 | 127.10 |
| cdb [fF] | 3.89 | 6.99 | 12.16 | 22.48 | 53.47 | 105.12 |
| cgs\_calc | 6.13 | 15.33 | 30.67 | 61.33 | 153.33 | 306.67 |

|  |  |  |
| --- | --- | --- |
|  | x | y |
| cgs | 3.567 | 0 |
| cgd | 0.503 | 0 |
| cgb | 0.055 | 0 |
| csb | 1.25 | 2.1 |
| cdb | 1.033 | 1.826 |

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Limitations to the parasitic capacitance model:

|  |  |  |  |
| --- | --- | --- | --- |
| Vds | 5.0v | 1.0v | % difference |
| cgs | 66.33 | 66.33 | 0.00 |
| cgd | 5.61 | 5.12 | -9.58 |
| cgb | 1.10 | 1.10 | 0.00 |
| csb | 11.00 | 11.00 | 0.00 |
| cdb | 5.57 | 8.40 | 33.78 |

Cdb as well as Cgd are functions of Vds which is not taken into account in this model.

