

EDA Tool Tutorial

- Global Routing

Oct 17, 2024

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■ Theoretical Background

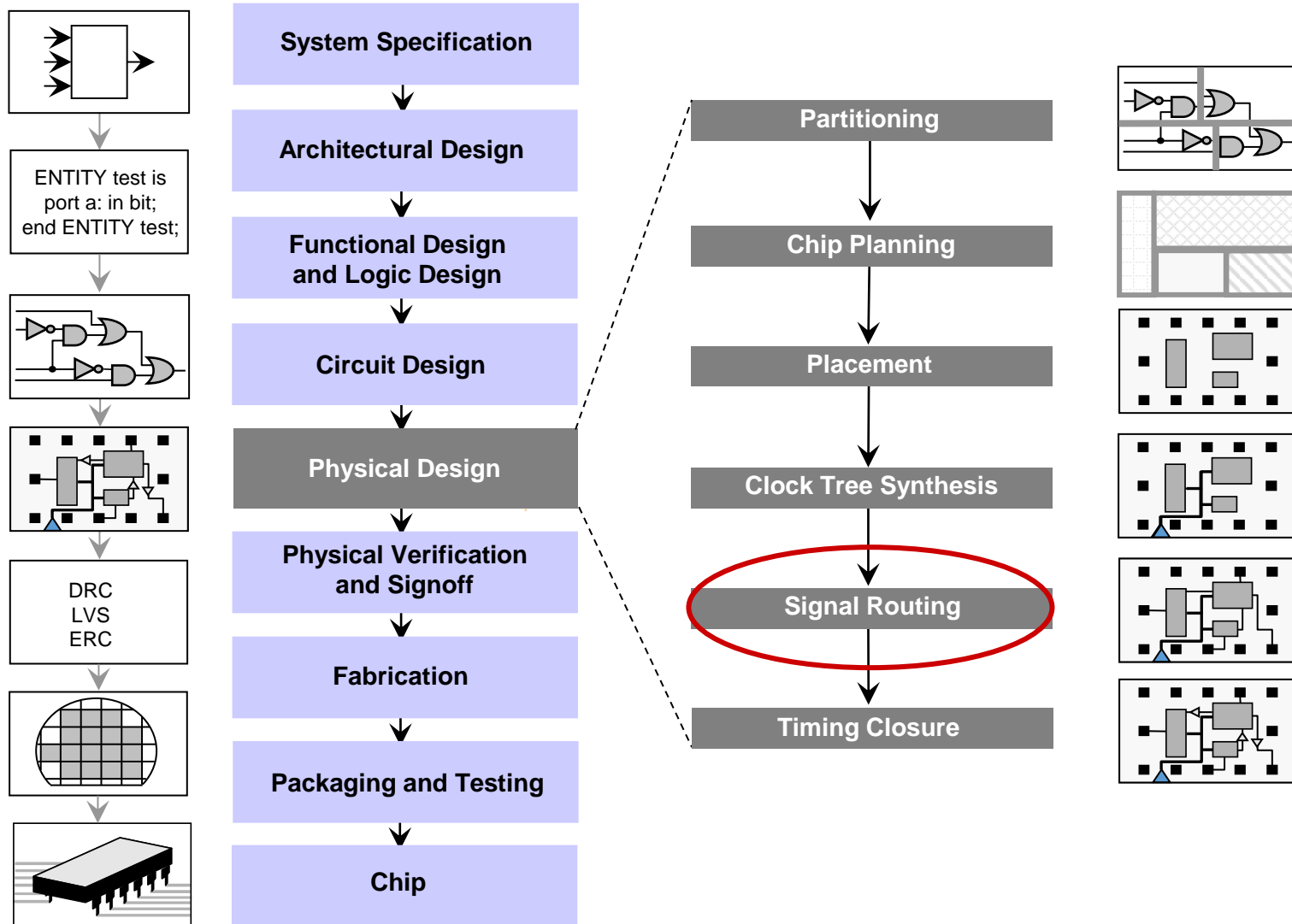
- Introduction to Routing
- Overview of Modern Global Router Flows

■ Lab

- Base P&R Flow
- Random Sensitivity Analysis
- Feature Extraction



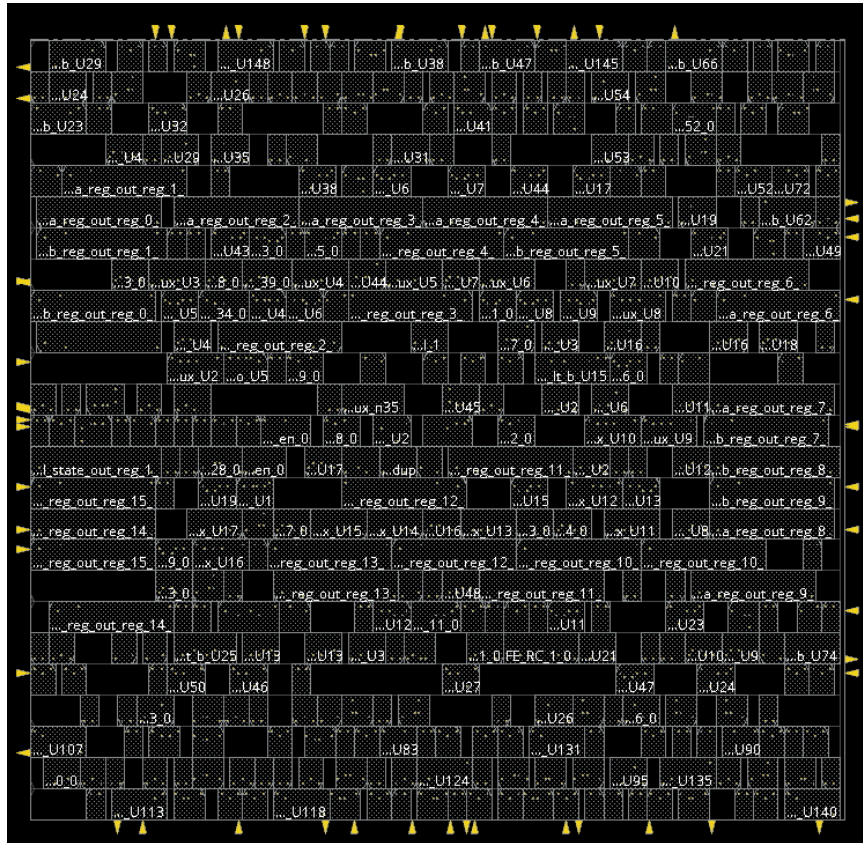
Introduction



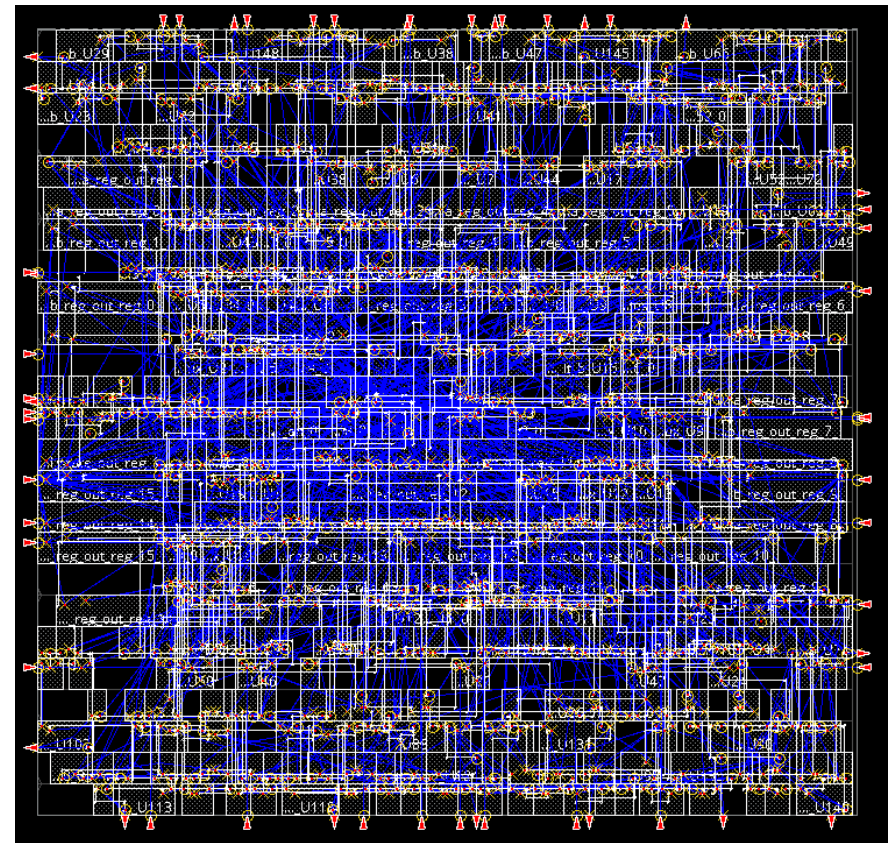
Introduction - Routing



Given a placement, a netlist and technology information,



Placement



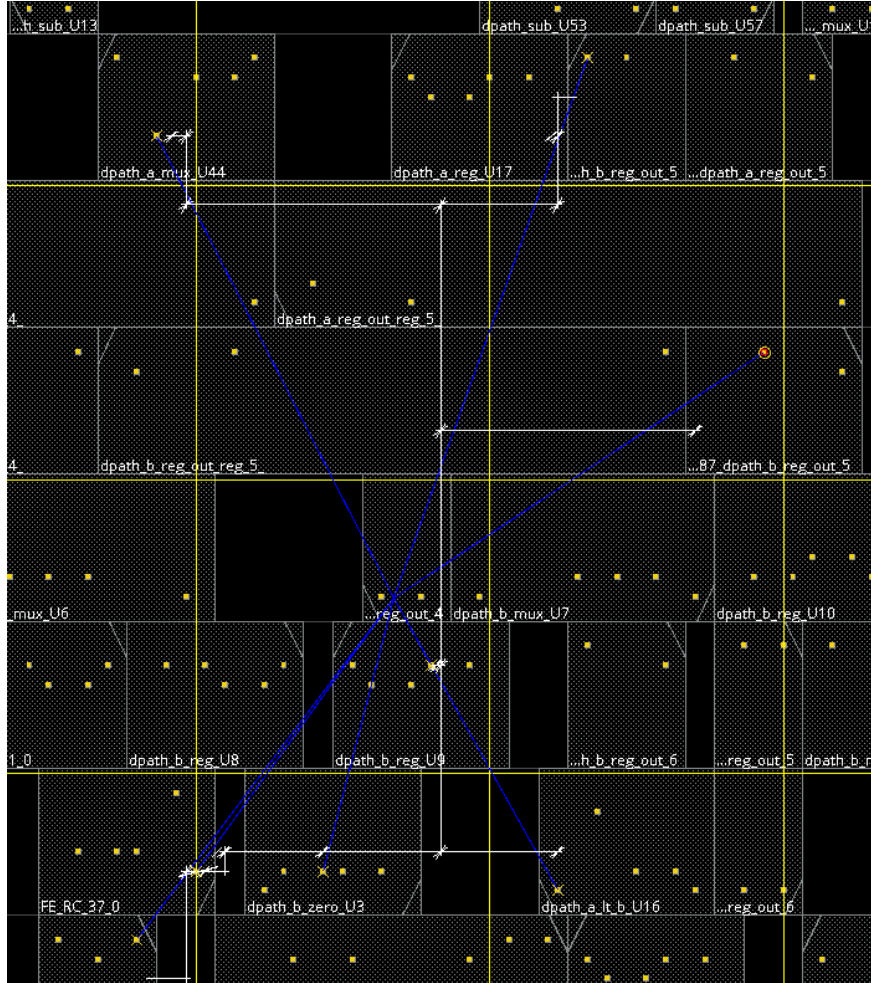
Nets



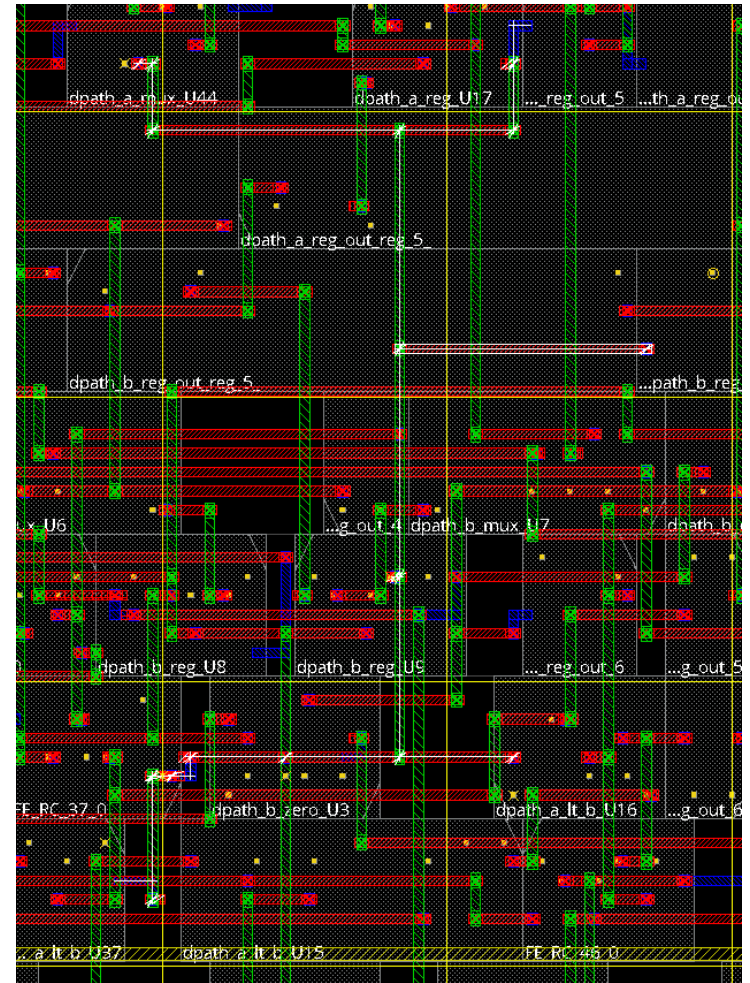
Global & Detailed Routing



Determine the necessary wiring, specific routing segments, to connect cells(pins)



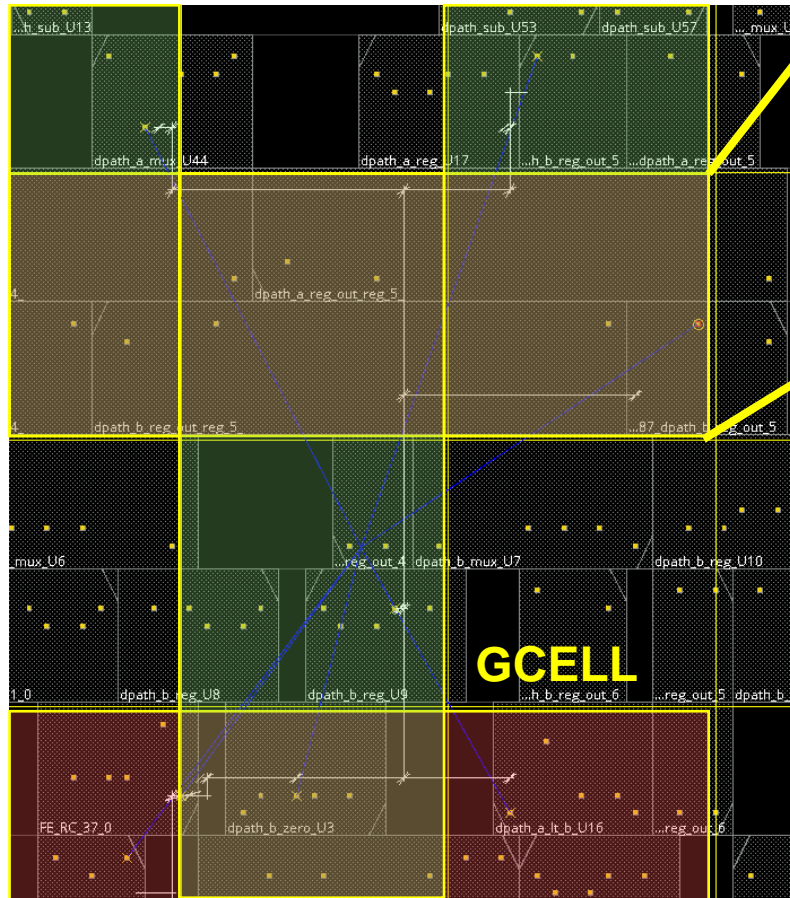
Pins on a net



Post-route

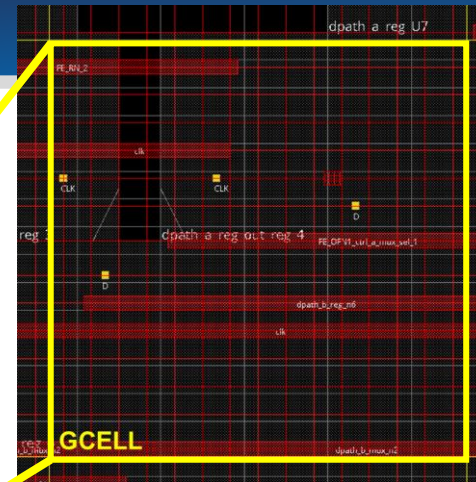


Global & Detailed Routing

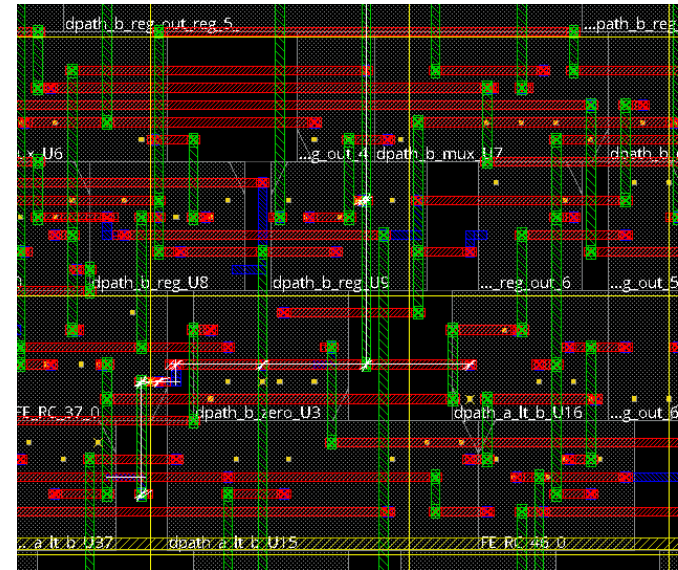


Global Routing

- Partitions the routing region into global routing cells (gcells)
- Plans routes as sequences of gcells
- Minimizes total length of routes and, possibly, routed congestion



— Track
(M2 Layer)



Detailed Routing

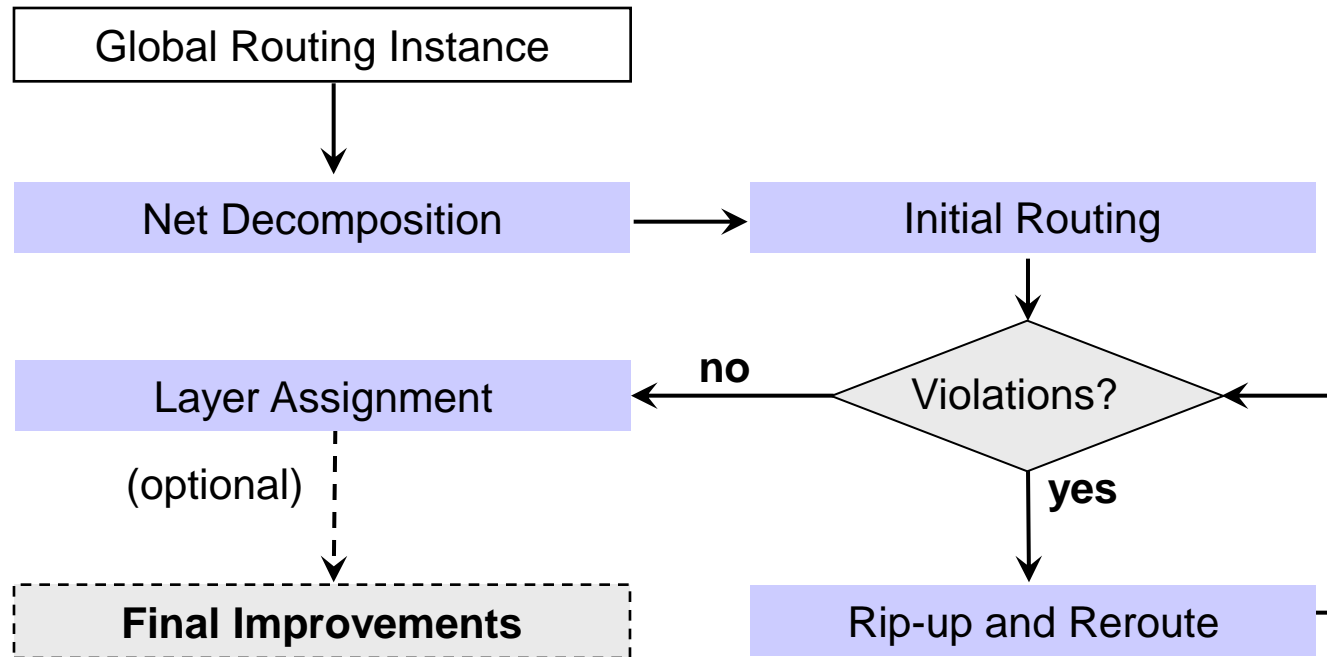
- Seeks to implement each global route as a sequence of track segments



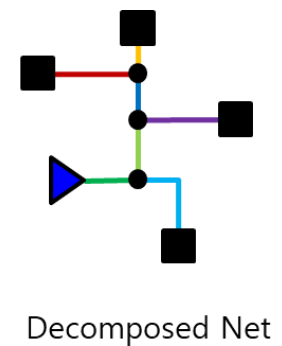
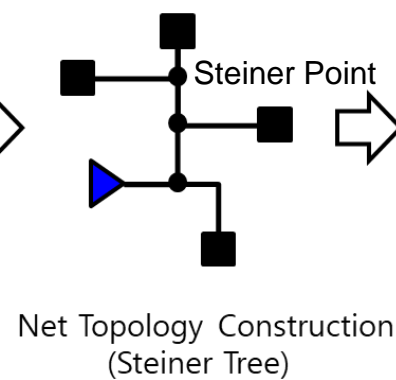
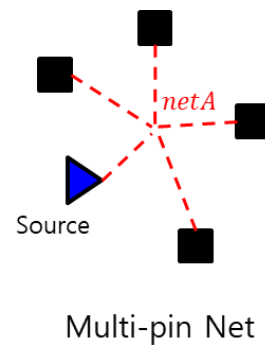
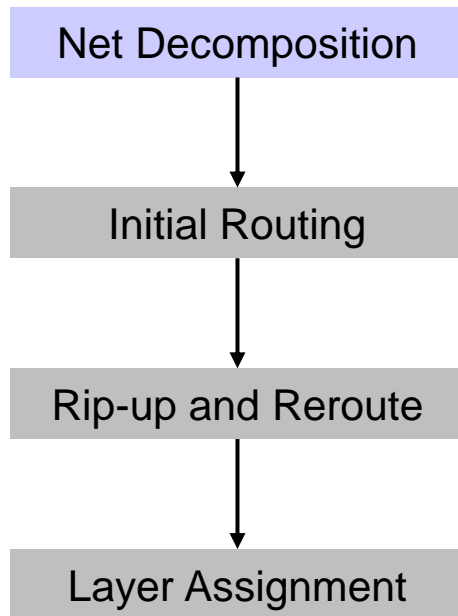
Flow for Modern Global Routers



- **General flow for modern global routers, where each router uses a unique set of optimizations:**



Net Decomposition



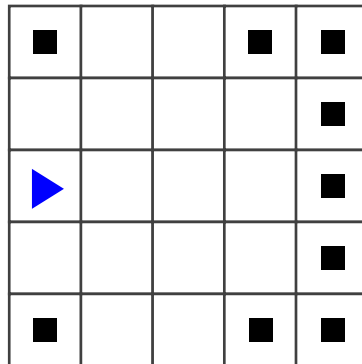
Net Topology Construction – Background



▶ Source ■ Sink ■ Critical sink

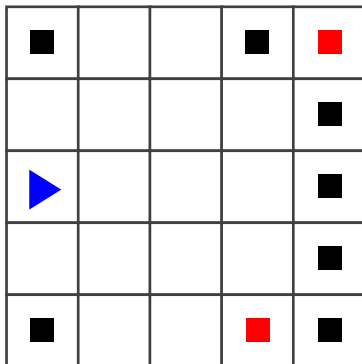
Pins on grid

Case 1



Net with non-critical pins

Case 2



Net with critical pins



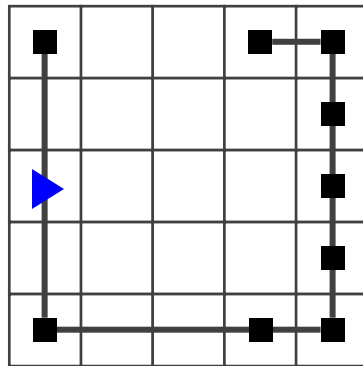
Net Topology Construction – Background



► Source ■ Sink ■ Critical sink

RSMT*

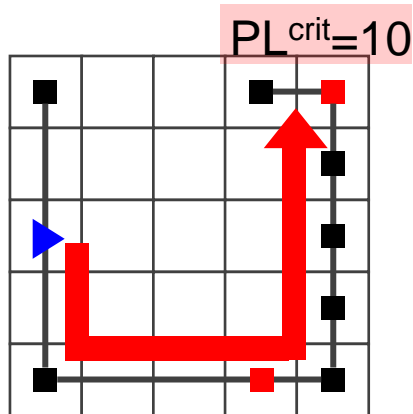
Case 1



Minimal WL

WL=13

Case 2



Long PL to critical pin
→ Timing violation

WL=13



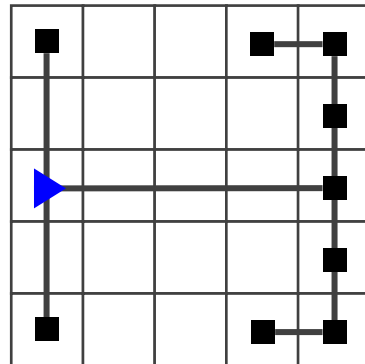
Net Topology Construction – Background



► Source ■ Sink ■ Critical sink

RSSLT**

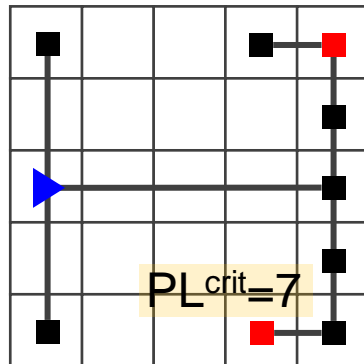
Case 1



WL=14

Longer WL
→ Increase power & routing congestion

Case 2



WL=14

Reasonable PL to all pins

PL_{crit}=7



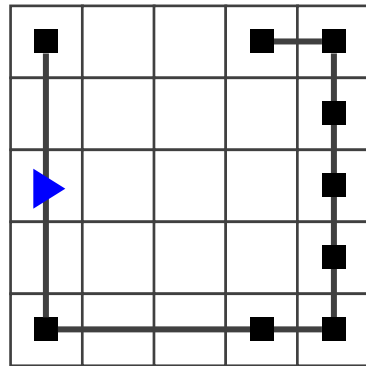
Net Topology Construction – Our Motivation



► Source ■ Sink ■ Critical sink

Proposed

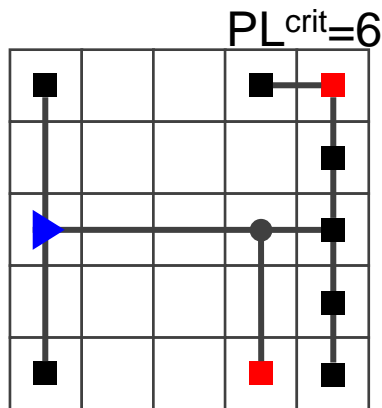
Case 1



WL=13

Minimal WL

Case 2



WL=15

Short PL to critical pins

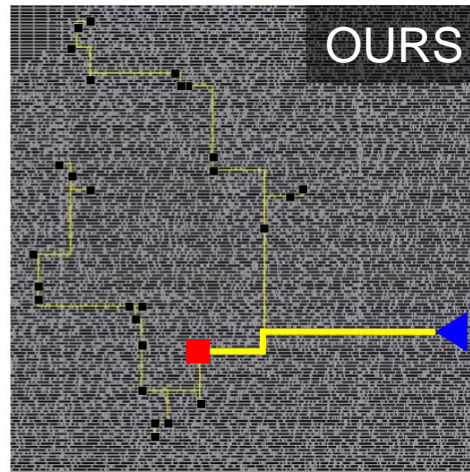
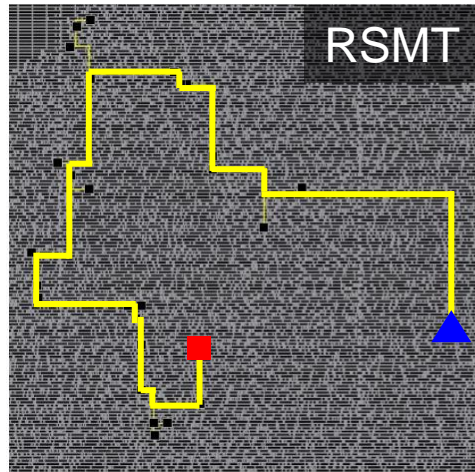
**Robust timing
w/ minimal WL increase**

Net Topology – Experimental Results



- Integrated our methodology into **OpenROAD(C++)**
- FLUTE(RSMT) vs PD-II(RSSLT) vs Ours

Example



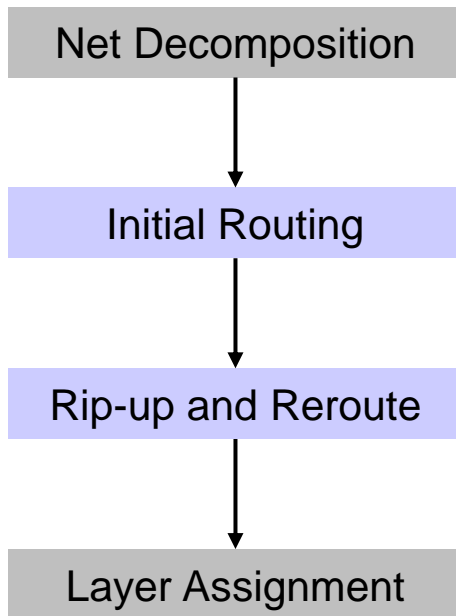
Delay to the **critical pin**:
 $64.6ps \rightarrow 21.7ps$

Comparison of results for the post-route final designs

WNS: -18.28% TNS: -53.37% Power: -0.06%

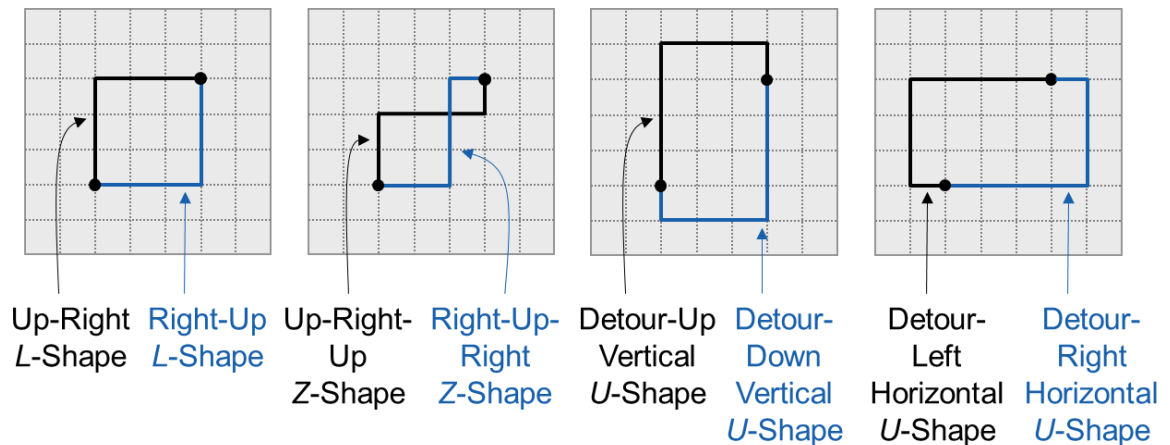
Reference: Jayoung Yang and Taewhan Kim, "Improving Timing Quality Through Net Topology Optimization in Global Routing"
IEEE International System-on-Chip Conference (SOCC) 2024

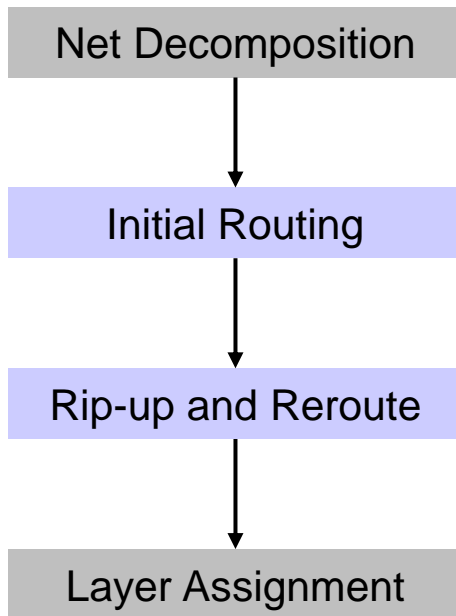




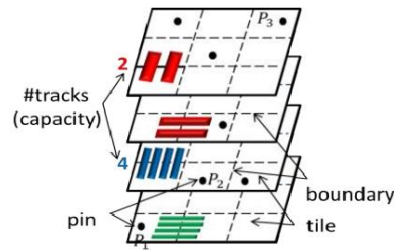
■ Pattern Routing

- ❑ Searches through a small number of route patterns to improve runtime
- ❑ Topologies commonly used in pattern routing: *L*-shapes, *Z*-shapes, *U*-shapes





■ Negotiated-Congestion Routing



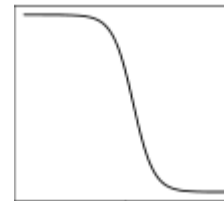
$capacity(e)$: Edge e 를 지나갈 수 있는 최대 track 수
(주로 $\frac{gcell_tile_size}{track_pitch}$ 로 계산)

$demand(e)$: Edge e 에서 routing에 사용된 track 수

The edge cost **$cost(e)$** is increased according to the *edge congestion*

Cost function of CUGR 2.0

$$1/(1 + e^{capacity(e) - demand(e)})$$



$capacity(e) - demand(e)$



- **Theoretical Background**

- Introduction to Routing
- Overview of Modern Global Router Flows

- **Lab**

- Base P&R Flow
- Random Sensitivity Analysis
- Feature Extraction



[LAB1] Download LAB Materials



```
alias ll='ls -alhrt --color' ; # Optional
cd ~
git clone https://github.com/jayoung-official/GLOBAL_ROUTE_LAB.git
cd GLOBAL_ROUTE_LAB
```

git clone 대신 copy도 가능

```
cp -rf ~/storage_ojXWdb/LAB_Download/241017_SNUCAD/GLOBAL_ROUTE_LAB ~
```

```
bash-4.4$ rm -rf GLOBAL_ROUTE_LAB
bash-4.4$ clear
bash-4.4$ alias ll='ls -alhrt --color' ; # Optional
bash-4.4$ cd ~
bash-4.4$ git clone https://github.com/jayoung-official/GLOBAL_ROUTE_LAB.git
Cloning into 'GLOBAL_ROUTE_LAB'...
remote: Enumerating objects: 155, done.
remote: Counting objects: 100% (108/108), done.
remote: Compressing objects: 100% (78/78), done.
remote: Total 155 (delta 40), reused 70 (delta 25), pack-reused 47 (from 1)
Receiving objects: 100% (155/155), 59.46 MiB | 20.50 MiB/s, done.
Resolving deltas: 100% (57/57), done.
bash-4.4$ cd GLOBAL_ROUTE_LAB
bash-4.4$ ll
total 1.2M
drwxr-xr-x 29 ukrprod_swtKa ukrprod_swtKa 4.0K Oct  9 16:48 ..
-rw-rw-rw-  1 ukrprod_swtKa ukrprod_swtKa 130 Oct  9 16:48 .gitignore
-rwxrwxrwx  1 ukrprod_swtKa ukrprod_swtKa 3.0K Oct  9 16:48 5_summarize.py
-rwxrwxrwx  1 ukrprod_swtKa ukrprod_swtKa 415 Oct  9 16:48 5_random_sensitivity_analysis.py
-rw-rw-rw-  1 ukrprod_swtKa ukrprod_swtKa 935 Oct  9 16:48 5_random_run.tcl
```



[LAB1] LAB Materials



Name	Size	Type
NETLIST_AES	4.0 KiB	folder
NETLIST_GCD	4.0 KiB	folder
PDK_ASAP7	4.0 KiB	folder
0_initdesign_aes.tcl	1.9 KiB	Tcl script
0_initdesign_gcd.tcl	1.9 KiB	Tcl script
1_floorplan.tcl	132 bytes	Tcl script
2_placement.tcl	190 bytes	Tcl script
3_ccopt.tcl	1.9 KiB	Tcl script
4_route.tcl	35 bytes	Tcl script
5_random_run.tcl	935 bytes	Tcl script
5_random_sensitivity_analysis.py	415 bytes	Python 3 script
5_summarize.py	2.9 KiB	Python 3 script
6_feature_extraction.tcl	2.2 KiB	Tcl script
LAB_GUIDE.pdf	1.1 MiB	PDF document
README.md	19 bytes	Markdown document

} Input netlists (after synthesis)

} Technology library

} Base P&R flow scripts

} LAB1

} LAB2

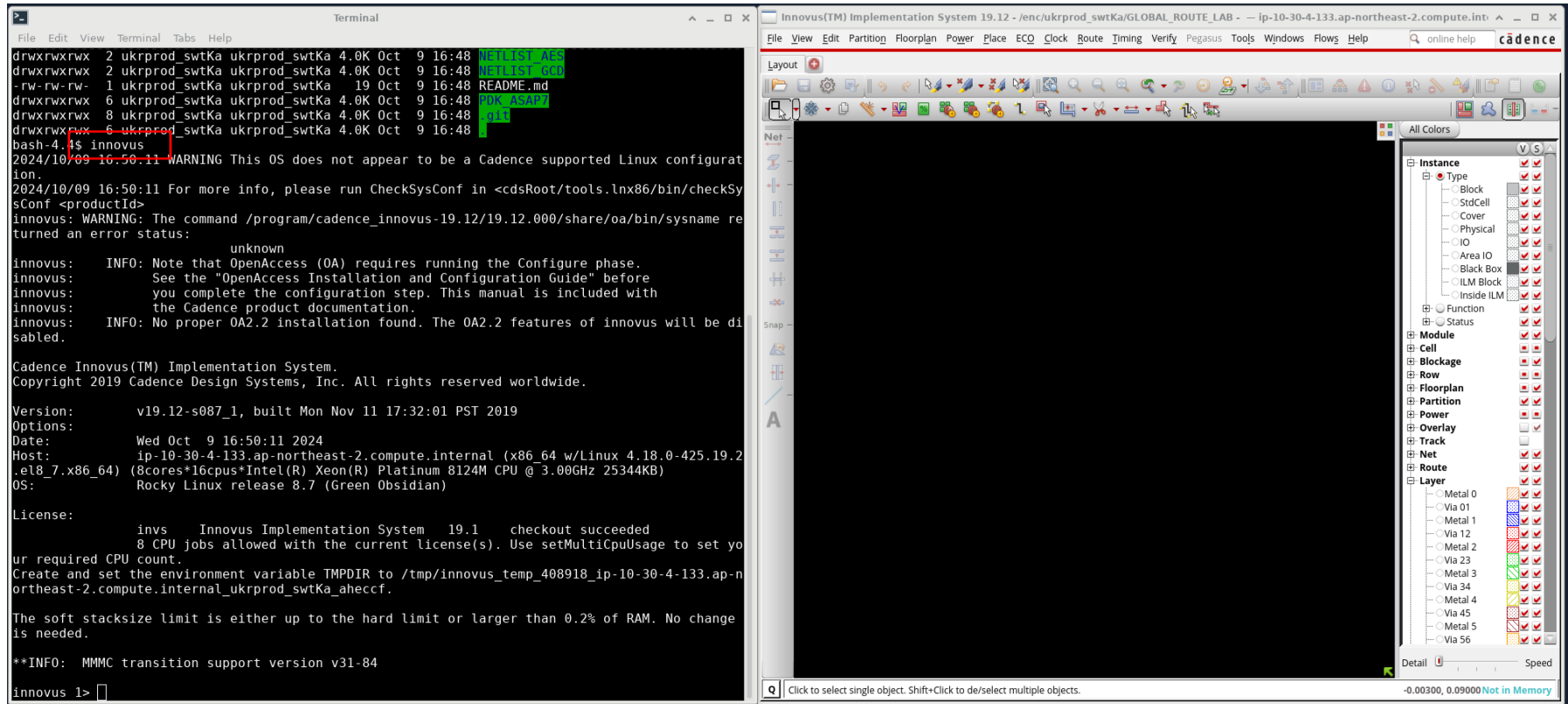
} This slide

Rescale 안에서 guide open 가능
evince ./LAB_GUIDE.pdf &



[LAB1] Run Innovus

innovus



Terminal Output:

```
drwxrwxrwx 2 ukrprod_swtKa ukrprod_swtKa 4.0K Oct 9 16:48 README.md
drwxrwxrwx 1 ukrprod_swtKa ukrprod_swtKa 19 Oct 9 16:48 README.md
drwxrwxrwx 6 ukrprod_swtKa ukrprod_swtKa 4.0K Oct 9 16:48 README.md
drwxrwxrwx 8 ukrprod_swtKa ukrprod_swtKa 4.0K Oct 9 16:48 README.md
drwxrwxrwx 6 ukrprod_swtKa ukrprod_swtKa 4.0K Oct 9 16:48 README.md
bash-4.1$ innovus
2024/10/09 16:50:11 WARNING This OS does not appear to be a Cadence supported Linux configuration.
2024/10/09 16:50:11 For more info, please run CheckSysConf in <cdsRoot/tools.lnx86/bin/checkSysConf <productId>
innovus: WARNING: The command /program/cadence_innovus-19.12/19.12.000/share/oa/bin/sysname returned an error status:
unknown
innovus: INFO: Note that OpenAccess (OA) requires running the Configure phase.
innovus: See the "OpenAccess Installation and Configuration Guide" before
innovus: you complete the configuration step. This manual is included with
innovus: the Cadence product documentation.
innovus: INFO: No proper OA2.2 installation found. The OA2.2 features of innovus will be disabled.

Cadence Innovus(TM) Implementation System.
Copyright 2019 Cadence Design Systems, Inc. All rights reserved worldwide.

Version: v19.12-s087_1, built Mon Nov 11 17:32:01 PST 2019
Options:
Date: Wed Oct 9 16:50:11 2024
Host: ip-10-30-4-133.ap-northeast-2.compute.internal (x86_64 w/Linux 4.18.0-425.19.2.el8_7.x86_64) (8cores*16cpus*Intel(R) Xeon(R) Platinum 8124M CPU @ 3.00GHz 25344KB)
OS: Rocky Linux release 8.7 (Green Obsidian)

License:
invs Innovus Implementation System 19.1 checkout succeeded
8 CPU jobs allowed with the current license(s). Use setMultiCpuUsage to set your required CPU count.
Create and set the environment variable TMPDIR to /tmp/innovus_temp_408918_ip-10-30-4-133.ap-northeast-2.compute.internal_ukrprod_swtKa_ahccf.

The soft stacksize limit is either up to the hard limit or larger than 0.2% of RAM. No change is needed.

**INFO: MMMC transition support version v31-84

innovus 1>
```

Cadence Innovus GUI:

- Instance panel (checked items):
 - Type
 - Block
 - StdCell
 - Cover
 - Physical
 - IO
 - Area IO
 - Black Box
 - ILM Block
 - Inside ILM
 - Function
 - Status
- Module
 - Cell
- Blockage
- Row
- Floorplan
- Partition
- Power
- Overlay
- Track
- Net
- Route
- Layer
 - Metal 0
 - Via 01
 - Metal 1
 - Via 12
 - Metal 2
 - Via 23
 - Metal 3
 - Via 34
 - Metal 4
 - Via 45
 - Metal 5
 - Via 56

Detail: 0.00300, 0.09000 Not in Memory

[LAB1] Run Init Design

```
source 0_initdesign_gcd.tcl
```

The image shows a terminal window on the left and the Cadence Innovus implementation system interface on the right.

Terminal Window:

```
bash-4.4$ innovus
2024/10/09 16:52:19 WARNING This OS does not appear to be a Cadence supported Linux configuration.
2024/10/09 16:52:19 For more info, please run CheckSysConf in <cdsRoot/tools.lnx86/bin/checkSysConf <productId>
innovus: WARNING: The command /program/cadence_innovus-19.12/19.12.000/share/oa/bin/sysname returned an error status:
unknown
innovus: INFO: Note that OpenAccess (OA) requires running the Configure phase.
innovus: See the "OpenAccess Installation and Configuration Guide" before
innovus: you complete the configuration step. This manual is included with
innovus: the Cadence product documentation.
innovus: INFO: No proper OA2.2 installation found. The OA2.2 features of innovus will be disabled.

Cadence Innovus(TM) Implementation System.
Copyright 2019 Cadence Design Systems, Inc. All rights reserved worldwide.

Version:      v19.12-s087_1, built Mon Nov 11 17:32:01 PST 2019
Options:
Date:         Wed Oct 9 16:52:19 2024
Host:         ip-10-30-4-133.ap-northeast-2.compute.internal (x86_64 w/Linux 4.18.0-425.19.2.el8_7.x86_64) (8cores*16cpus*Intel(R) Xeon(R) Platinum 8124M CPU @ 3.00GHz 25344KB)
OS:           Rocky Linux release 8.7 (Green Obsidian)

License:
  invs   Innovus Implementation System   19.1   checkout succeeded
         8 CPU jobs allowed with the current license(s). Use setMultiCpuUsage to set your required CPU count.
         Create and set the environment variable TMPDIR to /tmp/innovus_temp_409328_ip-10-30-4-133.ap-northeast-2.compute.internal_ukrprod_swtkKa_oyLUX1.

The soft stacksize limit is either up to the hard limit or larger than 0.2% of RAM. No change is needed.

**INFO: MMMC transition support version v31-84

innovus 1> source 0_initdesign_gcd.tcl
Searching LEF files...
Searching LIB files...

Loading LEF file PDK_ASAP7/techlef/asap7_tech_4x_201209.lef ...
```

Cadence Innovus Implementation System:

The interface shows the "Layout" tab selected. The main workspace is empty. The right-hand pane displays the "Instance" tree, which includes a list of components and their status. The status column shows red checkmarks for most items, indicating they are loaded or configured successfully.

Instance	Type	Status
Block	Block	✓
StdCell	StdCell	✓
Cover	Cover	✓
Physical	Physical	✓
IO	IO	✓
Area IO	Area IO	✓
Black Box	Black Box	✓
Function	Function	✓
Status	Status	✓
Module	Module	✓
Cell	Cell	✓
Blockage	Blockage	✓
Row	Row	✓
Floorplan	Floorplan	✓
Partition	Partition	✓
Power	Power	✓
Overlay	Overlay	✓
Track	Track	✓
Net	Net	✓
Route	Route	✓
Layer	Layer	✓
Active(0)	Active(0)	✓
V0(0)	V0(0)	✓
M1(1)	M1(1)	✓
V1(1)	V1(1)	✓
M2(2)	M2(2)	✓
V2(2)	V2(2)	✓
M3(3)	M3(3)	✓
V3(3)	V3(3)	✓
M4(4)	M4(4)	✓
V4(4)	V4(4)	✓
M5(5)	M5(5)	✓
V5(5)	V5(5)	✓
M6(6)	M6(6)	✓
V6(6)	V6(6)	✓

[LAB1] Run Floorplan

```
source 1_floorplan.tcl
```

The screenshot displays the Cadence Innovus implementation system interface. On the left, a terminal window shows the execution of the `source 1_floorplan.tcl` script. The script performs various setup tasks, including setting process parameters, applying capacitance filtering thresholds, and saving design data. The terminal output includes the following text:

```
INNVDCx5p33 ASAP7_75t_R CKINVDCx6p67 ASAP7_75t_R CKINVDCx9p33 ASAP7_75t_R INVx11 ASAP7_75t_R INVx13 ASAP7_75t_R INVx1 ASAP7_75t_R INVx2 ASAP7_75t_R INVx3 ASAP7_75t_R INVx4 ASAP7_75t_R INVx5 ASAP7_75t_R INVx6 ASAP7_75t_R INVx8 ASAP7_75t_R INVxp67 ASAP7_75t_R INVxp33 ASAP7_75t_R
Total number of usable inverters: 21
List of unusable inverters:
Total number of unusable inverters: 0
List of identified usable delay cells: HB3xp67_ASAP7_75t_R HB4xp67_ASAP7_75t_R
Total number of identified usable delay cells: 2
List of identified unusable delay cells:
Total number of identified unusable delay cells: 0
## Process: 7 (User Set)
## Node: (not set)

## Check design process and node:
## Design tech node is not set.

Applying the recommended capacitance filtering threshold values for 7nm process node: total_c_th=0, relative_c_th=1 and coupling_c_th=0.1.
These values will be used by all post-route extraction engines, including TQuantus, IQquantus and Quantus QRC extraction.
Capacitance filtering mode(-capFilterMode option of the setExtractRCMode) is 'relAndCouple' for all engines.
The accuracy mode for postRoute effortLevel low extraction will be set to 'high'.
Default value for EffortLevel(-effortLevel option of the setExtractRCMode) in postRoute extraction mode is 'medium'.
Process node set using 'setDesignMode' is less than or equal to 32nm, for which captable file(s) would be ignored as preRoute extraction would instead use technology file. For postRoute extraction, default value for effort level would be 'medium' and effort level 'low' would not be allowed.
innovus 2>
innovus 2>
innovus 2>
innovus 2> source 1_floorplan.tcl
Adjusting core size to PlacementGrid : width :28.224 height : 27.072
% Begin save design ... (date=10/09 16:54:55, mem=942.9M)
% Begin Save ccopt configuration ... (date=10/09 16:54:55, mem=944.8M)
% End Save ccopt configuration ... (date=10/09 16:54:55, total cpu=0:00:00.0, real=0:00:00.0, peak res=946.1M, current mem=946.1M)
% Begin Save netlist data ... (date=10/09 16:54:55, mem=946.1M)
Writing Binary DB to 1_floorplan.enc.dat/gcd.v.bin in single-threaded mode...
% End Save netlist data ... (date=10/09 16:54:55, total cpu=0:00:00.0, real=0:00:00.0, peak res=949.0M, current mem=947.0M)
2024/10/09 16:54:55 WARNING This OS does not appear to be a Cadence supported Linux configuration.
```

On the right, the main layout area shows a floorplan with a grid of cells. The right-hand pane displays the 'Instance' and 'Module' lists, which include various components like 'Block', 'StdCell', 'Cover', 'Physical', 'IO', 'Area IO', 'Black Box', 'Function', and 'Status'. The bottom status bar indicates the current state: '0.15925, 24.48700 Sel: 0 in Memory'.

Layout area floorplan

[LAB1] Run Floorplan

gedit 1_floorplan.tcl

Terminal Output:

```
% Begin Save floorplan data ... (date=10/09 16:54:55, mem=952.0M)
Saving floorplan file ...
2024/10/09 16:54:55 WARNING This OS does not appear to be a Cadence supported Linux configuration.
2024/10/09 16:54:55 For more info, please run CheckSysConf in <cdsRoot/>
sConf <productId>
% End Save floorplan data ... (date=10/09 16:54:55, total cpu=0:00:00.0,
res=952.2M, current mem=952.2M)
Saving Drc markers ...
... No Drc file written since there is no markers found.
% Begin Save placement data ... (date=10/09 16:54:55, mem=952.2M)
** Saving stdCellPlacement_binary (version# 2) ...
Save Adaptive View Pruning View Names to Binary file
% End Save placement data ... (date=10/09 16:54:55, total cpu=0:00:00.0,
res=953.1M, current mem=953.1M)
% Begin Save routing data ... (date=10/09 16:54:55, mem=953.1M)
Saving route file ...
2024/10/09 16:54:55 WARNING This OS does not appear to be a Cadence supported Linux configuration.
2024/10/09 16:54:55 For more info, please run CheckSysConf in <cdsRoot/>
sConf <productId>
*** Completed saveRoute (cpu=0:00:00.0 real=0:00:00.0 mem=956.5M) ***
% End Save routing data ... (date=10/09 16:54:55, total cpu=0:00:00.0,
s=958.4M, current mem=957.5M)
Saving property file 1_floorplan.enc.dat/gcd.prop
*** Completed saveProperty (cpu=0:00:00.0 real=0:00:00.0 mem=959.5M) ***
Saving preRoute extracted patterns in file '1_floorplan.enc.dat/gcd.tcl'
Saving preRoute extraction data in directory '1_floorplan.enc.dat/extra'
% Begin Save power constraints data ... (date=10/09 16:54:55, mem=959.2M)
% End Save power constraints data ... (date=10/09 16:54:55, total cpu=0:00:00.0,
peak res=959.2M, current mem=959.2M)
Generated self-contained design 1_floorplan.enc.dat
#% End save design ... (date=10/09 16:54:56, total cpu=0:00:01.2, real=0:00:01.8M, current mem=962.6M)
*** Message Summary: 0 warning(s), 0 error(s)

0
innovus 3>
innovus 3>
innovus 3> gedit
innovus 4> gedit 1_fl
1_floorplan.enc 1_floorplan.enc.dat/ 1_floorplan.tcl
innovus 4> gedit 1_floorplan.tcl
```

Key commands:

- # ★ Key commands
- # 현재 Design 저장
- saveDesign 이름.enc
- # 불러오기
- source 이름.enc

Cadence Interface Details:

- File: View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify Pegasus Tools Windows Flows Help
- Layout
- 1_floorplan.tcl
- Save
- Instance: Type, Block, StdCell, Cover, Physical, IO, Area IO, Black Box, Function, Status
- Module: Cell, Blockage, Row, Floorplan, Partition, Power, Overlay, Track, Net, Route, Layer
- Layer: Active(0), V0(0), M1(1), V1(1), M2(2), V2(2), M3(3), V3(3), M4(4), V4(4), M5(5), V5(5), M6(6), V6(6)
- Detail Speed
- 0.63000, 13.97775 Sel: 0 In Memory

[LAB1] Run Placement

```
source 2_placement.tcl
```

The image displays two side-by-side windows from a Cadence implementation system. The left window is a terminal showing the execution of a Tcl script. The right window is the 'Implementation System' interface, showing a detailed layout of a circuit with various components and their connections.

Terminal Window Output:

```
File Edit View Terminal Tabs Help
% Begin Save placement data ... (date=10/09 17:13:36, mem=953.1M)
** Saving stdCellPlacement binary (version# 2) ...
Save Adaptive View Pruning View Names to Binary file
% End Save placement data ... (date=10/09 17:13:36, total cpu=0:00:00.0, real=0:00:00.0, peak res=954.0M, current mem=954.0M)
% Begin Save routing data ... (date=10/09 17:13:36, mem=954.0M)
Saving route file ...
2024/10/09 17:13:36 WARNING This OS does not appear to be a Cadence supported Linux configuration.
2024/10/09 17:13:36 For more info, please run CheckSysConf in <cdsRoot/tools.lnx86/bin/checkSysConf <productId>
*** Completed saveRoute (cpu=0:00:00.0 real=0:00:00.0 mem=954.4M) ***
% End Save routing data ... (date=10/09 17:13:36, total cpu=0:00:00.0, real=0:00:00.0, peak res=959.3M, current mem=958.4M)
Saving property file 1_floorplan.enc.dat.tmp/gcd.prop
*** Completed saveProperty (cpu=0:00:00.0 real=0:00:00.0 mem=957.4M) ***
Saving preRoute extracted patterns in file '1_floorplan.enc.dat.tmp/gcd.techData.gz' ...
Saving preRoute extraction data in directory '1_floorplan.enc.dat.tmp/extraction/' ...
% Begin Save power constraints data ... (date=10/09 17:13:36, mem=960.2M)
% End Save power constraints data ... (date=10/09 17:13:36, total cpu=0:00:00.0, real=0:00:00.0, peak res=960.2M, current mem=960.2M)
Generated self-contained design 1_floorplan.enc.dat.tmp
% End save design ... (date=10/09 17:13:37, total cpu=0:00:01.1, real=0:00:02.0, peak res=963.7M, current mem=963.3M)
*** Message Summary: 0 warning(s), 0 error(s)

0
innovus 3> gedit 1_floorplan.enc
innovus 4> source 2_placement.tcl
No user sequential activity specified, applying default sequential activity of "0.2" for Dynamic Power reporting.
'set default_switching_activity' finished successfully.
*** Starting GigaPlace ***
**INFO: user set placement options
**INFO: user set opt options

#optDebug: fT-E <X 2 3 1 0>
-place_design_floorplan_mode false # bool, default=false
*** Start deleteBufferTree ***
Info: Detect buffers to remove automatically.
Analyzing netlist ...
Updating netlist
AAE DB initialization (MEM=1034.13 CPU=0:00:00.2 REAL=0:00:01.0)
```

Implementation System Window:

The right window shows the 'Implementation System' interface. The main area displays a detailed layout of a circuit, with various components and their connections. The components are labeled with names like 'b.U24', 'b.U23', 'reg_out_reg_0', 'reg_out_reg_1', etc. The layout is color-coded, with red lines indicating connections and green lines indicating power or ground connections. The right sidebar shows a list of components and their properties, including 'Type', 'Block', 'Cover', 'Physical', 'IO', 'Area IO', 'Black Box', 'Function', 'Status', 'Module', 'Cell', 'Blockage', 'Row', 'Floorplan', 'Partition', 'Overlay', 'Track', 'Net', 'Route', and 'Layer'. The bottom status bar shows the current state: '1.91775, 21.87000 Sel: 0 Timing Analyzed'.

Place instances(cells)

placement w/ trial route

[LAB1] Run CTS

```
source 3_ccopt.tcl
```

The image shows two side-by-side windows. The left window is a terminal running the 'source 3_ccopt.tcl' command. The right window is the Cadence Innovus Implementation System showing a routing layout.

Terminal Output:

```
innovus> source 3_ccopt.tcl
Deleting AAE DB due to SOCV option changes -----
**ERROR: (IMPTCM-163): Option "-immediate" for command create_ccopt_clock_tree_spec is obsolete and will be ignored. It no longer has any effect and should be removed from your script.
Creating clock tree spec for modes (timing configs): default_constraint
extract_clock_generator_skew_groups=true: create_ccopt_clock_tree_spec will generate skew groups with a name prefix of "_clock_gen" to balance clock generator connected flops with the clock generator they drive.
Reset timing graph...
Ignoring AAE DB Resetting ...
Reset timing graph done.
Ignoring AAE DB Resetting ...
Analyzing clock structure...
Analyzing clock structure done.
Reset timing graph...
Ignoring AAE DB Resetting ...
Reset timing graph done
```

Innovus Implementation System:

The right window displays the routing layout with various components and connections. The status bar at the bottom indicates: **-1.91775, 21.87000 Sel: 0 Timing Analyzed**.

CTS + Optimization

[LAB1] Run Route

```
source 4_route.tcl
```

The image displays two side-by-side windows from a computer screen. The left window is a terminal window titled 'Terminal' showing the output of a Tcl script. The right window is the Cadence Innovus Implementation System, showing a detailed routing layout.

Terminal Window Output:

```
File Edit View Terminal Tabs Help
Save Adaptive view Pruning view Names to binary file
% End Save placement data ... (date=10/09 17:20:45, total cpu=0:00:00.0, real=0:00:00.0, peak res=1374.7M, current mem=1374.7M)
% Begin Save routing data ... (date=10/09 17:20:45, mem=1374.7M)
Saving route file ...
2024/10/09 17:20:45 WARNING This OS does not appear to be a Cadence supported Linux configuration.
2024/10/09 17:20:45 For more info, please run CheckSysConf in <cdsRoot/tools.lnx86/bin/checkSysConf <productId>
*** Completed saveRoute (cpu=0:00:00.0 real=0:00:00.0 mem=1394.8M) ***
% End Save routing data ... (date=10/09 17:20:45, total cpu=0:00:00.0, real=0:00:00.0, peak res=1374.8M, current mem=1374.8M)
Saving property file 3_ccopt.enc.dat/gcd.prop
*** Completed saveProperty (cpu=0:00:00.0 real=0:00:00.0 mem=1397.8M) ***
#Saving pin access data to file 3_ccopt.enc.dat/gcd.apa ...
#
Saving rc congestion map 3_ccopt.enc.dat/gcd.congmap.gz ...
2024/10/09 17:20:45 WARNING This OS does not appear to be a Cadence supported Linux configuration.
2024/10/09 17:20:45 For more info, please run CheckSysConf in <cdsRoot/tools.lnx86/bin/checkSysConf <productId>
Saving preRoute extracted patterns in file '3_ccopt.enc.dat/gcd.techData.gz' ...
Saving preRoute extraction data in directory '3_ccopt.enc.dat/extraction/' ...
% Begin Save power constraints data ... (date=10/09 17:20:45, mem=1374.8M)
% End Save power constraints data ... (date=10/09 17:20:45, total cpu=0:00:00.0, real=0:00:00.0, peak res=1374.8M, current mem=1374.8M)
Generated self-contained design 3_ccopt.enc.dat
#% End save design ... (date=10/09 17:20:46, total cpu=0:00:01.2, real=0:00:02.0, peak res=1374.8M, current mem=1374.3M)
*** Message Summary: 0 warning(s), 0 error(s)

0
innovus 6>
innovus 6> genit 4_route.tcl
innovus 7> source 4_route.tcl
#% Begin routeDesign (date=10/09 17:22:25, mem=1374.4M)
#routeDesign: cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1374.37 (MB), peak = 1471.61 (MB)
##**INFO: setDesignMode -flowEffort standard
##**INFO: multi-cut via swapping will be performed after routing.
##**INFO: All auto set options tuned by routeDesign will be restored to their original settings on command completion.
Begin checking placement ... (start mem=1400.1M, init mem=1400.1M)
*info: Placed = 397
```

Cadence Innovus Implementation System Window:

The window shows a detailed routing layout of a circuit board. The top menu bar includes File, View, Edit, Partition, Floorplan, Power, Place, ECO, Clock, Route, Timing, Verify, Pegasus, Tools, Windows, Flows, and Help. The main area displays a complex routing diagram with various components and connections. The right sidebar shows a list of instances and modules, including Block, StdCell, Cover, Physical, IO, Area IO, Black Box, Function, and Status. The bottom status bar indicates the current location and speed: 4.85300, 17.50850 Set: 0 Routed.

Global + Detail Route

[LAB1] Report



기본 Flow 결과 Report 저장

```
report_analysis_summary > base.timing  
report_power > base.power
```

```
innovus 9> report_analysis_summary > base.timing  
#####  
# Design Stage: PostRoute  
# Design Name: gcd  
# Design Mode: 7nm  
# Analysis Mode: MMMC OCV  
# Parasitics Mode: No SPEF/RCDB  
# Signoff Settings: SI Off  
#####  
Extraction called for design 'gcd' of instances=397 and nets=435 using extraction engine 'preRoute'.  
PreRoute RC Extraction called for design gcd.  
RC Extraction called in multi-corner(1) mode.  
RCMode: PreRoute  
RC Corner Indexes      0  
Capacitance Scaling Factor : 1.00000  
Resistance Scaling Factor  : 1.00000  
Clock Cap. Scaling Factor   : 1.00000  
Clock Res. Scaling Factor   : 1.00000  
Shrink Factor              : 1.00000  
PreRoute extraction is honoring NDR/Shielding/ExtraSpace for clock nets.  
Using Quantus QRC technology file ...  
Updating RC grid for preRoute extraction ...  
Initializing multi-corner resistance tables ...  
PreRoute RC Extraction DONE (CPU Time: 0:00:00.0 Real Time: 0:00:00.0 MEM: 1476.445M)  
Calculate early delays in OCV mode...  
Calculate late delays in OCV mode...  
Start delay calculation (fullDC) (1 T). (MEM=1501.93)  
Total number of fetched objects 433  
AAE INFO: Total number of nets for which stage creation was skipped for all views 0  
End delay calculation. (MEM=1576.38 CPU=0:00:00.0 REAL=0:00:00.0)  
End delay calculation (fullDC). (MEM=1576.38 CPU=0:00:00.3 REAL=0:00:00.0)  
innovus 10> report_power > base.power  
1
```

Report 확인

```
gedit base.timing  
gedit base.power
```



[LAB1] Objective - Random Sensitivity Analysis

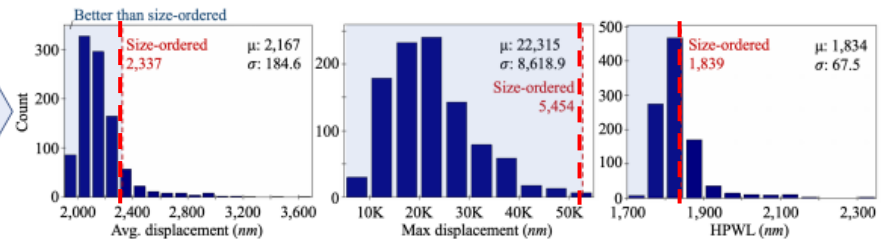
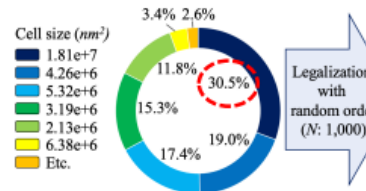
Random exploration can be used to identify **potential improvements over default flow**

• Ex) Random-ordered Cell Placement → Placement metric change

S. -Y. Lee, et al., "RL-Legalizer: Reinforcement Learning-based Cell Priority Optimization in Mixed-Height Standard Cell Legalization," 2023 DATE

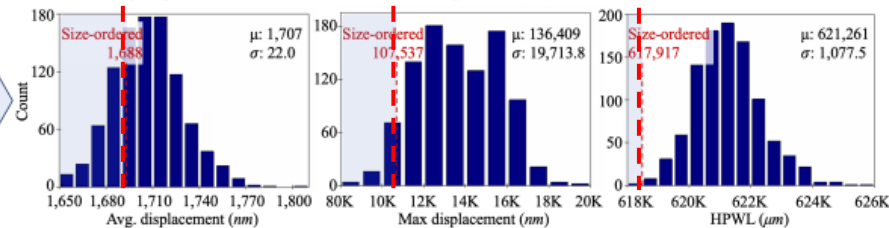
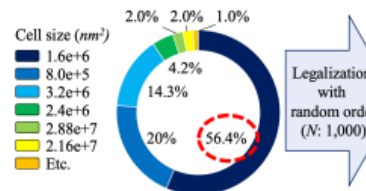
(a) *usb_phy*

OpenCores design implemented with 75% util. and 1.0 aspect ratio in 45-nm NanGate technology.



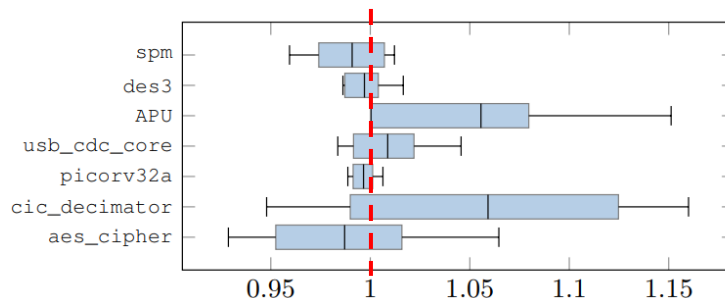
(b) *pci_bridge32_b_md3*

ICCAD-2017 CAD contest benchmark.



• Ex) Random Steiner Point Disturbance → Timing metric change

S. Liu, Z. et al., "Concurrent Sign-off Timing Optimization via Deep Steiner Points Refinement," 2023 DAC



Distribution of sign-off TNS ratio of the updated solution with random Steiner point disturbance to the original one

[LAB1] Adjustable parameters in Routing (Innovus)

```
setAttribute -net <net_name> -avoid_detour {true|false} -weight <integer> ...
```

Attaches attributes to nets and subnets. Attaching the attributes allows the NanoRoute routing commands [to route the nets following specific requirements](#).

Parameters

`-avoid_detour {true | false}`

[Avoids detours](#) of roughly more than a few gcell grids on the specified nets. This attribute affects global routing only. (Default: false)

Note: Cadence recommends that you use caution with this attribute, as it adds congestion to the design.

`-weight <integer>`

Specifies a relative weight for routing nets. In each switch box, the NanoRoute router [routes nets with the highest weight first](#), then the next highest weight, and so on. Specify a value higher than 2 to ensure a net is routed before other nets. (Default: **2**)



[LAB1] Run Random Sensitivity Analysis



Random Sensitivity Analysis 실행 전 innovus 종료하여 shell로 이동

```
exit
```

Check run script(python)

```
gedit 5_random_sensitivity_analysis.py
```

```
#!/usr/bin/env python3
import subprocess

N_RUNS = 5

def run_script():
    try:
        result = subprocess.run('innovus -files 5_random_run.tcl', shell=True)
        if result.stderr:
            print("Error:")
            print(result.stderr)
    except Exception as e:
        print(f"An error occurred: {e}")

for _ in range(N_RUNS):
    run_script()
```

5_random_run.tcl 스크립트를
5회 반복 수행



[LAB1] Run Random Sensitivity Analysis



Check 5_random_run.tcl

gedit 5_random_run.tcl

```
5_random_run.tcl
~/GLOBAL_ROUTE_LAB

source 3_ccopt.enc

set timestamp [clock format [clock seconds] -format "%y%m%d_%H%M%S"]
puts $timestamp

set avoid_detour_prob [expr {(int(rand() * 5) + 1) * 0.1}] ;# 0.1에서 0.5 사이

set dataList {}

foreach_in_collection net [get_nets] {
    set weight [expr {int(rand() * 4) + 2}] ; # 2에서 5 사이의 값
    set avoid_detour [expr {rand() < ${avoid_detour_prob} ? "true" : "false"}]
    set net_name [get_property $net name]
    setAttribute -net $net_name -weight $weight -avoid_detour $avoid_detour

    lappend dataList [list $net_name $weight $avoid_detour]
}

routeDesign

# REPORTS
set fileId [open "random_${timestamp}_${avoid_detour_prob}.nets.csv" "w"]
puts $fileId "Net,Weight,Avoid_Detour"
foreach row $dataList {
    puts $fileId [join $row ","]
}
close $fileId

report_analysis_summary > "random_${timestamp}_${avoid_detour_prob}.timing"
report_power > "random_${timestamp}_${avoid_detour_prob}.power"

exit
```

3_ccopt.enc Design을 불러온 후
net별 weight, avoid_detour 랜덤 할당

결과 비교를 위한 Report 후 Exit



[LAB1] Run Random Sensitivity Analysis



Run script 실행 / 약 5분 소요(N_RUNS=5 기준)

```
./5_random_sensitivity_analysis.py
```

결과 조회 (*.timing, *.power 파싱)

```
./5_summarize.py
```

기본 Flow

Random x10

Name	WNS	TNS	POWER
base	-8.415	-22.376	0.33842197
random_241009_174125_0.1	-8.415	-22.376	0.33842197
random_241009_174203_0.2	-8.415	-22.376	0.33842197
random_241009_174240_0.3	-8.415	-22.376	0.33842197
random_241009_174318_0.1	-8.415	-22.376	0.33842197
random_241009_174355_0.5	-8.535	-22.835	0.33845897
random_241009_174433_0.1	-8.535	-22.835	0.33845897
random_241009_174511_0.5	-8.535	-22.835	0.33845897
random_241009_174549_0.4	-8.415	-22.376	0.33842197
random_241009_174627_0.1	-8.535	-22.835	0.33845897
random_241009_174704_0.2	-8.415	-22.376	0.33842197

Toy design net 수가 적어(약 400개) 큰 효과 없음



[LAB1] Results for AES_CIPHER_TOP



#Nets of Design: 약 10000개

Name	WNS	TNS	POWER
base	-9.208	-339.913	4.62745333
random_241009_055859_0.5	-9.684	-374.335	4.62808571
random_241009_060453_0.5	-9.812	-333.828	4.62767426
random_241009_061049_0.4	-10.168	-373.995	4.62823325
random_241009_061644_0.4	-10.022	-365.142	4.62761984
random_241009_062236_0.4	-9.605	-347.652	4.62797298
random_241009_062832_0.2	-11.032	-363.802	4.62793837
random_241009_063425_0.3	-10.568	-359.964	4.62790291
random_241009_064018_0.4	-9.236	-363.022	4.62795988
random_241009_064607_0.3	-11.273	-368.496	4.62805885
random_241009_065204_0.4	-11.753	-370.290	4.62816721
random_241009_093218_0.5	-9.793	-349.804	4.62796977
random_241009_093814_0.1	-12.990	-428.342	4.62795213
random_241009_094407_0.3	-11.646	-372.209	4.62724831
random_241009_094958_0.1	-9.773	-356.929	4.62731261
random_241009_095549_0.3	-9.290	-369.146	4.62773923
random_241009_100143_0.5	-10.732	-374.225	4.62784993
random_241009_100733_0.5	-11.444	-414.964	4.62819967
random_241009_101322_0.3	-8.441	-337.672	4.62749583
random_241009_101909_0.4	-9.937	-335.503	4.62738434
random_241009_102501_0.5	-11.339	-367.085	4.62801802

개선 가능성 확인

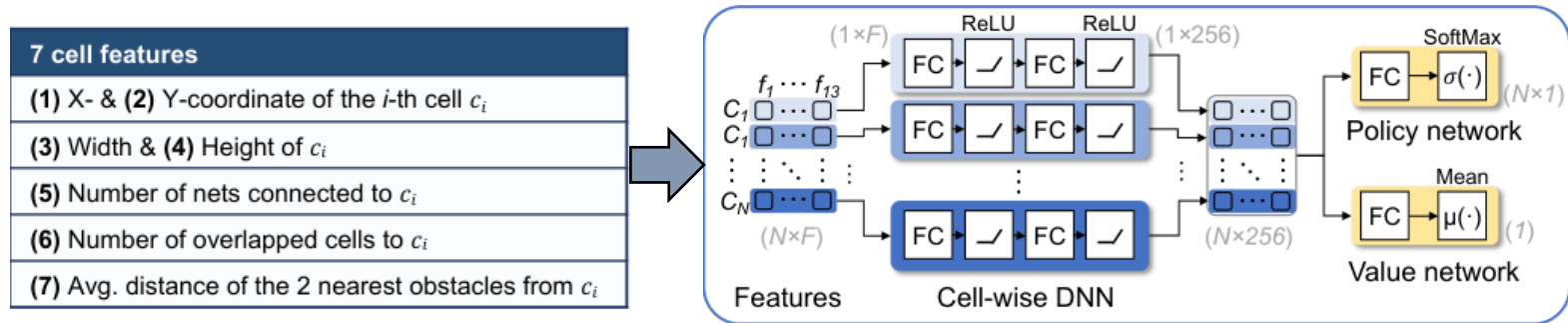
[LAB2] Feature Extraction



Extensive feature extraction is crucial for optimization / machine learning.

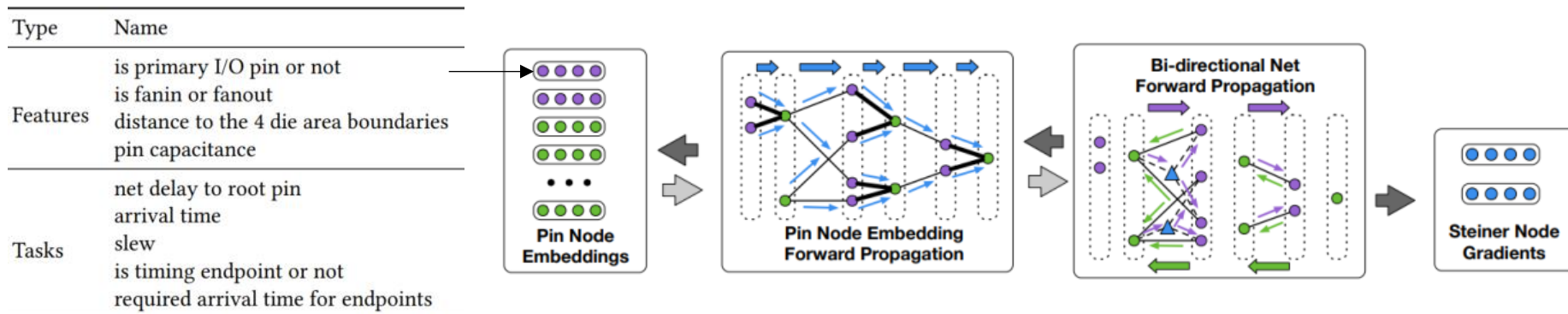
• Ex) RL-based placement priority optimization

S. -Y. Lee, et al., "RL-Legalizer: Reinforcement Learning-based Cell Priority Optimization in Mixed-Height Standard Cell Legalization," 2023 DATE



• Ex) Timing Optimization via Deep Steiner Points Refinement

S. Liu, Z. et al., "Concurrent Sign-off Timing Optimization via Deep Steiner Points Refinement," 2023 DAC



[LAB2] Feature Extraction

gedit 6_feature_extraction.tcl

```
Open 6_feature_extraction.tcl ~GLOBAL_ROUTE_LAB Save
foreach_in_collection net [get_nets] {
    set net_name [get_property $net name]
    set pins [get_pins -of_objects $net]
    set n_pins [sizeof_collection $pins]

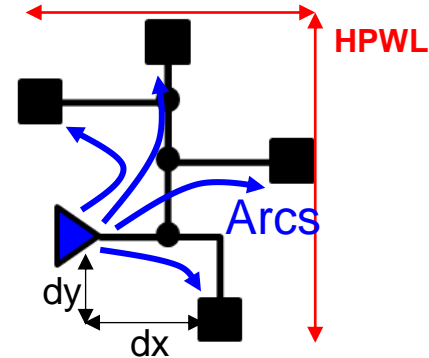
    puts "Net: $net_name"
    puts " Pins: $n_pins"

    set x_coordinates [get_property $pins x_coordinate]
    set y_coordinates [get_property $pins y_coordinate]
    set min_x [lindex [lsort -real $x_coordinates] 0]
    set max_x [lindex [lsort -real $x_coordinates] end]
    set min_y [lindex [lsort -real $y_coordinates] 0]
    set max_y [lindex [lsort -real $y_coordinates] end]
    set hpwl [expr {($max_x - $min_x) + ($max_y - $min_y)}]
    puts " HPWL: $hpwl"

    set arcs [get_arcs -of_objects $net]
    foreach_in_collection arc $arcs {
        set source_pin [get_property $arc source_pin]
        set sink_pin [get_property $arc sink_pin]
        set source_pin_name [get_property $source_pin full_name]
        set sink_pin_name [get_property $sink_pin full_name]
        puts " Arc: $source_pin_name -> $sink_pin_name"
        set is_clock [get_property $sink_pin is_clock]
        puts " is_clock: $is_clock"
        set delay_max_fall [get_property $arc delay_max_fall]
        set delay_max_rise [get_property $arc delay_max_rise]
        if { $delay_max_fall > $delay_max_rise } {
            puts " delay: $delay_max_fall"
        } else {
            puts " delay: $delay_max_rise"
        }

        set slack_max_fall [get_property $sink_pin slack_max_fall]
        set slack_max_rise [get_property $sink_pin slack_max_rise]
        if { $slack_max_fall < $slack_max_rise } {
            puts " slack: $slack_max_fall"
        } else {
            puts " slack: $slack_max_rise"
        }

        set source_coordinate_x [get_property $source_pin x_coordinate]
        set source_coordinate_y [get_property $source_pin y_coordinate]
        set sink_coordinate_x [get_property $sink_pin x_coordinate]
        set sink_coordinate_y [get_property $sink_pin y_coordinate]
        set diff_x [expr {abs($source_coordinate_x - $sink_coordinate_x)}]
        set diff_y [expr {abs($source_coordinate_y - $sink_coordinate_y)}]
        puts " diff_x: $diff_x"
        puts " diff_y: $diff_y"
    }
}
```



```
Open features.txt ~GLOBAL_ROUTE_LAB Save
diff y: 1.8
Net: dpath_a_lt_b_n18
Pins: 5
HPWL: 13.896
Arc: FE_0FC11_dpath_a_reg_out_0/Y -> dpath_sub_U23/A
is_clock: false
delay: 0.200
slack: 112.021
diff_x: 0.936
diff_y: 2.16
Arc: FE_0FC11_dpath_a_reg_out_0/Y -> dpath_sub_U24/A
is_clock: false
delay: 0.200
slack: -2.115
diff_x: 0.936
diff_y: 2.52
Arc: FE_0FC11_dpath_a_reg_out_0/Y -> dpath_b_mux_U2/B2
is_clock: false
delay: 0.300
slack: 141.066
diff_x: 4.752
diff_y: 6.624
Arc: FE_0FC11_dpath_a_reg_out_0/Y -> FE_RC_33_0/B2
is_clock: false
delay: 0.200
slack: 164.921
diff_x: 2.664
diff_y: 3.816
Net: dpath_a_lt_b_n19
Pins: 4
HPWL: 5.4
Arc: FE_0FC35_dpath_a_reg_out_1/Y -> dpath_a_lt_b_U43/B2
is_clock: false
```

[LAB2] Feature Extraction



innovus

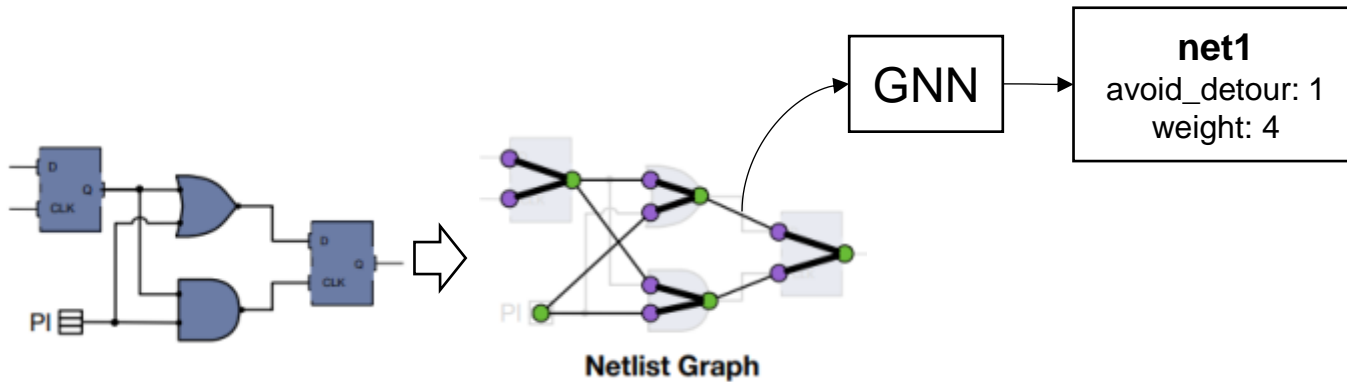
```
source 4_route.enc
source 6_feature_extraction.tcl > features.txt
gedit features.txt
```

```
diff_y: 1.8
Net: dpath_a_lt_b_n18
Pins: 5
HPWL: 13.896
Arc: FE_OFC11_dpath_a_reg_out_0/Y -> dpath_sub_U23/A
  is_clock: false
  delay: 0.200
  slack: 112.021
  diff_x: 0.936
  diff_y: 2.16
Arc: FE_OFC11_dpath_a_reg_out_0/Y -> dpath_sub_U24/A
  is_clock: false
  delay: 0.200
  slack: -2.115
  diff_x: 0.936
  diff_y: 2.52
Arc: FE_OFC11_dpath_a_reg_out_0/Y -> dpath_b_mux_U2/B2
  is_clock: false
  delay: 0.300
  slack: 141.066
  diff_x: 4.752
  diff_y: 6.624
Arc: FE_OFC11_dpath_a_reg_out_0/Y -> FE_RC_33_0/B2
  is_clock: false
  delay: 0.200
  slack: 164.921
  diff_x: 2.664
  diff_y: 3.816
Net: dpath_a_lt_b_n19
Pins: 4
HPWL: 5.4
Arc: FE_OFC35_dpath_a_reg_out_1/Y -> dpath_a_lt_b_U43/B2
  is_clock: false
```



생각해볼 거리

- Additional features
- Rule-based algorithms
- ML-model designs





Thank you

