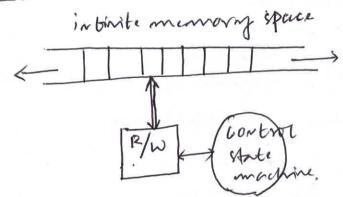
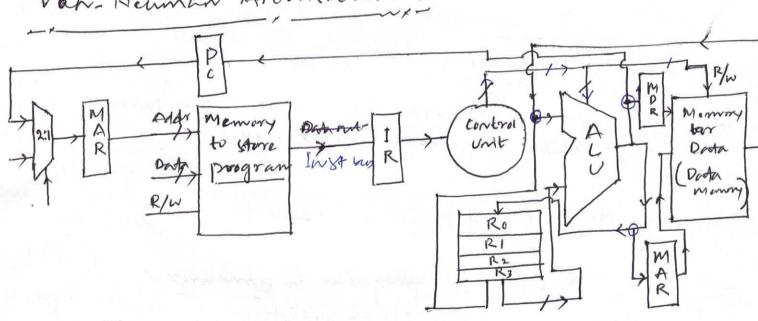
| - Lecture -12 - (11/10/2019) (16/10/2019) | C |
|---|-----|
| compreter organisation and | |
| Architecture. | |
| Summary: | |
| - Digital components | |
| - ALU - Memory - Registers | |
| - Instruction sel- Architecture | |
| - formal- | |
| - Encoling Addroningmode. | |
| - Machine & Amensbly language programing | |
| Campbuter organisation: | |
| - Computer organisation: | |
| Bustion: - How to organise all the signal components such that a program candbe executed ? | |
| | |
| The ponkriple: - stored program approach | |
| The odea :- O Store the program on amomony | uau |
| The sidea: - O Store the program on amounty Sunambigo (Set of well letino) Sunambigo instruction (one by one) | |
| instruction (the organis) | 2 |
| 3) Decide uni instruction to identity control signals | |
| and operand. | |
| a Fetch wir operand | Ls |
| 1) Execute the instruction using control signer and operand | |
| D Store back the result | |
| O store back the resulte (thoughy the current- state of the machine) | |

Vor. Neumann Architecture | Tuning Machine -

Tunny Machine:



Van- Neuman Architecture :-



→ The exact data 2 control path with nutricient Heaving legge & Interconnect will be drawn enter on.

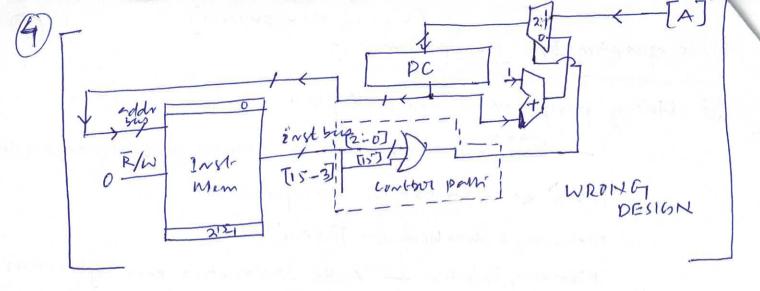
The Microoperations: -

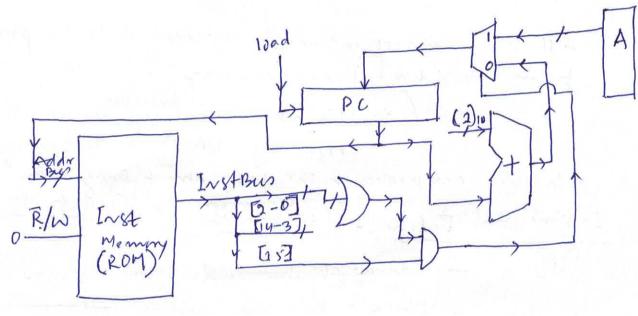
- Whe mino steps required to execute an instruction time of the bive major steps.

Micro operation for over processor: 1 Storney pragram at the bern place - This is a work of resumme manager Coperating Insta MAR & Address of in stored program Memory address bus & [MAR] Memory Data his & sale In Araction en a byte orund All these microoperations be repeated to low a prigram from Hard dom to mannemerny

(in the modern computer this is being Some by DMA- Birect memory 2) In the HACK processor the program is Burgleded Access)

[2) In Aruction Fetch: Tot simulatory through the means - Adam of that INSTruction required - place to keep the sontruction brice totales - Any post procening. - Regumement: Addres of the instruction to be betoned. place to keep the between instruction. post processing (reporting pc content) [Address 520] Content of [PC] REPORT R/W < 0 [Instruction bus] + Memory [Add bus] it in struction [2/10] +0 pc < [A] PC < PC+1





Instruction Derode: -(1D)

Decoling is essential to understand the control signals and operands.

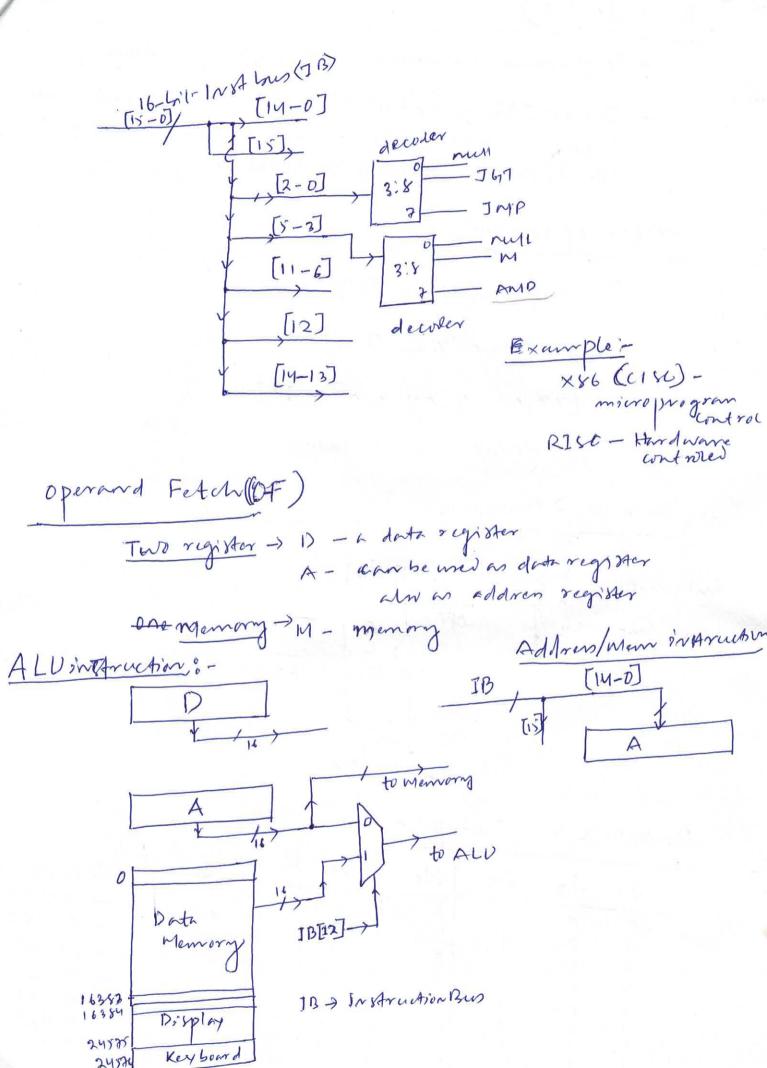
Micro operations:
Contro logic

[Invariations]

Control signals

Control logic

Partial control path Herign:-





- To perborm assumetic and work operation
- The recenany watron signals are appropriately we connected to steer the operand to ALU and execute the in Aruction according to op-tode.

micro operation: -

Data Palli Design:

| Deuta po | auti bor | Jun | mp: | - | | | 1-1 | 10. | 111 | JA |) | |
|----------|----------|-----|-----|-----|-----|-------------|------|-----|-------|----|---|---------|
| | 1 | 10 | 110 | JAI | 112 | Jd3 | Jan. | 305 | -0716 | 0 | _ | rull |
| 11 | 12 | 7.3 | - | 0 | U | 0 | 0 | 0 | 0 | 0 | _ | out 70 |
| 0 | 0 | U | 0 | 1 | 0 | -, <i>U</i> | U | 0 | 0 | 0 | - | oul-=0 |
| U | 0 | 1 | 0 | 0 | 1 | D | U | n | o | 0 | | out-7/0 |
| 0 | 1 | 1 | 0 | U | O | 1 | 0 | n | 0 | v | | out-20 |
| 0 | , | D | 0 | U | U | 0 | | | a | 7 | _ | nd- 70 |

0 1 0

it out=0 else 27=0 22=1 it nd- <0 else ng=0 mg = 1 -> 2r=1 -> mg=1 ml- <0 => m- +0 8 m- 40 2720 & ng 20 > oul-=0 OR total oul-70 out 7/0 (2721) OR (2720 8 Ng=0) -> 2×=0 > ou-=0 or ou-10 (27=1) or (ng=1) pc increment by 2 Jump - either Jump shortrucken Logic non Jump sustruction PC

Home work: - complete the design of Junt logic using the work conditional control signals.

Ine-

(8) . Writing bren the result (WB):-

- Writing back the result computed by ALU to respective destination.

Note: - Address/ memory instruction dennot require write back

ALV & Jump Instruction:

