Report

Implementation of FIR Filters

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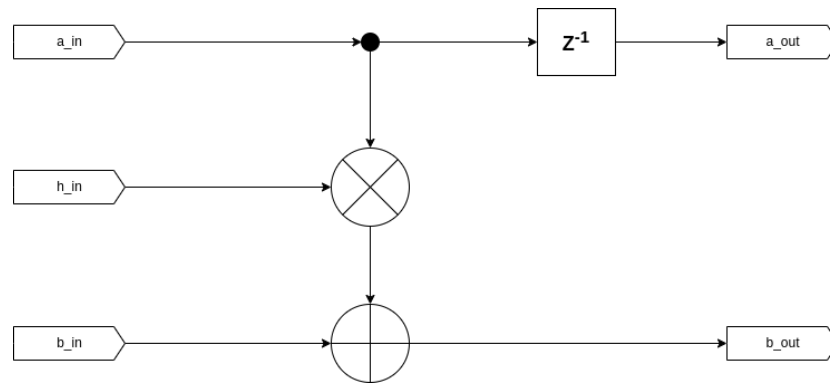March 23, 2024

Figure 1: Single stage of FIR Filter
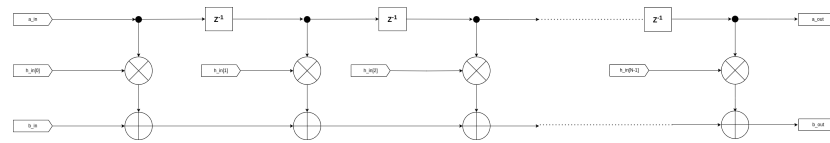

Figure 2: N-stage FIR Filter
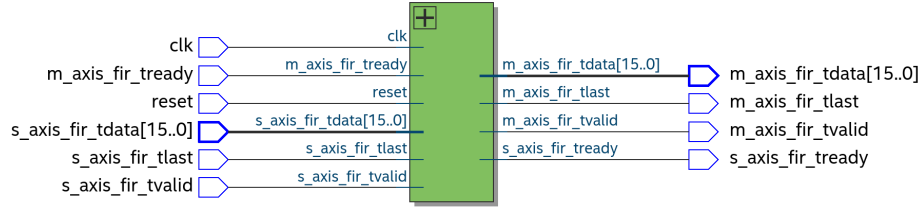
Figure 3: Top Level Schema of FIR Filter

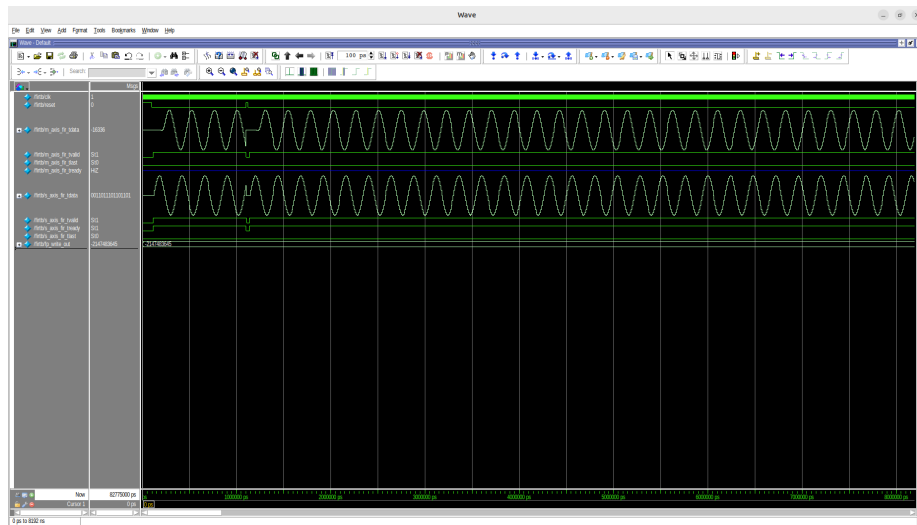| Signal	Interpretation
clk	Input clock signal
$reset$	Global Reset
$s\_axis\_fir\_tdata$	Input data
$s\_axis\_fir\_tvalid$	Valid input data
$s\_axis\_fir\_tready$	FIR module is ready
$s\_axis\_fir\_tlast$	Last Input data
$m\_axis\_fir\_tready$	Downstream channel is ready
$m\_axis\_fir\_tdata$	Output data
$m\_axis\_fir\_tvalid$	Valid output data
$m\_axis\_fir\_tlast$	Last output data

Table 1: Interpreting Signals

Figure 4: Simulation Result