

Report

Pipelining of FIR Filters

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1 Implementation of FIR Filter Without Pipelining

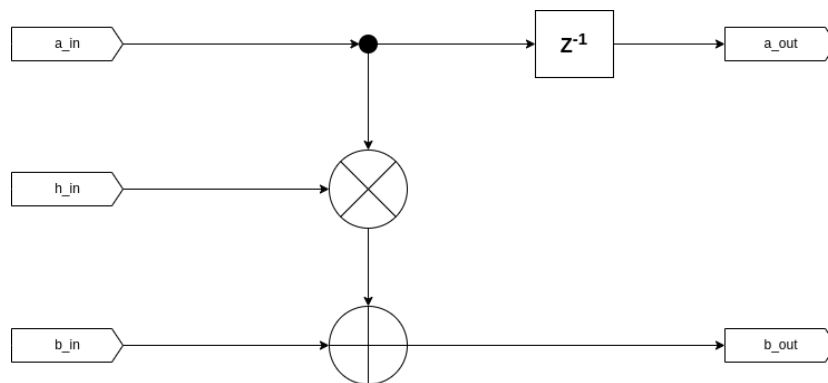


Figure 1: Single stage of FIR Filter

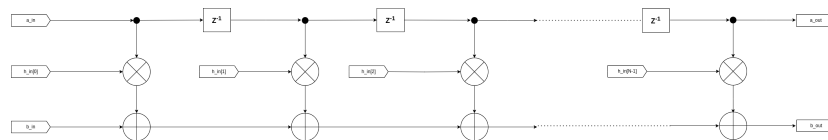


Figure 2: N-stage FIR Filter

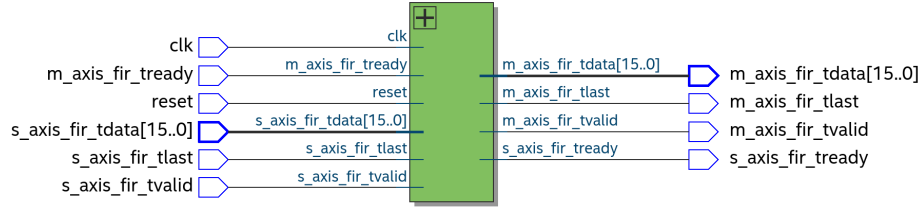


Figure 3: Top Level Schema of FIR Filter

Signal	Interpretation
<i>clk</i>	Input clock signal
<i>reset</i>	Global Reset
<i>s_axis_fir_tdata</i>	Input data
<i>s_axis_fir_tvalid</i>	Valid input data
<i>s_axis_fir_tready</i>	FIR module is ready
<i>s_axis_fir_tlast</i>	Last Input data
<i>m_axis_fir_tready</i>	Downstream channel is ready
<i>m_axis_fir_tdata</i>	Output data
<i>m_axis_fir_tvalid</i>	Valid output data
<i>m_axis_fir_tlast</i>	Last output data

Table 1: Interpreting Signals

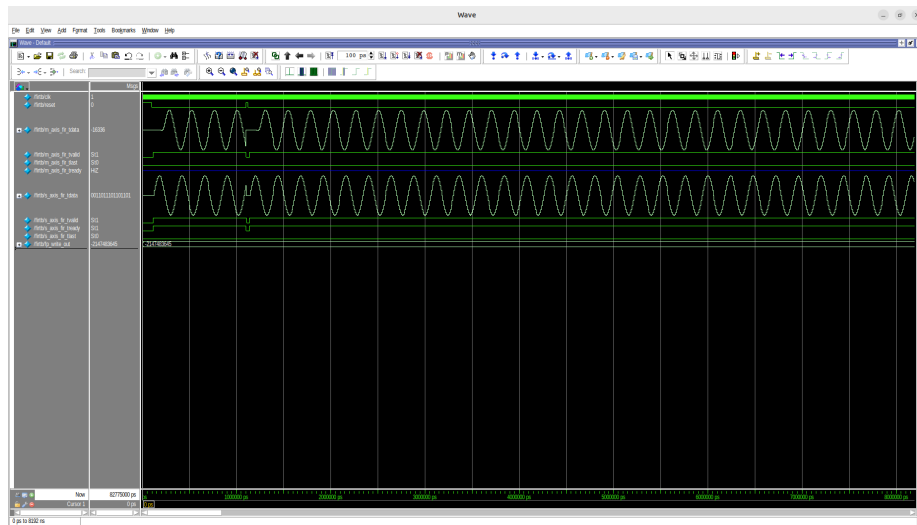


Figure 4: Simulation Result

2 Single stage Pipelining of the FIR Filter at Pth Stage

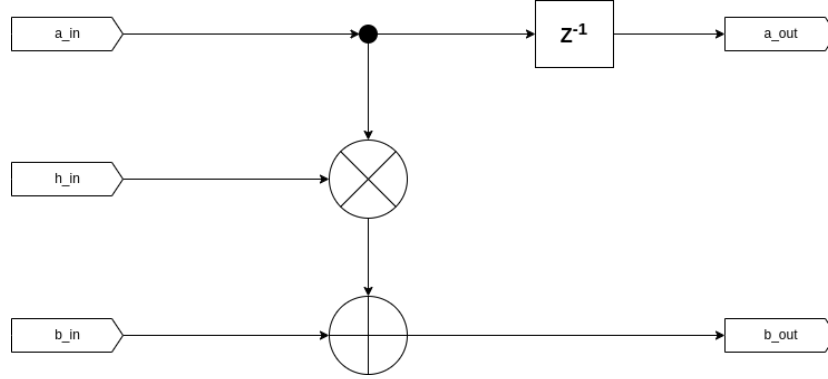


Figure 5: Single stage of FIR Filter

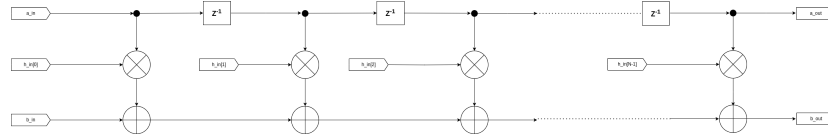


Figure 6: N-stage FIR Filter

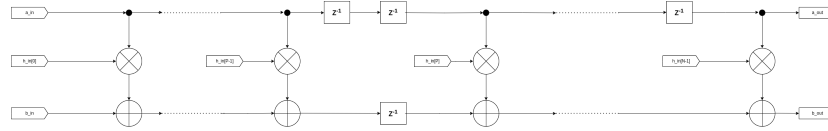


Figure 7: N-stage FIR Filter Pipelined at Pth stage

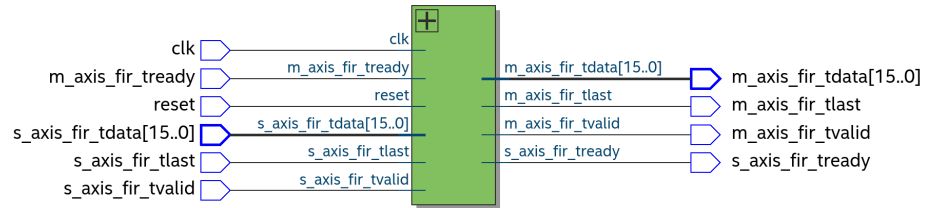


Figure 8: Top Level Schema of FIR Filter

Signal	Interpretation
<i>clk</i>	Input clock signal
<i>reset</i>	Global Reset
<i>s_axis_fir_tdata</i>	Input data
<i>s_axis_fir_tvalid</i>	Valid input data
<i>s_axis_fir_tready</i>	FIR module is ready
<i>s_axis_fir_tlast</i>	Last Input data
<i>m_axis_fir_tready</i>	Downstream channel is ready
<i>m_axis_fir_tdata</i>	Output data
<i>m_axis_fir_tvalid</i>	Valid output data
<i>m_axis_fir_tlast</i>	Last output data

Table 2: Interpreting Signals

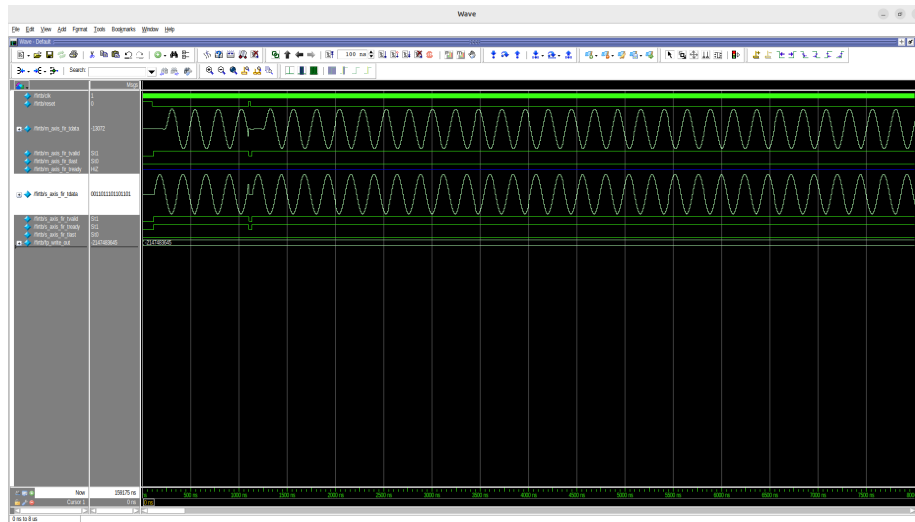


Figure 9: Simulation Result

3 N-1 stages Pipelining of the FIR Filter

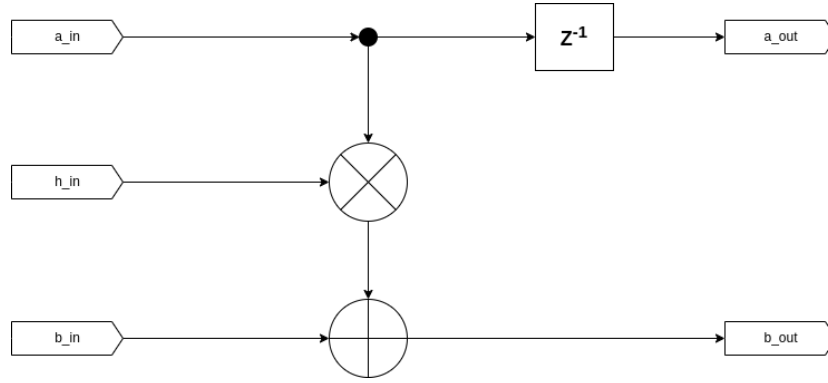


Figure 10: Single stage of FIR Filter

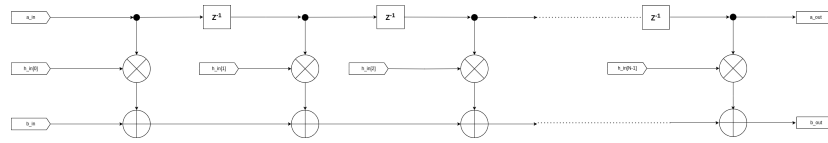


Figure 11: N-stage FIR Filter

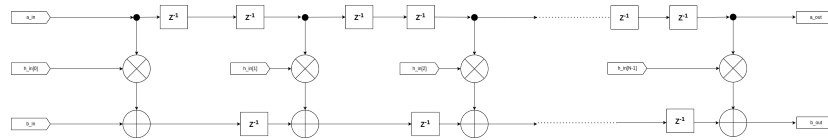


Figure 12: N-stage FIR Filter Pipelined at N-1 stages

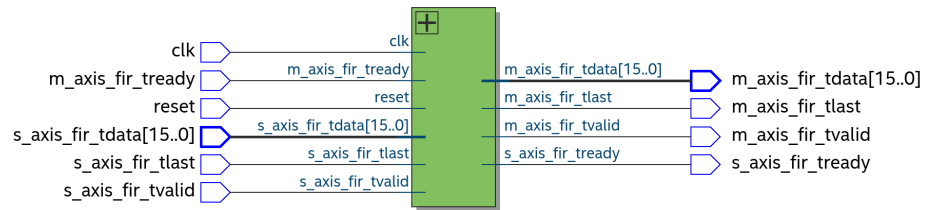


Figure 13: Top Level Schema of FIR Filter

Signal	Interpretation
<i>clk</i>	Input clock signal
<i>reset</i>	Global Reset
<i>s_axis_fir_tdata</i>	Input data
<i>s_axis_fir_tvalid</i>	Valid input data
<i>s_axis_fir_tready</i>	FIR module is ready
<i>s_axis_fir_tlast</i>	Last Input data
<i>m_axis_fir_tready</i>	Downstream channel is ready
<i>m_axis_fir_tdata</i>	Output data
<i>m_axis_fir_tvalid</i>	Valid output data
<i>m_axis_fir_tlast</i>	Last output data

Table 3: Interpreting Signals

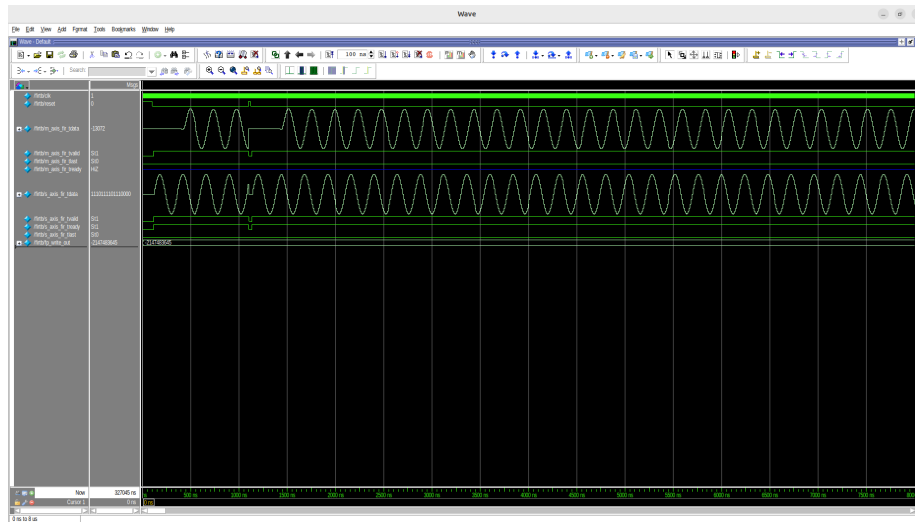


Figure 14: Simulation Result