NG SHU JIE

Final-Year Computer Engineering Student | Digital Systems & FPGA Enthusiast

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SUMMARY

Final-year Computer Engineering student at UTAR with hands-on experience in processor architecture, RTL design, and hardware verification. Proficient in SystemVerilog, ModelSim, and Vivado. Demonstrated leadership and event coordination through organizing campus-wide financial talk. Seeking a 3-month internship (27 Oct 2025 – 24 Jan 2026) to contribute to FPGA, IC, or microprocessor development while deepening expertise in digital circuit design.

SKILLS AND TOOLS

Technical Skills

- **Languages**: SystemVerilog, Verilog, Assembly, Python, C/C++, MATLAB, HTML/CSS/JavaScript
- **Concepts**: Processor Architecture (RISC-V, MIPS, ARM), FSM Design, Digital Signal Processing, Machine Learning
- **OS:** Windows (XP–11), Ubuntu Linux

Tools & Platforms

- **Simulation & Synthesis**: Vivado, Modelsim, Quartus Prime
- **IDEs**: Visual Studio Code, MATLAB, ArduinoIDE, Keil uVision3

Languages

- Mandarin Chinese (Native), English (Fluent), Malay (Intermediate), Japanese (Basic)

PROJECTS

MIPS Multi-Cycle Processor Design

Team-based Project (3 Members) | SystemVerilog, Vivado Jul 2025 - Present

- Architected modular RTL components (Datapath, Control Unit, ALU, Memory, CP0) for multi-cycle MIPS processor
- Developed instruction-level test suites covering arithmetic, branching, memory access, and exception handling
- Integrated C/C++ programs into MIPS assembly for test generation to validate system-level behaviour
- Debugged timing and functional mismatches via waveform analysis in Vivado Simulator
- Documented architectural design, module interfaces, and verification outcomes for reproducibility

RISC-V Pipeline Processor Design : Specification Development

Team-based Project (4 Members) | SystemVerilog, ModelSim, Quartus Prime Jul 2024 - Sep 2024

- Led RTL development of 5-stage pipelined RISC-V CPU with hazard detection and forwarding logic
- Designed control signals for stalls, flushes, and branch prediction mechanisms
- Created cycle-accurate testbenches to validate instruction flow and resolve data hazards
- Achieved 95% functional coverage across instruction set and control scenarios using ModelSim
- Presented architectural specifications and verification results in team-based documentation

EDUCATION

Universiti Tunku Abdul Rahman - Kampar, Perak, Malaysia

Bachelor of Information Technology (Honours) Computer Engineering - 3.47 Jun 2023 - Jun 2026

LEADERSHIP & EXTRACURRICULAR ACTIVITIES

Finance Leader – "Start Managing Your Personal Finance" Talk (Nov 2024)

- Spearheaded planning and budgeting for a university-wide financial literacy event
- Coordinated with external financial professionals to deliver talks on investment, budgeting, and career finance
- Managed logistics, venue setup, and promotional outreach, attracting over 70 student attendees
- Strengthened team collaboration and public engagement through effective communication and leadership
- Enhanced stakeholder coordination and time management under tight planning timelines