Assignment - 05

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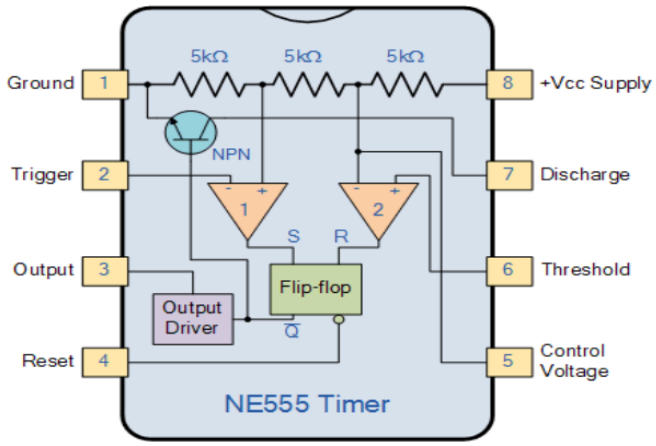
EE22BTECH11025

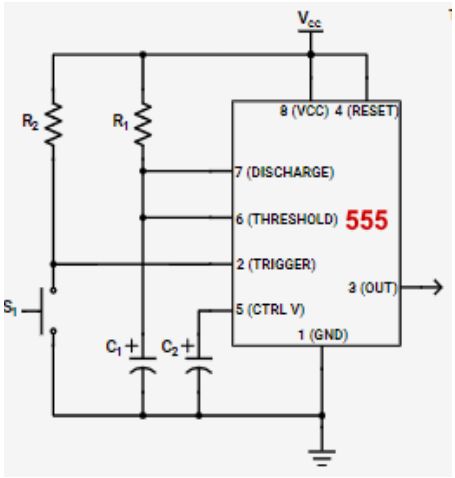
Q1.a) Monostable mode for a variable period of mono pulse varying from 100us to 1 ms.

Solution: In monostable mode, the 555 timer generates a single pulse (high output) when triggered externally. The duration of this pulse is determined by external components, primarily a resistor (R) and a capacitor (C), connected to the IC.

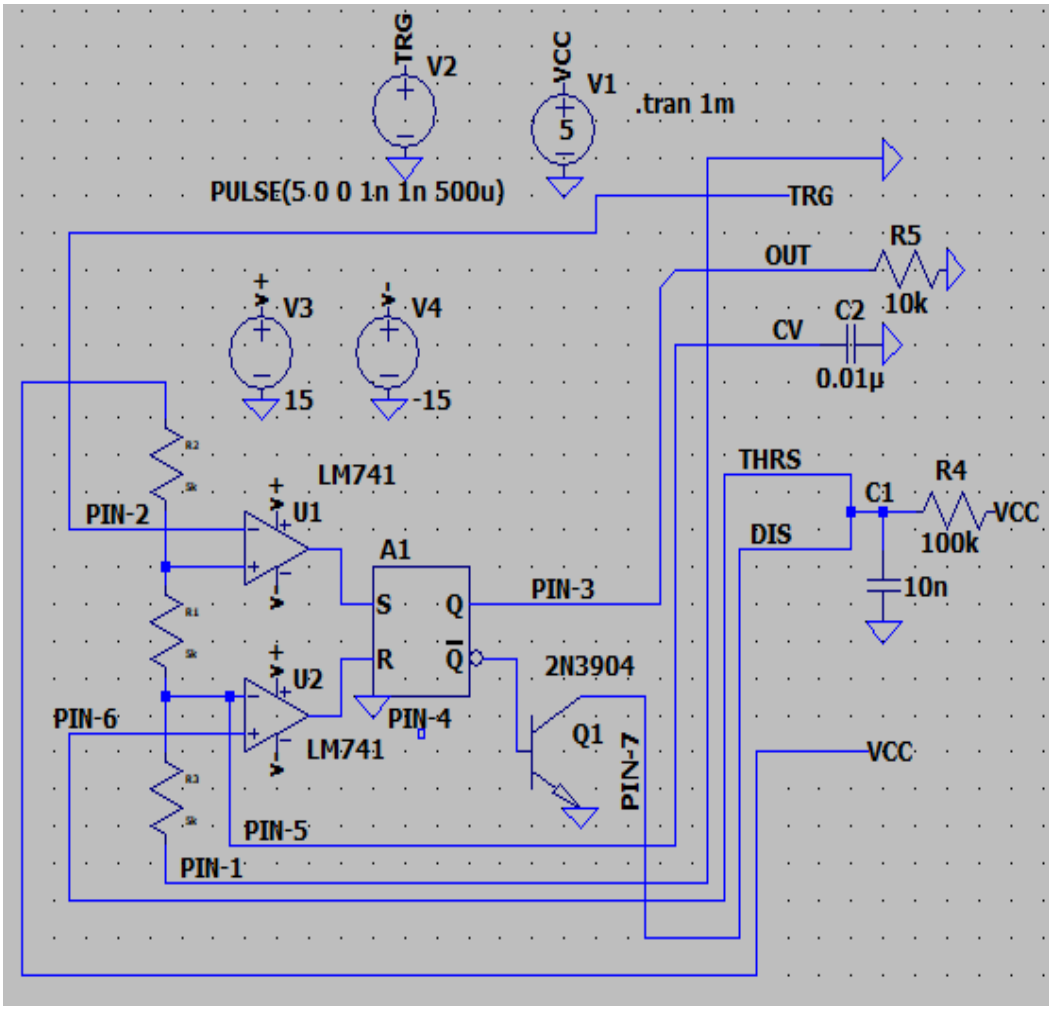
- Triggering the timer with a negative pulse on pin 2 causes the output (pin 3) to go high.
- The capacitor (C) charges through the resistor (R), determining the pulse duration $T = 1.1 \times R \times C$.
- Once the capacitor voltage reaches the threshold level (2/3 Vcc), the output returns to low, ending the pulse.

The reference circuit used,





The circuit used

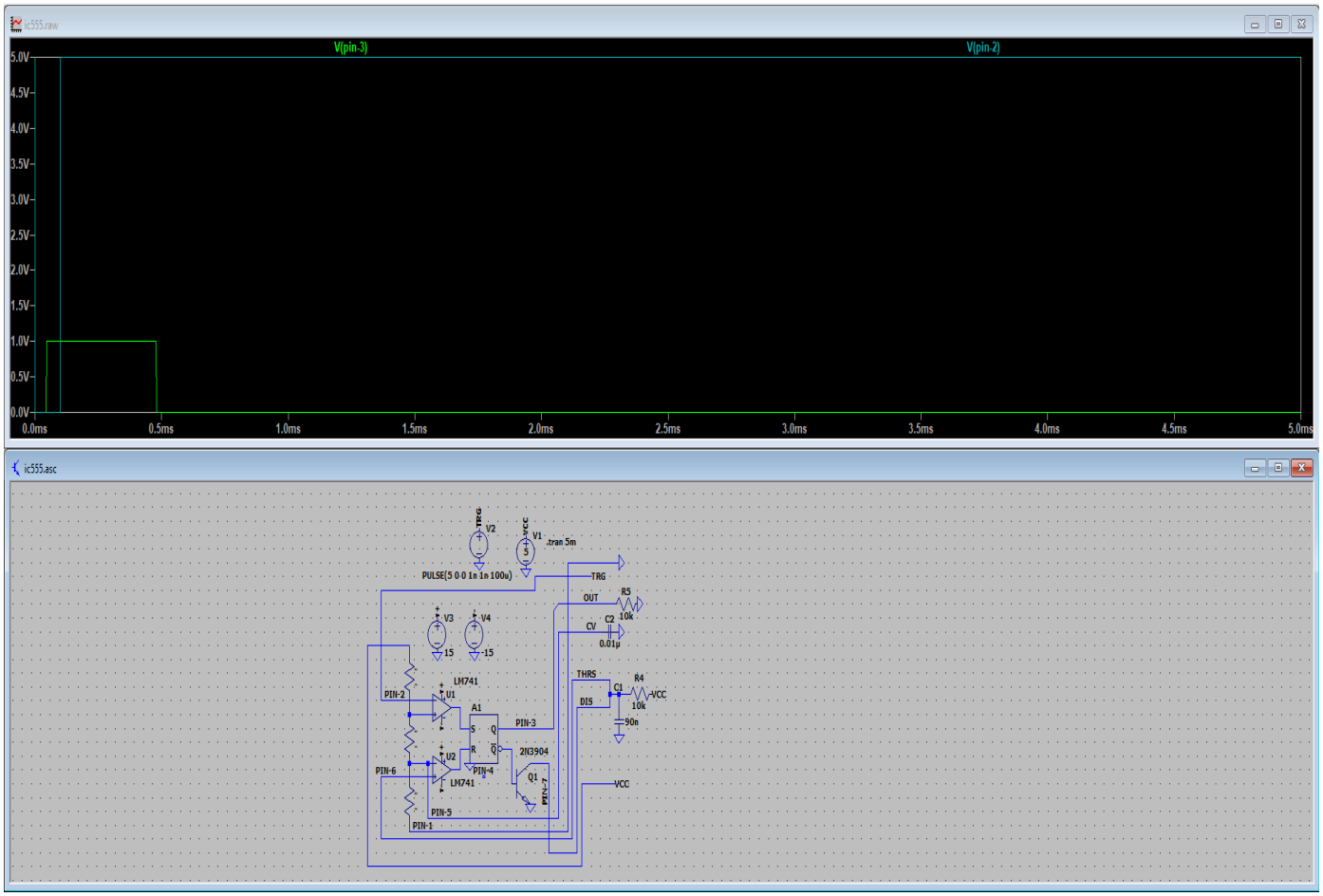


Formula:-

$T = 1.1\,RC$ which is the T_{on} of the output(pin-3) pulse

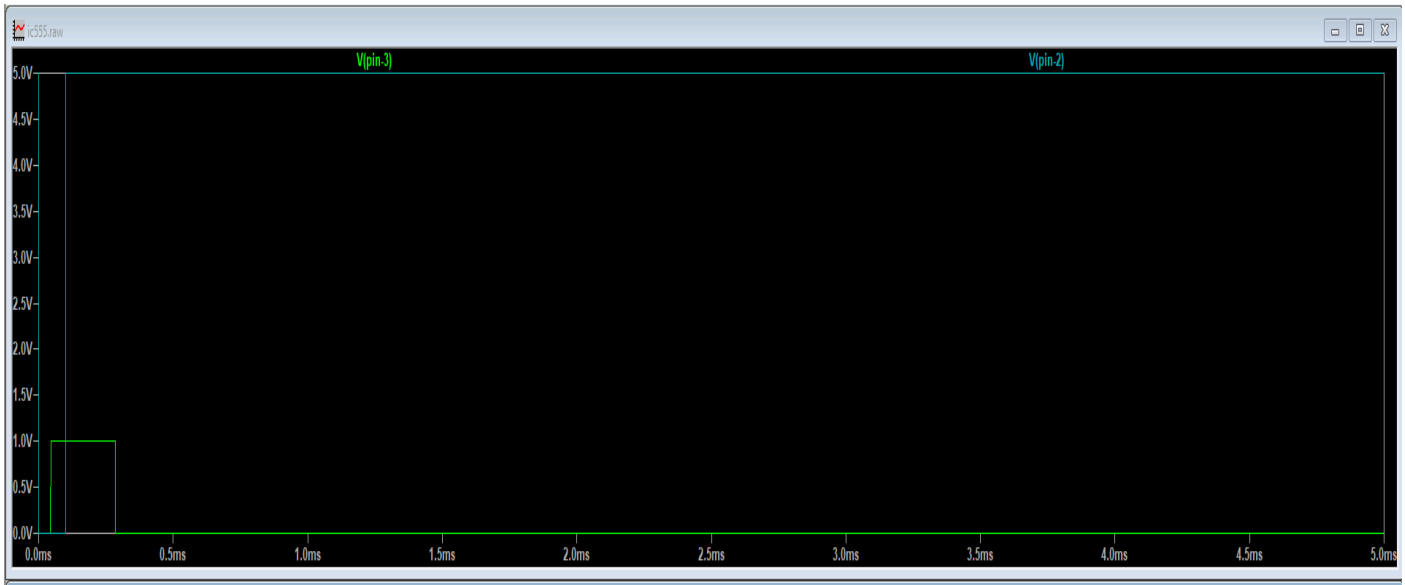
NOTE: I have named the operating point of the circuit as the block IC (NE555) PINs for more straightforward implementation.

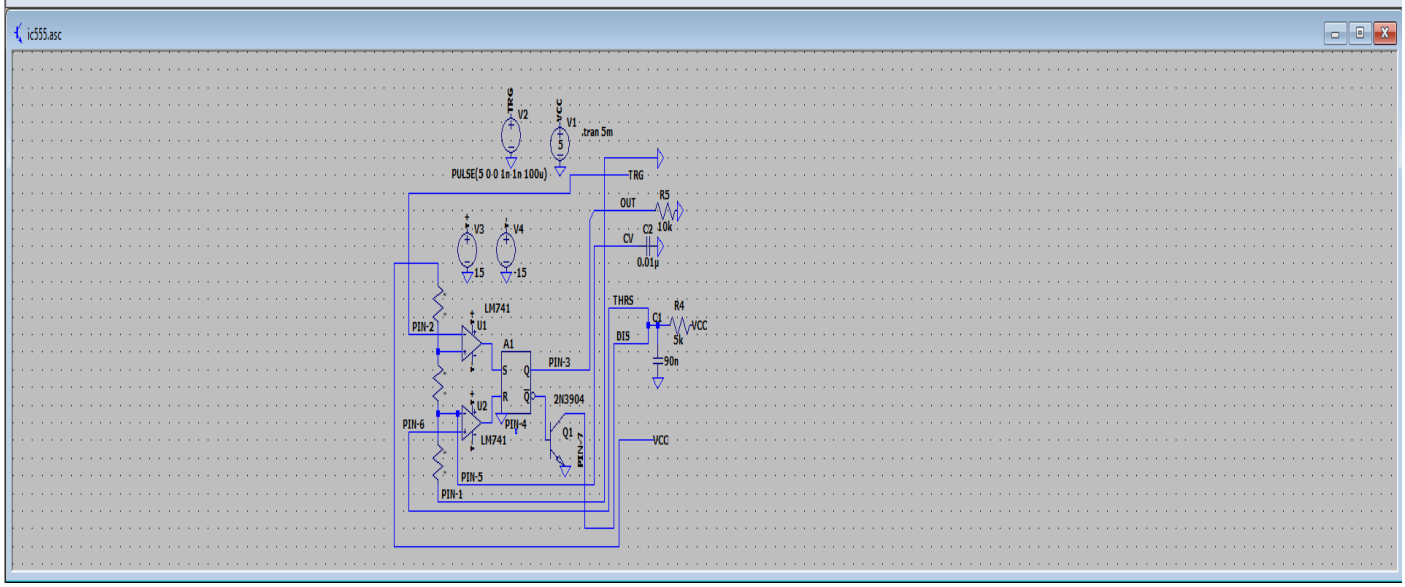
Case-1 [T_{on} = 1.1 x 10k x 90 = 0.99ms]



The output pulse width is nearly 1 ms (0.990 ms), close to the upper limit of the specified range (1 ms). This indicates that with a larger resistor value (10kΩ) and a fixed capacitor value (90nF), the monostable multivibrator produces a longer output pulse.

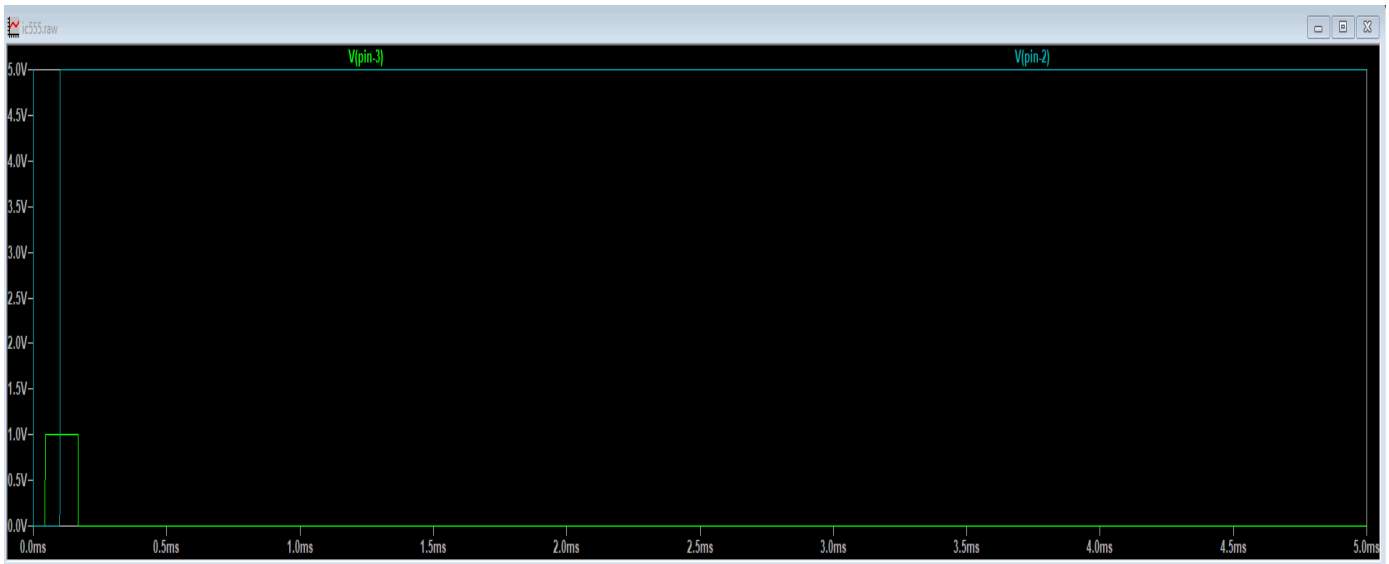
Case-2 [T_{on} = 1.1 x 5k x 90n = 0.495ms]

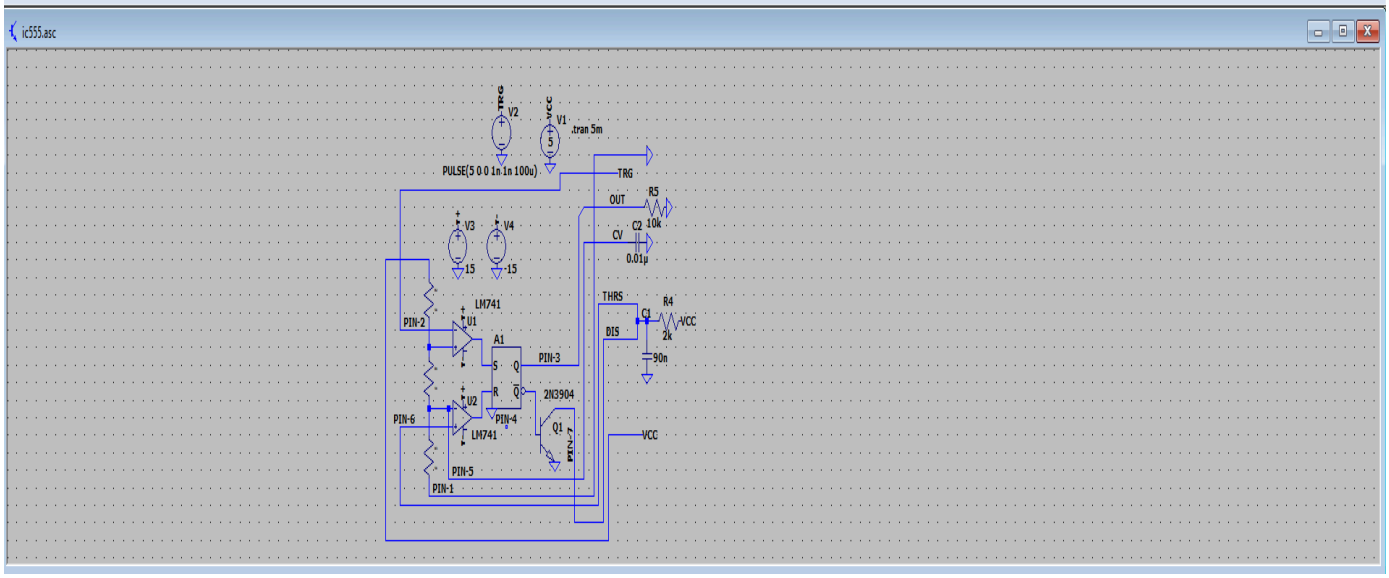




Here, the output pulse width is about 0.495 ms, midway within the desired range. A lower RC value than Case 1 leads to a shorter pulse width.

Case-3[T_{on} = 1.1 x 2k x 90n = 0.198ms]

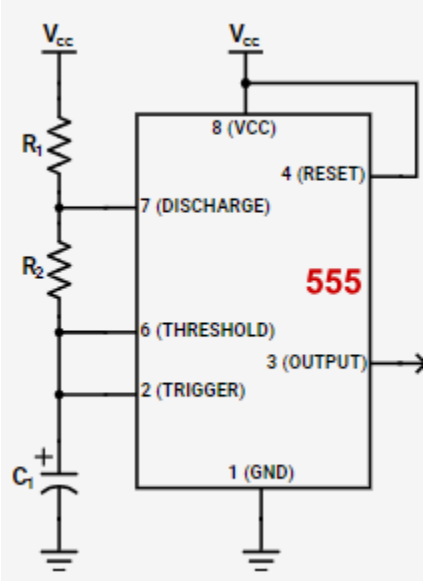




With the smallest resistor value of 2kΩ, the output pulse width is the shortest at 0.198 ms.

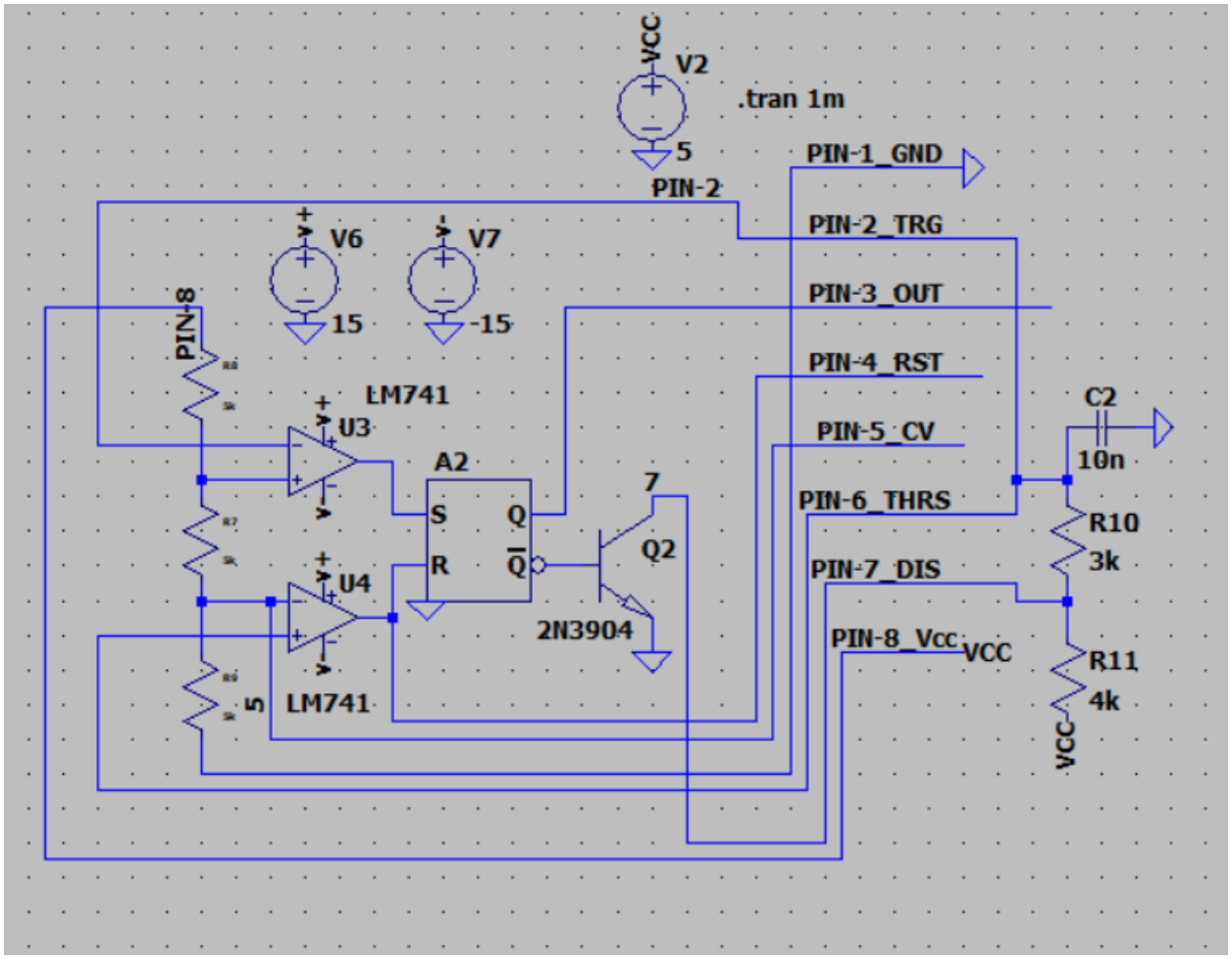
Q1.b)Astable mode for a duty cycle of 70% with the fundamental frequency varying from 2 kHz to 20 kHz. Also, find the maximum frequency achievable.

Solution: The circuit used ,



Working;

- Initially, the capacitor C is charged through R1 and R2.
- When the voltage across the capacitor reaches the threshold level (2/3 VCC), the internal flip-flop of the 555 timer changes state, causing the output (pin 3) to go low.
- This discharges the capacitor C through R2, until the voltage across the capacitor falls to the trigger level (1/3 VCC).
- The flip-flop then changes state again, and the cycle repeats, producing a continuous square wave at the output.



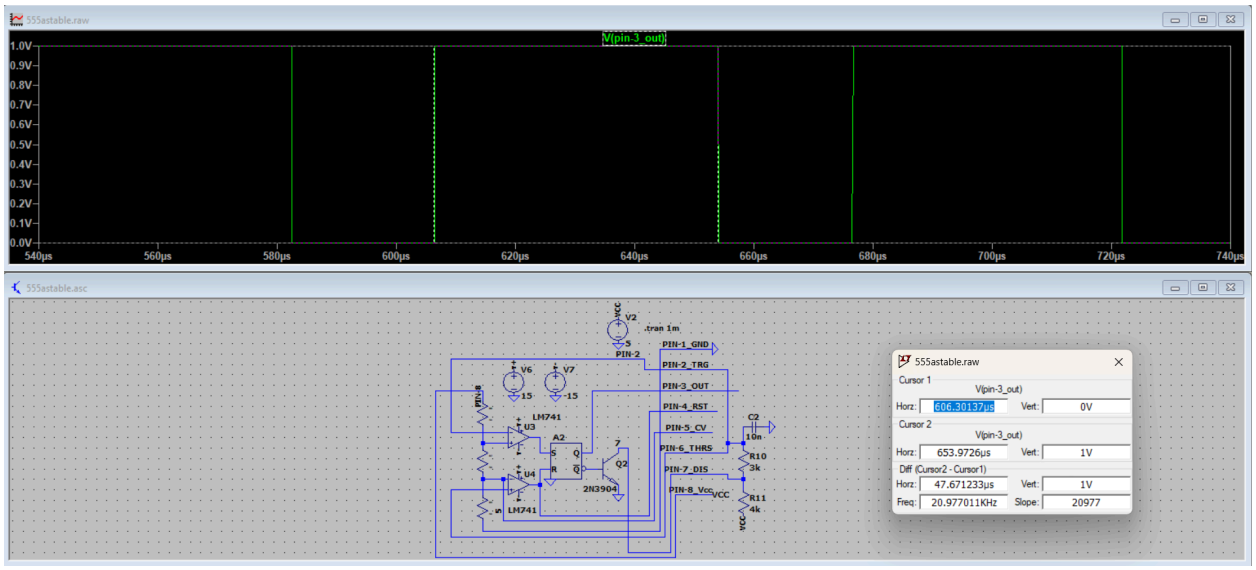
Taking R1 = 3k, R2= 4k ,C1= 10n

Formula used,

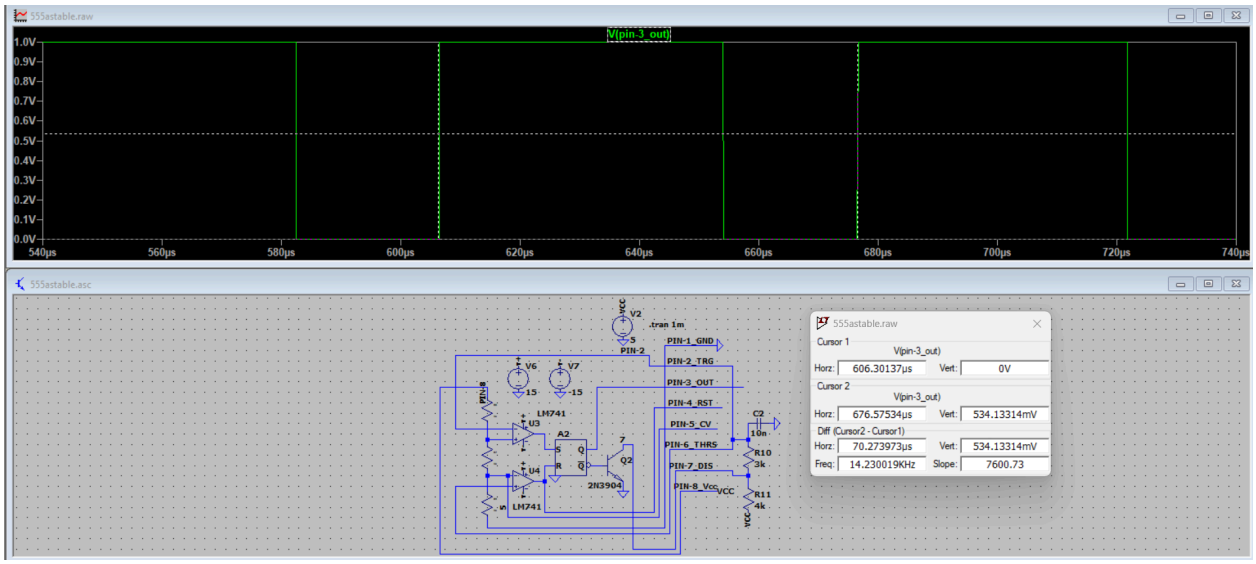
$Ton = 0.693(R1 + R2)C1$, $Toff = 0.693(R2)C1$

$f = \frac{1.44}{(R1+2R2)C1}$

Putting the values in the formula
Ton = 67.1 us ,Toff = 31.2 us ,f_max = 10kHz
Duty cycle approx 68%



Ton = 47 us



Ton + Toff = 70 us

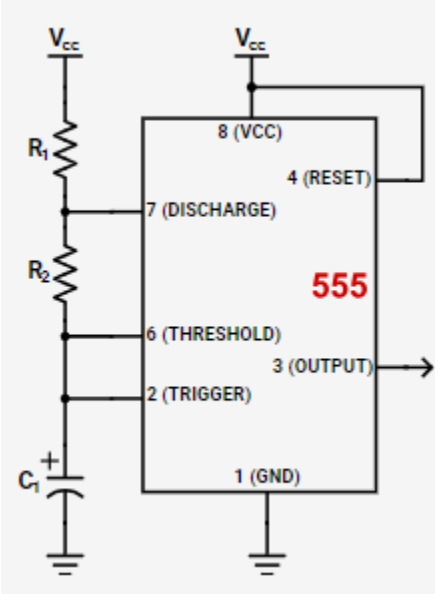
Maximum Frequency = 14.28 Khz

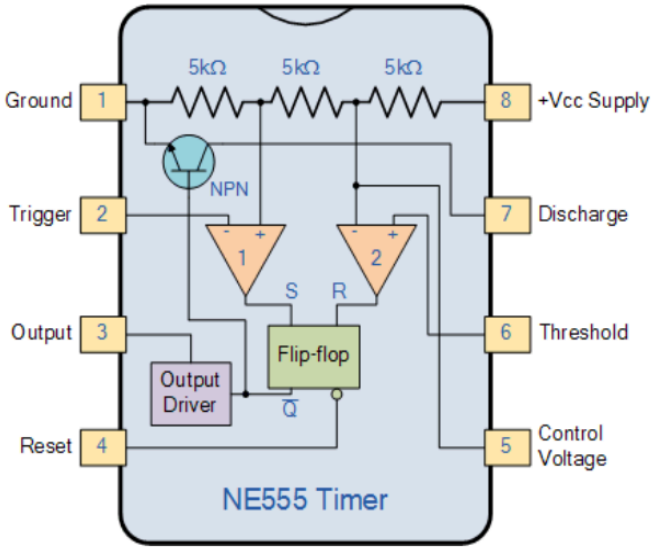
duty cycle = 67%

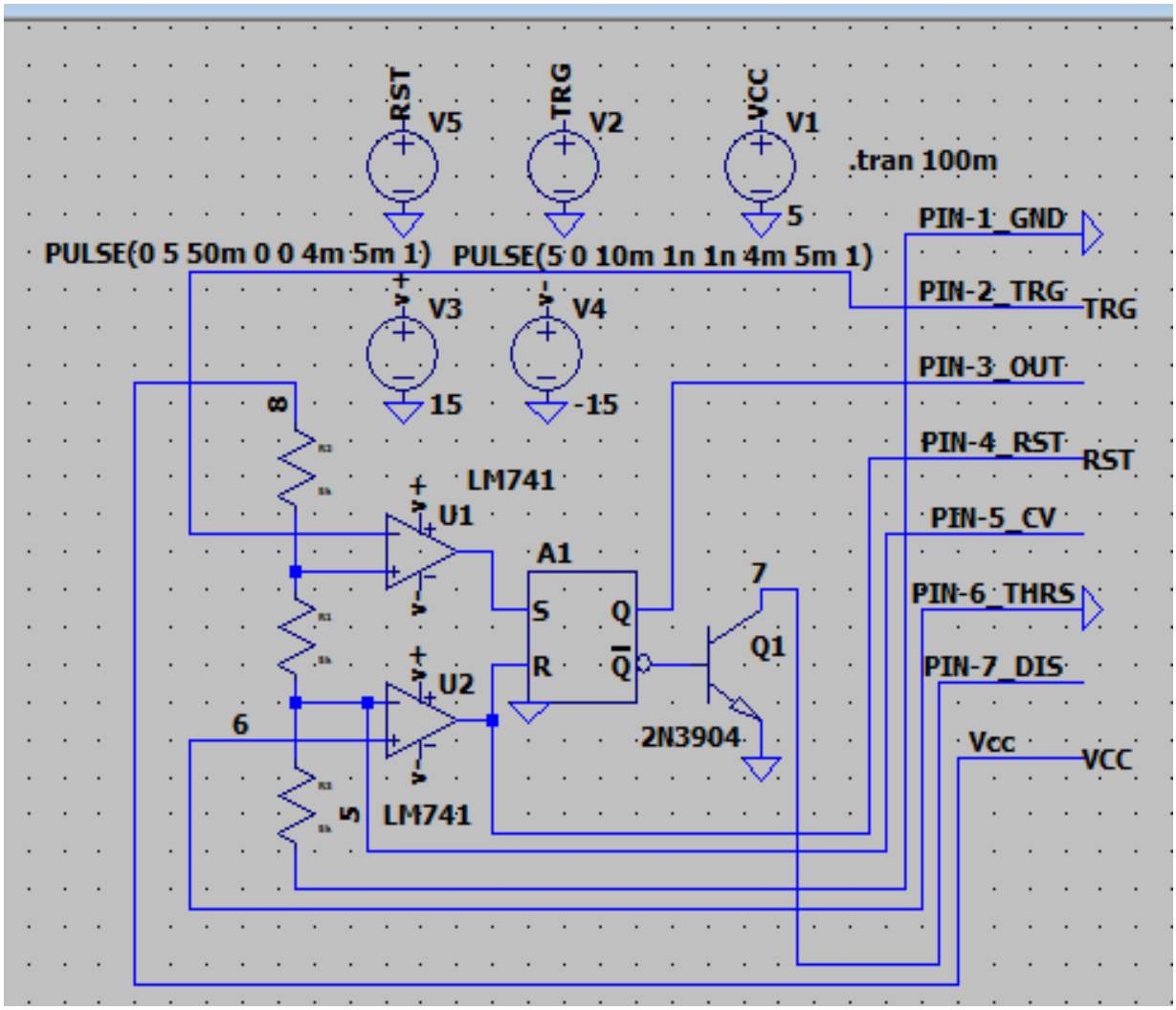
(Q1.c) Bistable mode

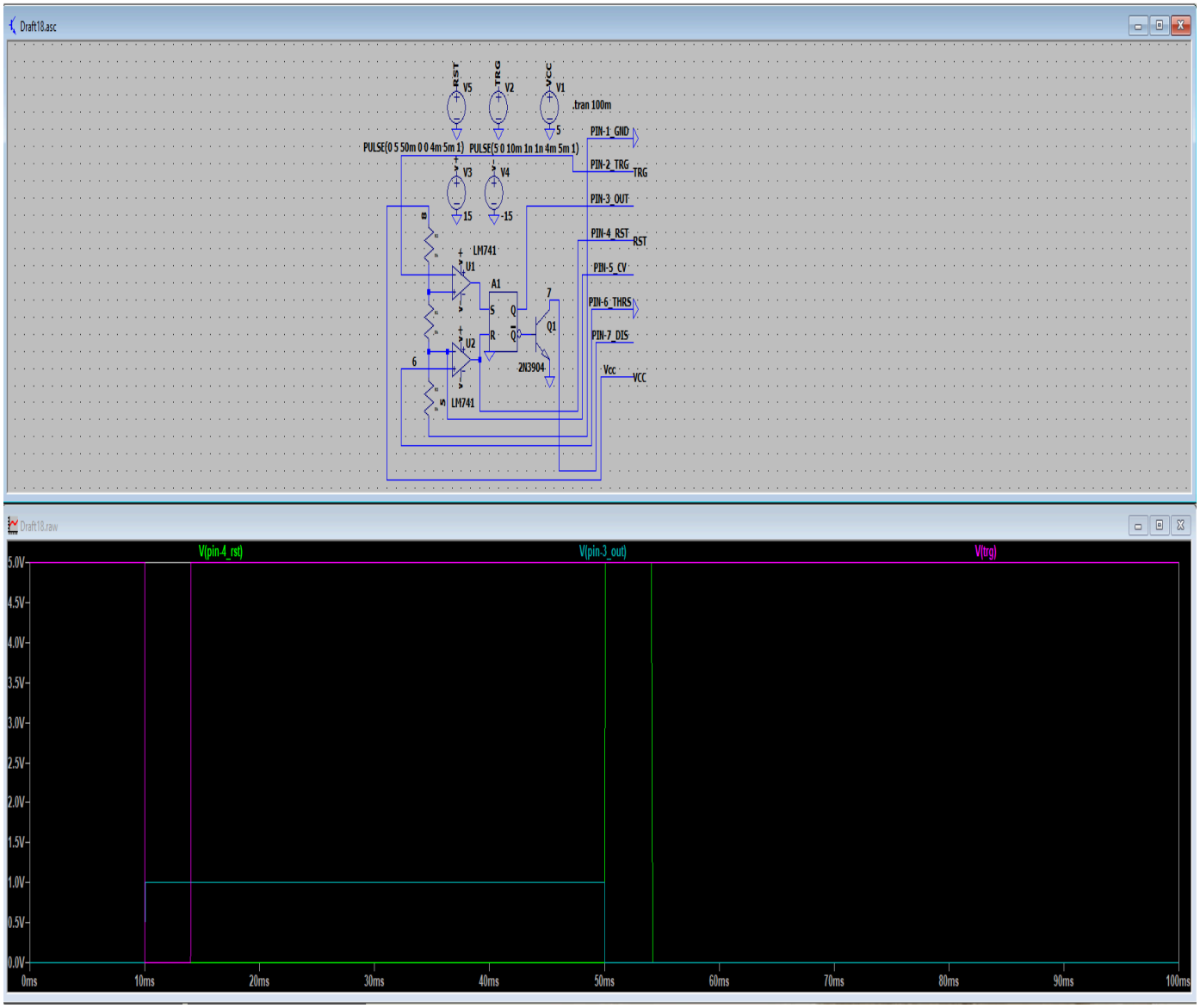
Solution:
The bistable mode of the NE555 timer, also known as the flip-flop or toggle mode, allows the timer to act as an essential binary memory element. This mode creates circuits that latch between two stable states based on external trigger signals.

The circuit used






RST
V5
TRG
V2
VCC
V1
.tran 100m
5
PULSE(0 5 50m 0 0 4m 5m 1)
PULSE(5 0 10m 1n 1n 4m 5m 1)
PIN-1_GND
PIN-2_TRG
TRG
V3
V4
PIN-3_OUT
15
-15
8
PIN-4_RST
RST
LM741
U1
PIN-5_CV
A1
7
S
Q
PIN-6_THRS
Q1
R
Q
U2
PIN-7_DIS
6
2N3904
Vcc
VCC
5
LM741



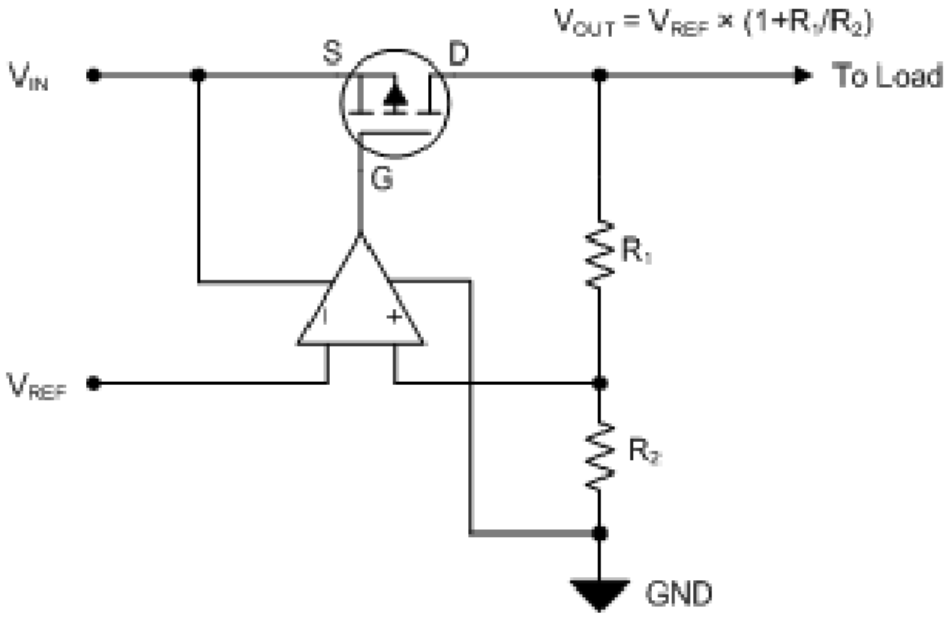
Working:

- Output (Pin 3) is stable (e.g., Low).
- First, a pulse is applied to the trigger pin (Pin 2).
- This sets the flip-flop to a new state (e.g., HIGH)[blue pulse]
- Apply a pulse to the reset pin (Pin 4) after triggering.
- The reset pin is connected to the ground (GND), so this pulse resets the flip-flop state.
- After the trigger pulse (setting to HIGH) and then the reset pulse (forcing a reset),
- The output state changes from its initial state to the opposite (e.g., LOW).
- The NE555 timer remains in this new state until triggered or reset again.

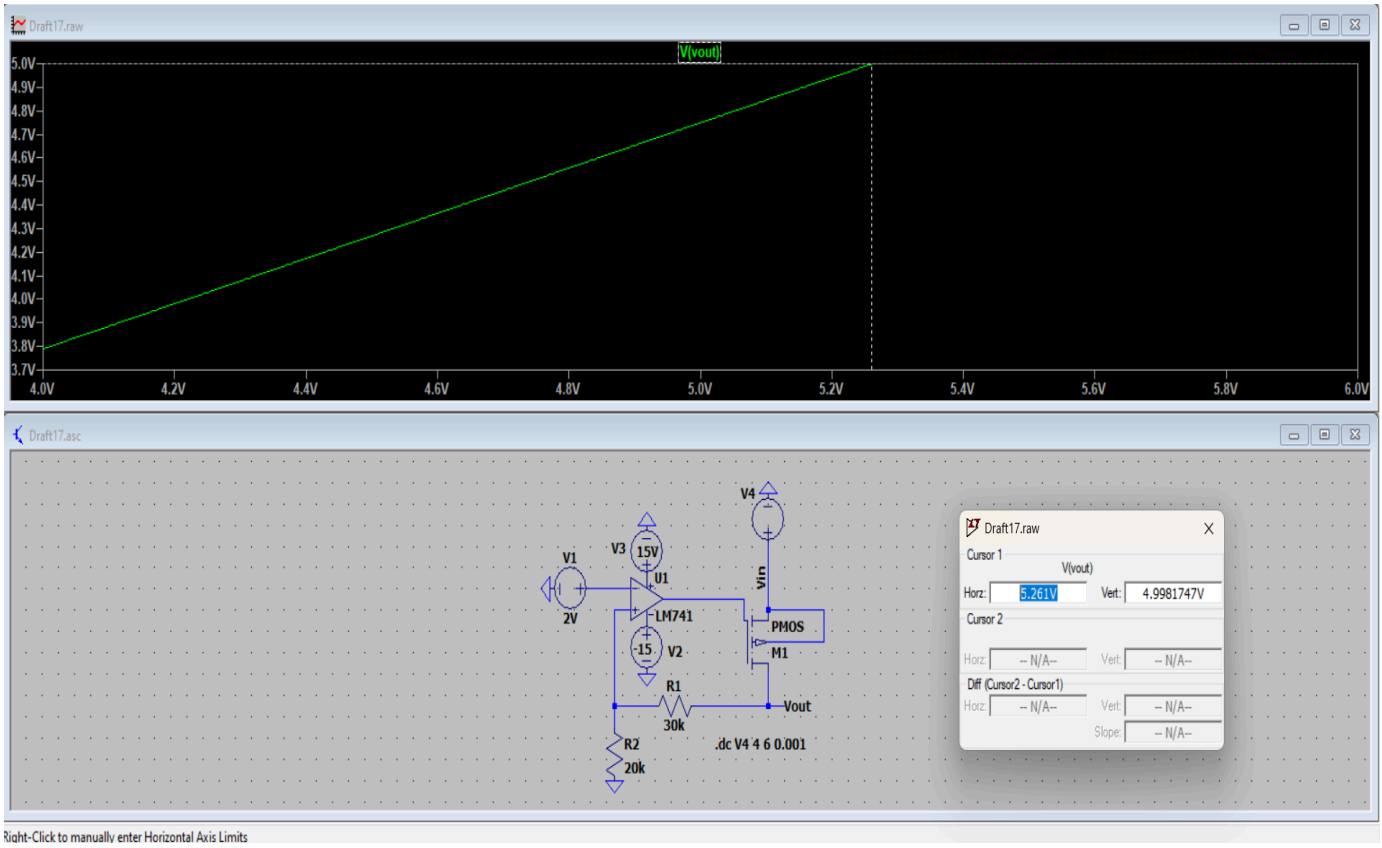
(Q2) Consider pMOS and nMOS MOSFET-based LDOs with Vref = 2V. Design the system for Vout ranging from 5 to 9 Volts (variable). Design the LDOs with a minimum value of Vin in each case for the entire range. Consider the value of current required is 100uA and W/L of the devices (pMOS and nMOS) is 10/1.

Solution:

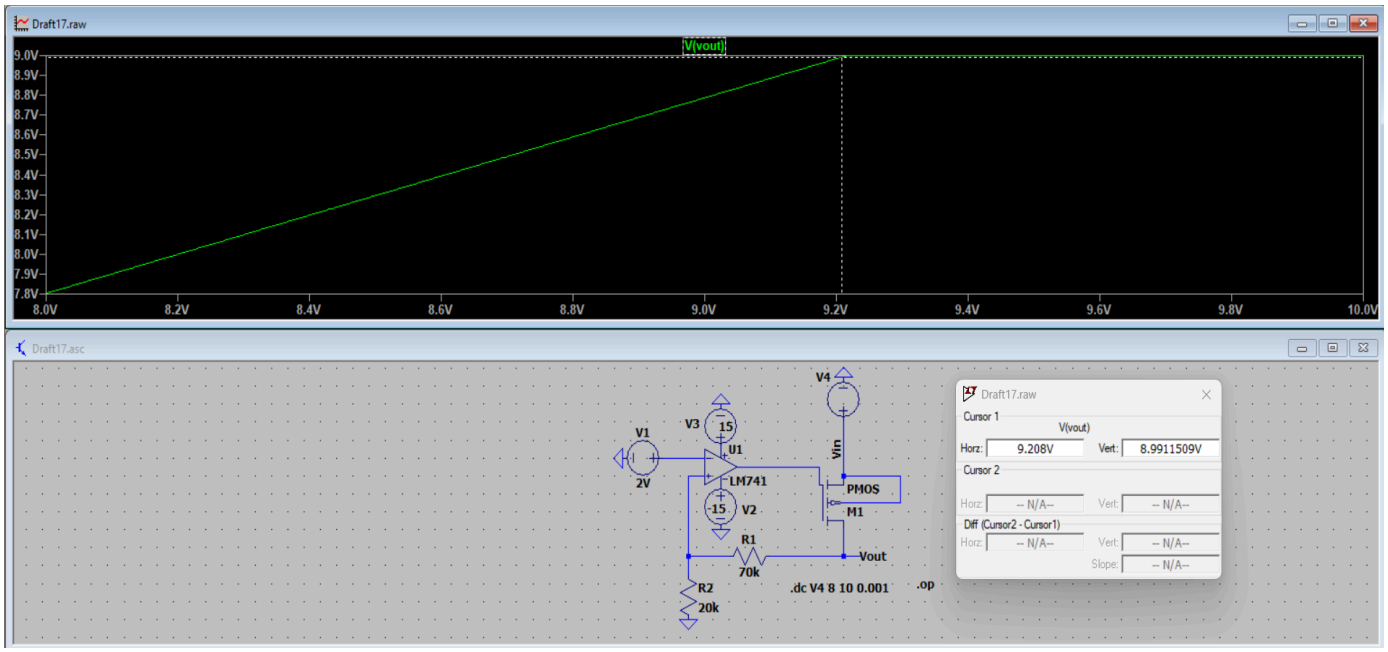
Reference circuit for pMOS,



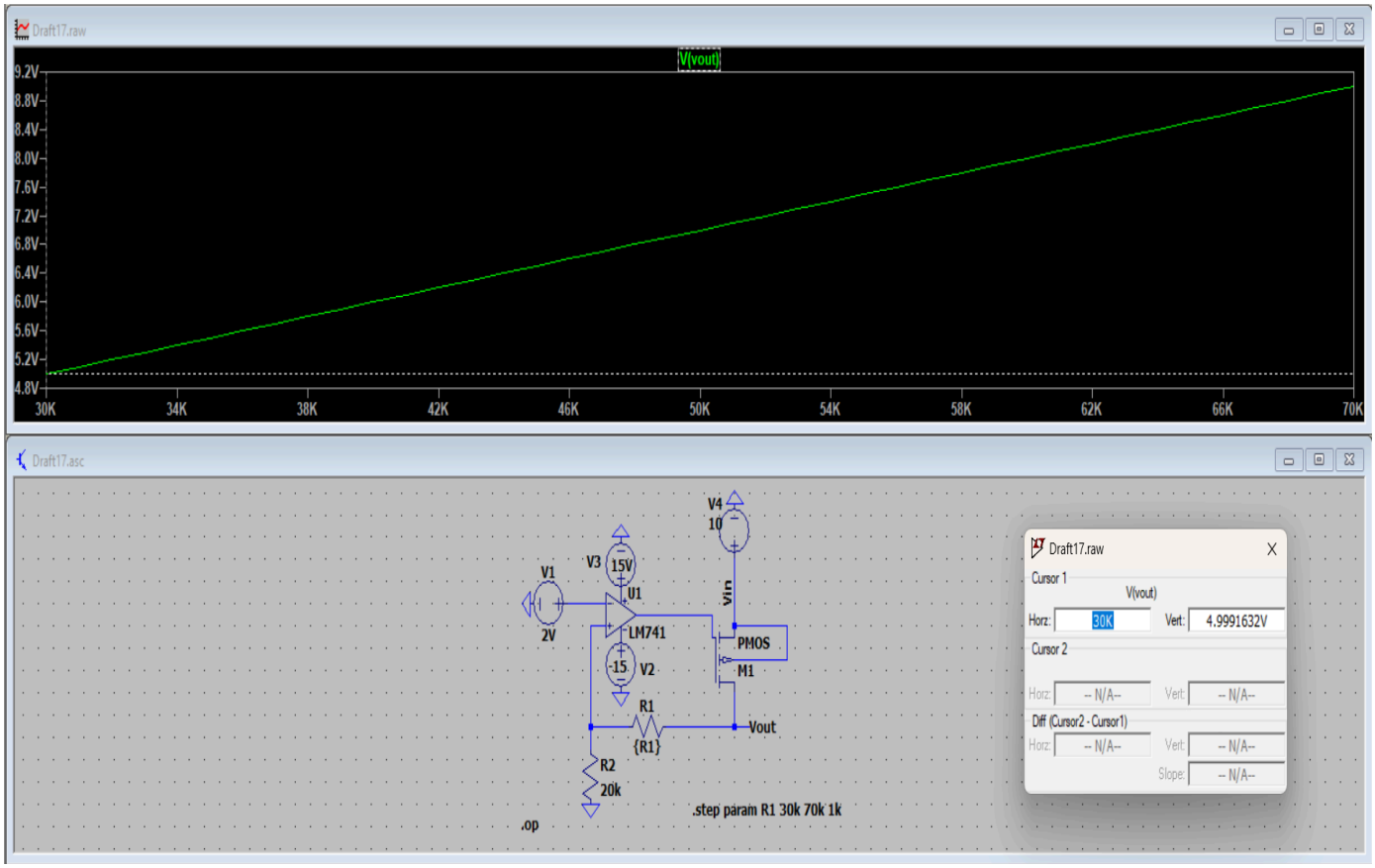
Case-1 pMOS



The value of Vmin(input) for output of 5V , we used DC sweeping of the voltage V4 labelled in the circuit and found that the minimum value of input is 5.261V as if we increase the voltage the output is constant at 5V.



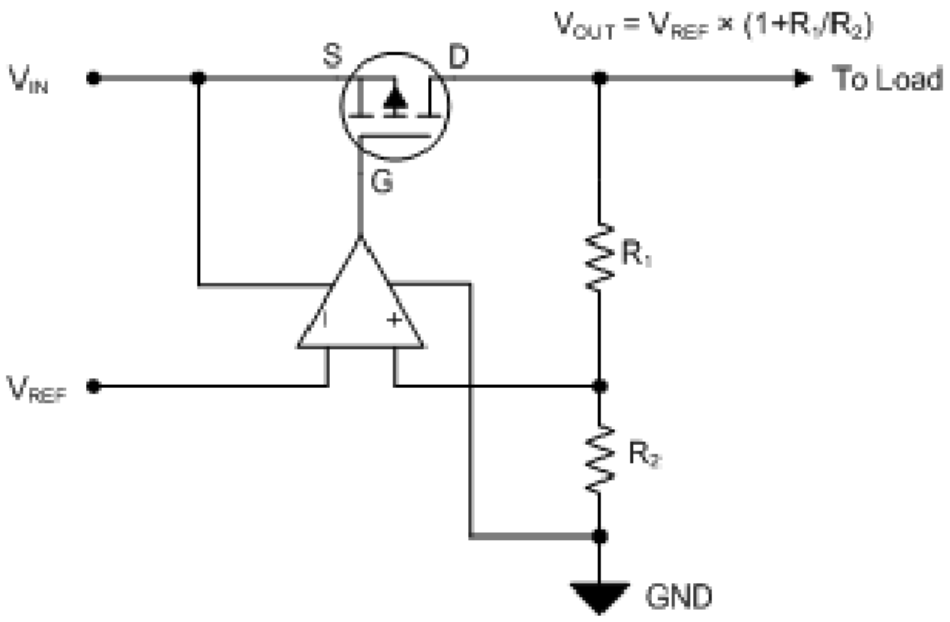
Similarly, we again used DC sweep to calculate the Vmin for output at 9V and we found that to be 9.208V.



We vary the value of resistor R1 across a range determined by the calculated formula:

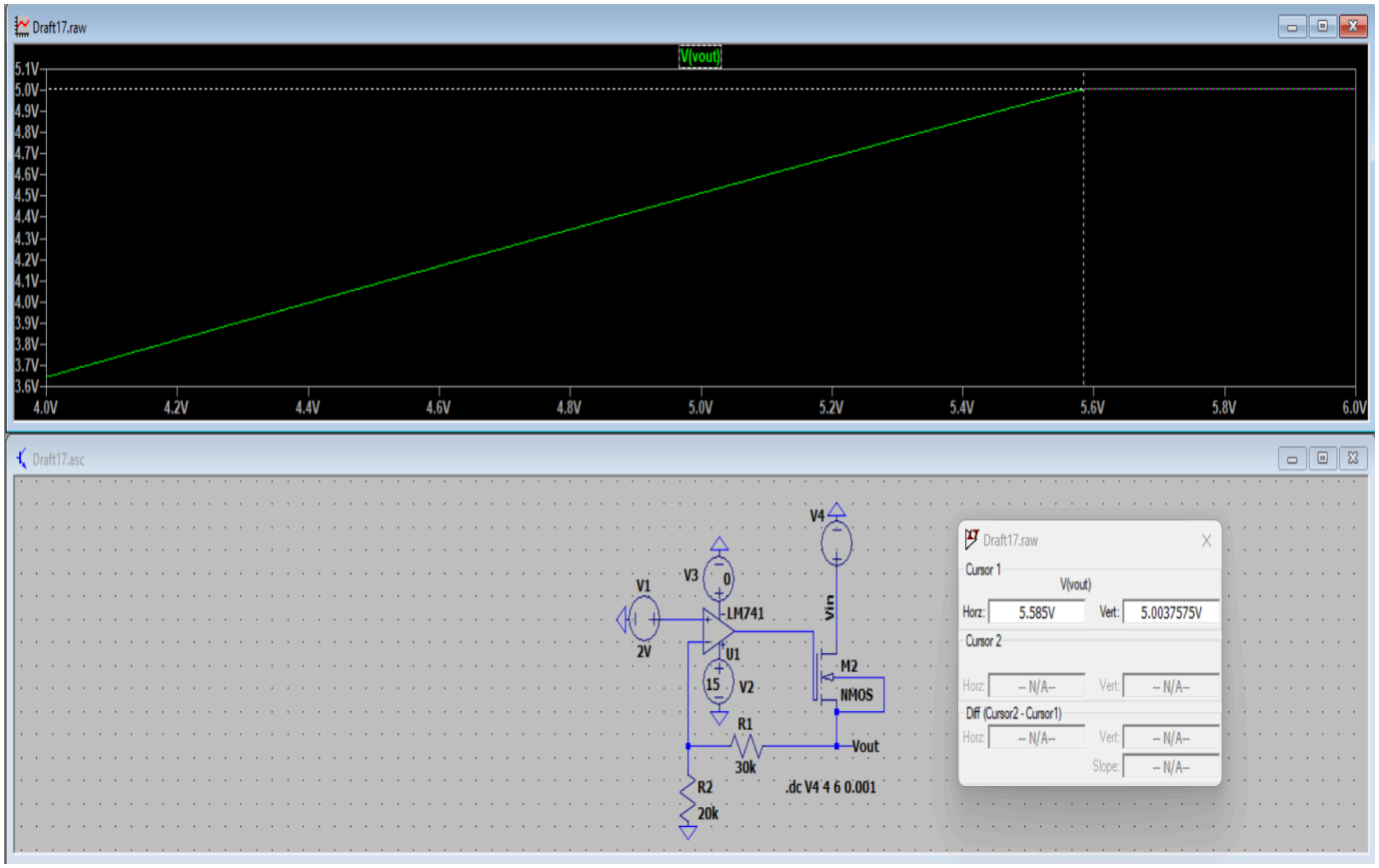
The specific values of R1 are adjusted based on the desired output voltage, following a calculated relationship. For instance, R1 is set to 30k ohms to achieve a 5V output and 70k ohms for a 9V output, with a fixed reference voltage Vref of 2V.

Reference circuit for nMos,

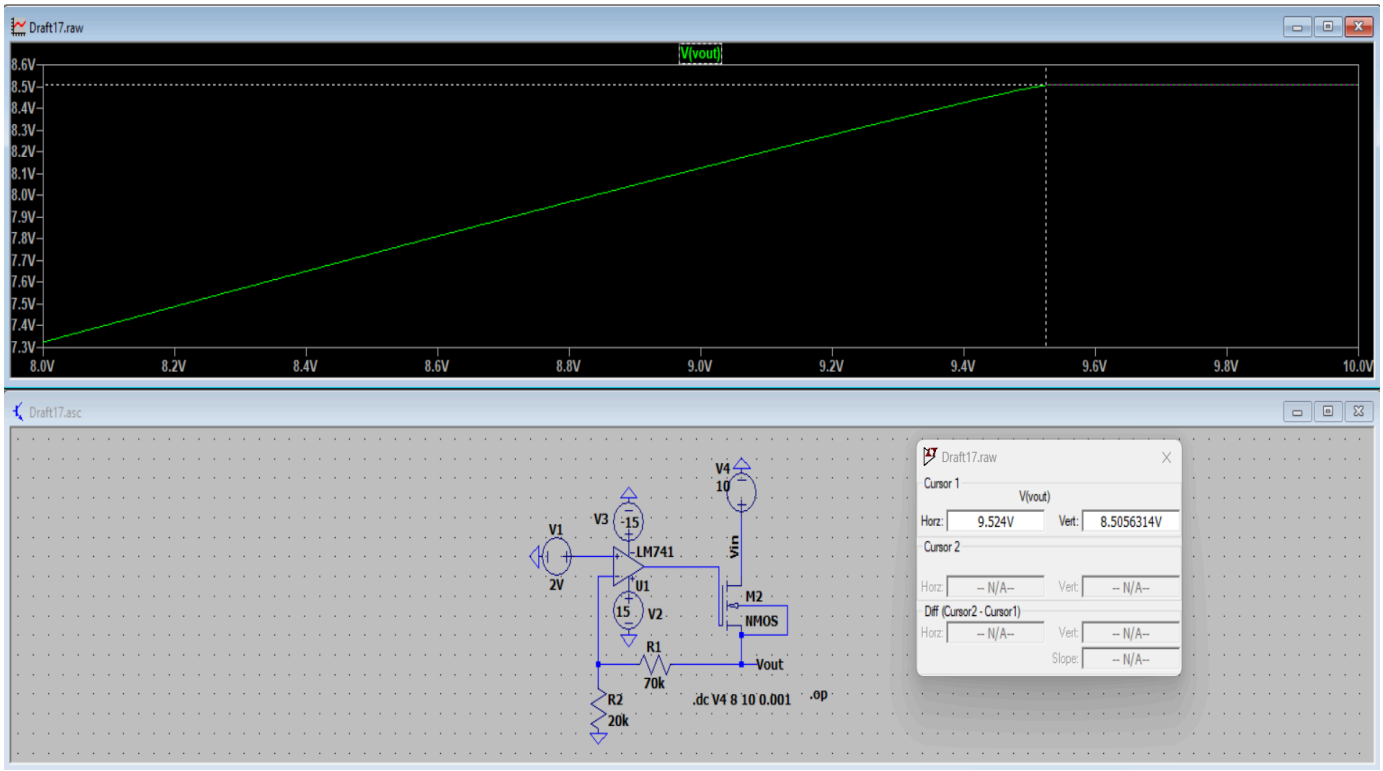


nMOS LDO working;

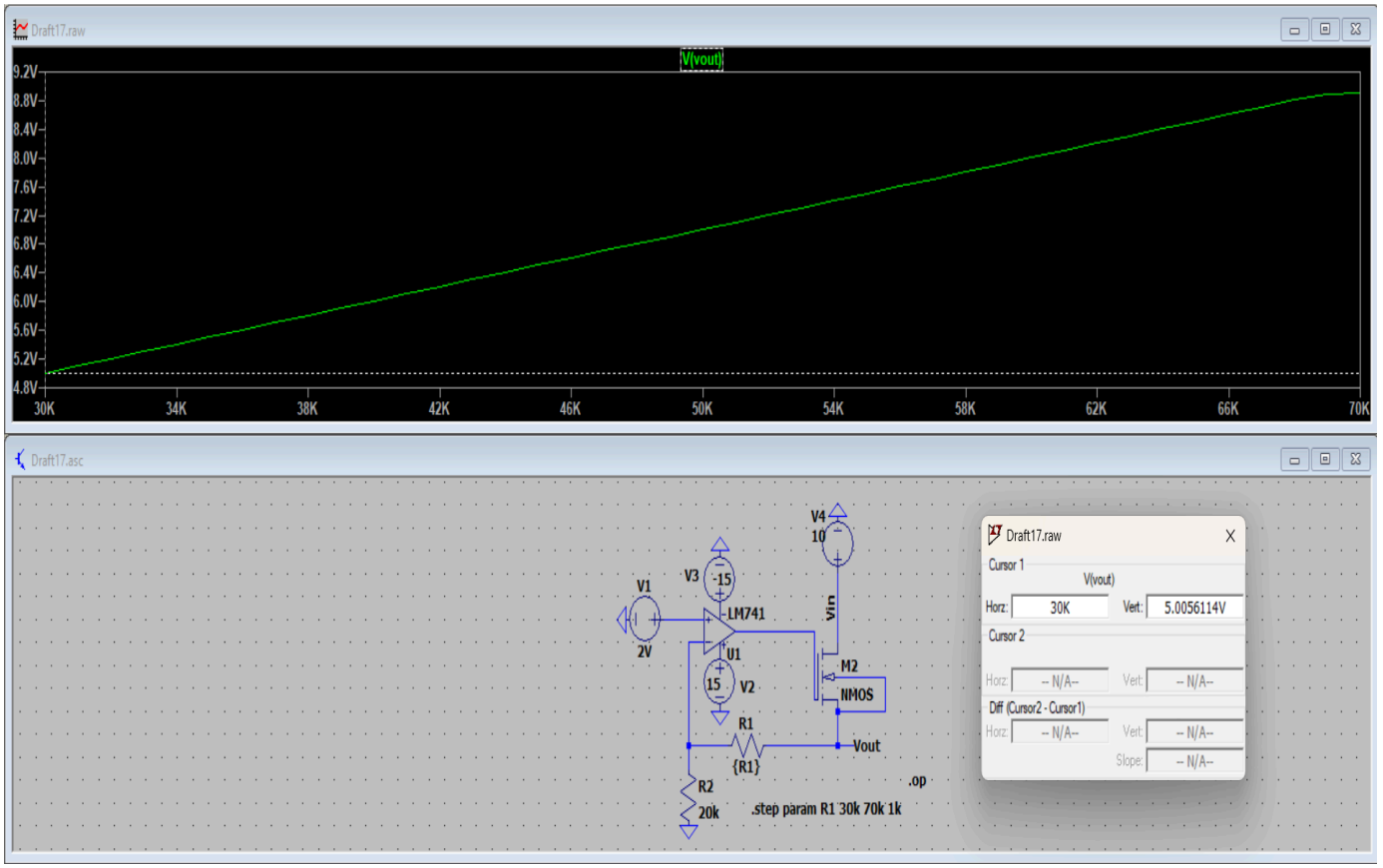
Case-2 nMOS



The value of Vmin(input) for output of 5V , we used DC sweeping of the voltage V4 labelled in the circuit and found that the minimum value of input is 5.585V as if we increase the voltage the output is constant at 5V.



Similarly, we again used DC sweep to calculate the Vmin for output at 9V and we found that to be 9.524V.



We vary the value of resistor R1 across a range determined by the calculated formula:

The specific values of R1 are adjusted based on the desired output voltage, following a calculated relationship. For instance, R1 is set to 30k ohms to achieve a 5V output and 70k ohms for a 9V output, with a fixed reference voltage Vref of 2V.