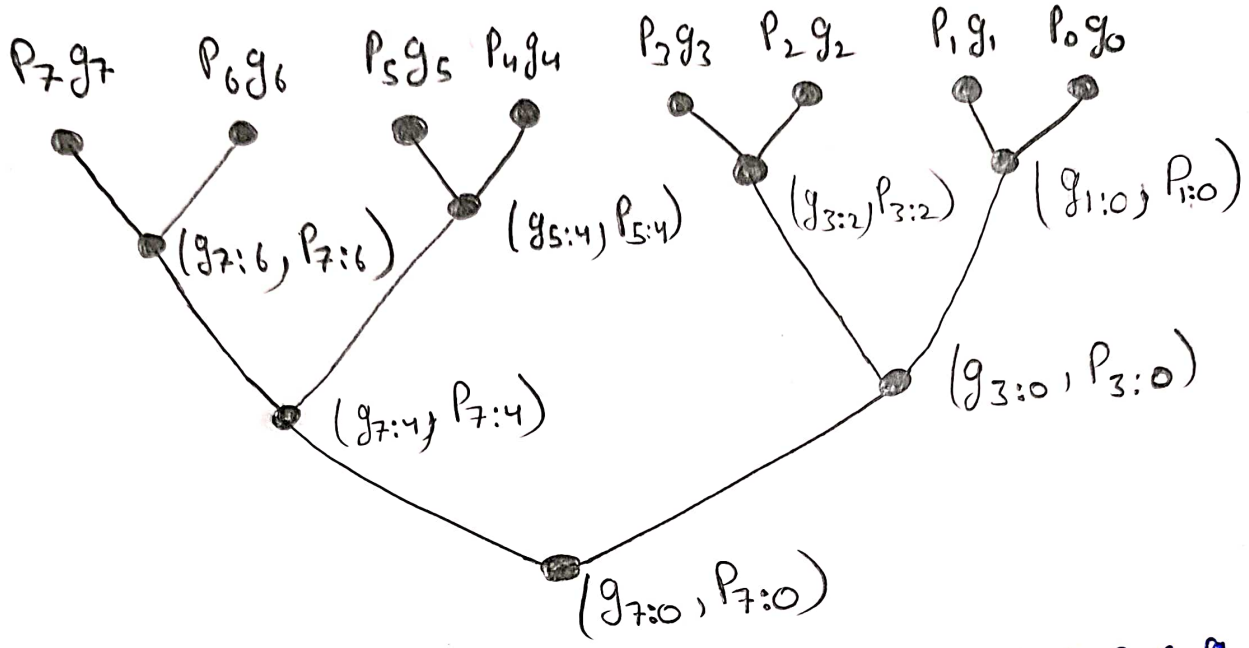
Assignment → 03

EE22BTECH11025

(1)

a)



b) $$C_{out} = g_7 + P_7g_6 + P_7P_6g_5 + P_7P_6P_5g_4 + P_7P_6P_5P_4g_3$$
$$+ P_7P_6P_5P_4P_3g_2 + P_7P_6P_5P_4P_3P_2g_1 + P_7P_6P_5P_4P_3P_2P_1g_0$$
$$+ P_7P_6P_5P_4P_3P_2P_1P_0C_{in}$$

$$C_{out} = (g_{7:0}, P_{7:0}C_{in})$$

c) Yes, we can use this technique of carry generate & carry propagate for base 10 number addition

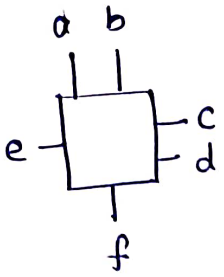
$$g_i = \begin{cases} 1, & a_i + b_i \geq 10 \\ 0, & \text{otherwise} \end{cases} \rightarrow \text{In case of carry generate}$$

$$P_i = \begin{cases} 1, & a_i + b_i = 9 \\ 0, & a_i + b_i \neq 0 \end{cases} \rightarrow \text{In case of carry propagate}$$

The operation '$\circ$' will remain same as in binary

$$(g_1, P_1) \circ (g_0, P_0) \equiv (g_1 + g_0P_1, P_1P_0)$$

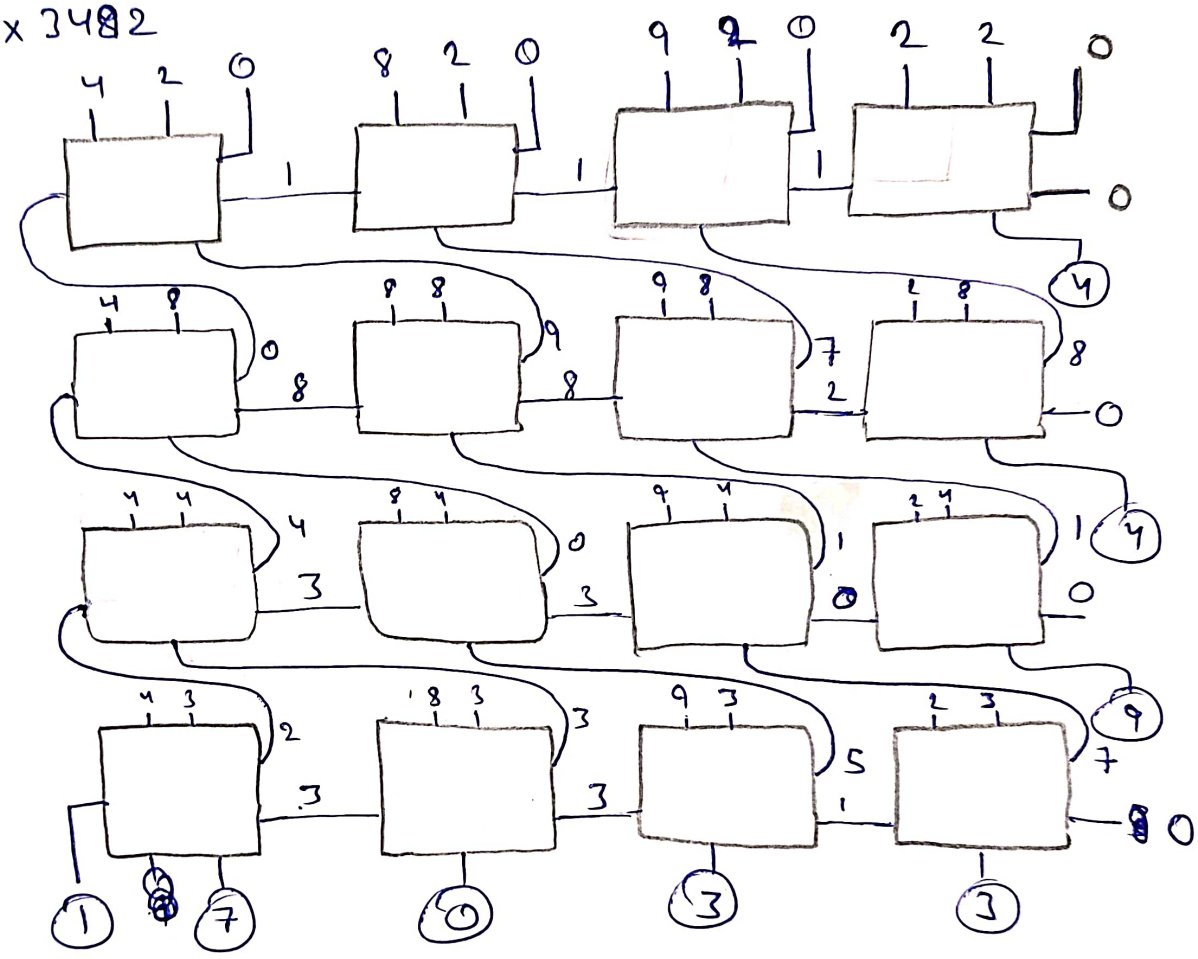
(2)



$a.b + c + d = e.B + f$

(B being the radix here it is 10)

For 4892 × 3482



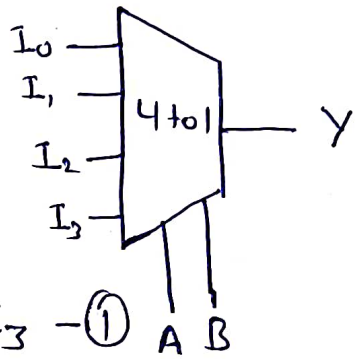
$\therefore$ **4892 × 3482 = 17033944**

(3)

We ~~can~~ have 2 variables & 1 variable with its complement, we can implement any 3 variable function using a 4x1 MUX.

$\Sigma(A,B,C)$	A	B	C
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

A	B	Select line
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3



$$Y = A'B'I_0 + A'BI_1 + AB'I_2 + ABI_3 \quad -(1)$$

For MUX to be complete

Any 3 variable function can be implemented by Y

As any 3 variable function can be represented in the form of SOP notation

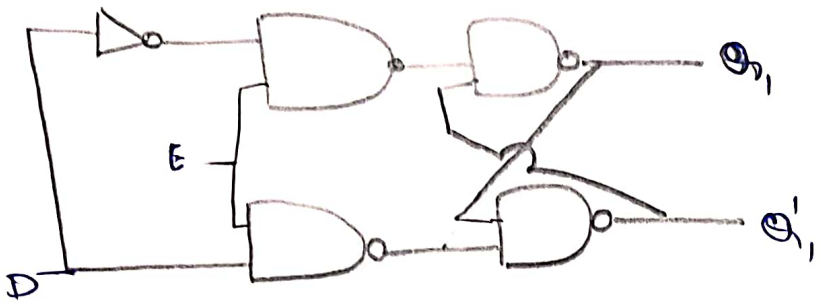
∴ by ~~ca~~ changing I_0, I_1, I_2, I_3 as either C or C'

we can have any SOP notation in equation -(1),

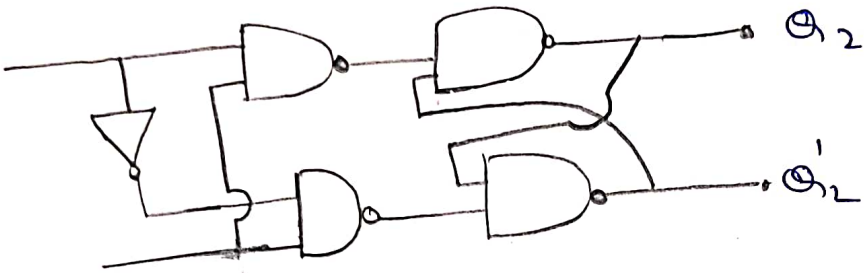
Thus, we can implement any binary function of 3 variable.

(4)

a)

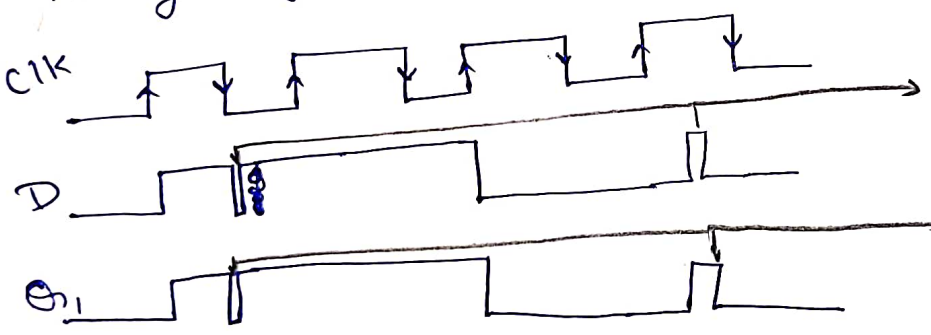


D - Latch



D - FF

a) Timing diagram

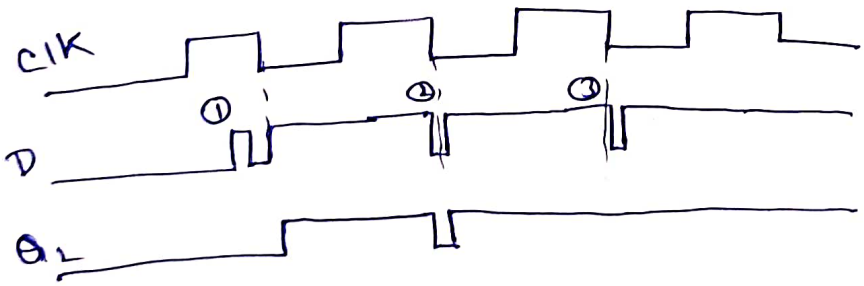


spurious signal

spurious signal in D-Latch

No effect in D-FF

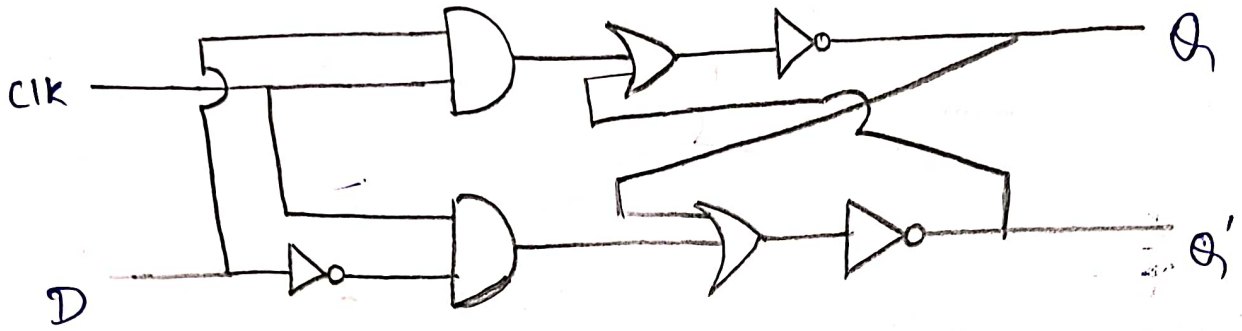
b)



→ spurious output may occur in D-FF, if spurious signal is very close to -ve edge of FlipFlop.

In case of ①, ③ where spurious signal is either before or after the -ve edge no change will occur.

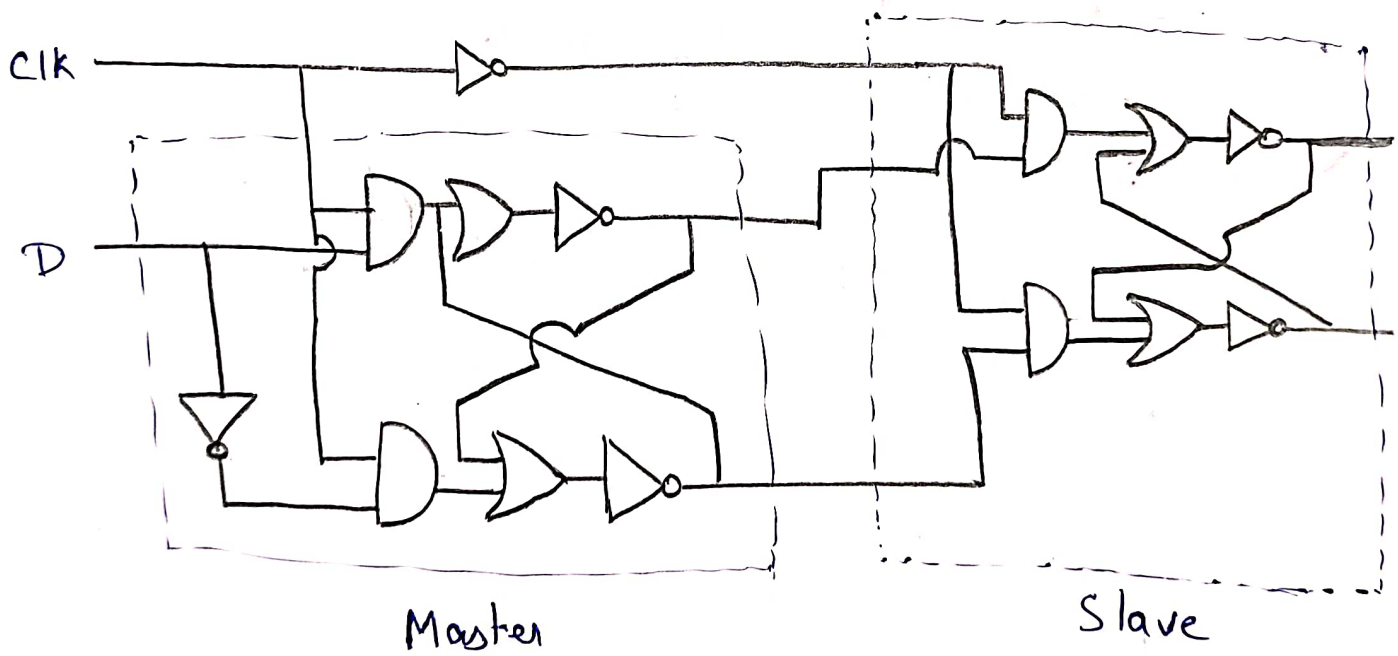
⑤ A D-Latch is as follows,



Maximum Delay time = $3t_{inv} + 2t_{and} + 2t_{or}$ -①

Minimum Delay time = $t_{inv} + t_{and} + t_{or}$ -②

D - FlipFlop is as follows,



Delay time $= 6t_{inv} + 4t_{and} + 4t_{or}$ - (3)

As we can replace 'or' gate with 'and' gate

$\therefore$ Maximum delay for D-Latch $= 3t_{inv} + 4t_{and}$ {from (1)}

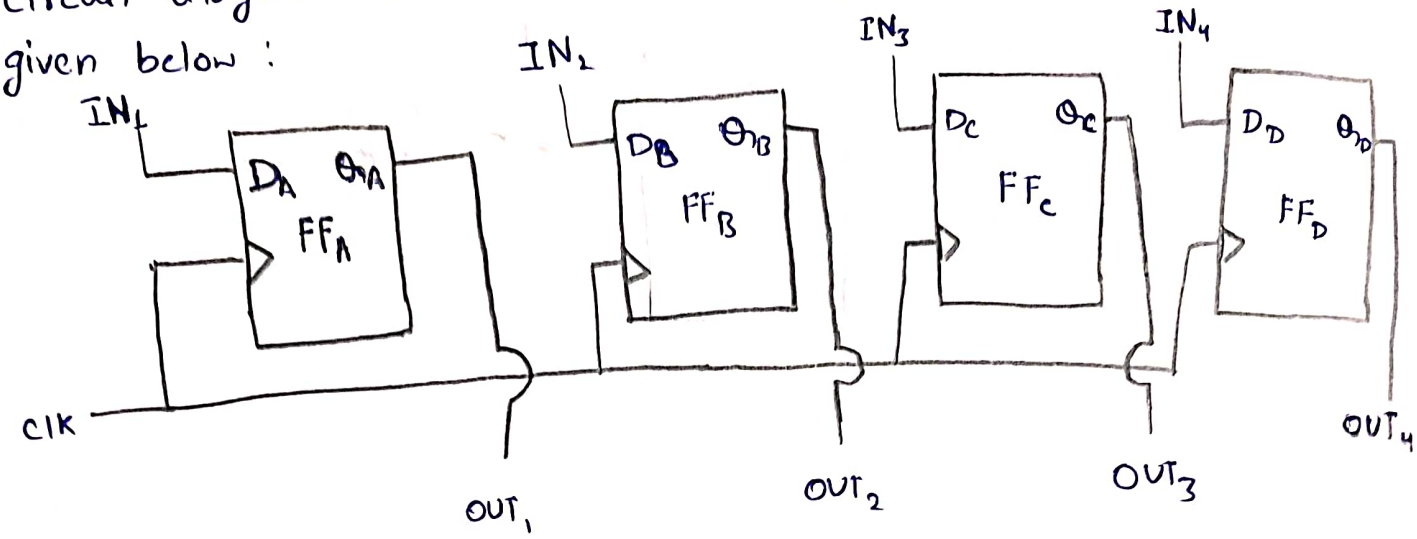
Minimum delay for D-Latch $= 2t_{inv} + 2t_{and}$ {from (2)}

Delay time for D-FF $= 6t_{inv} + 8t_{and}$ - {from (3)}

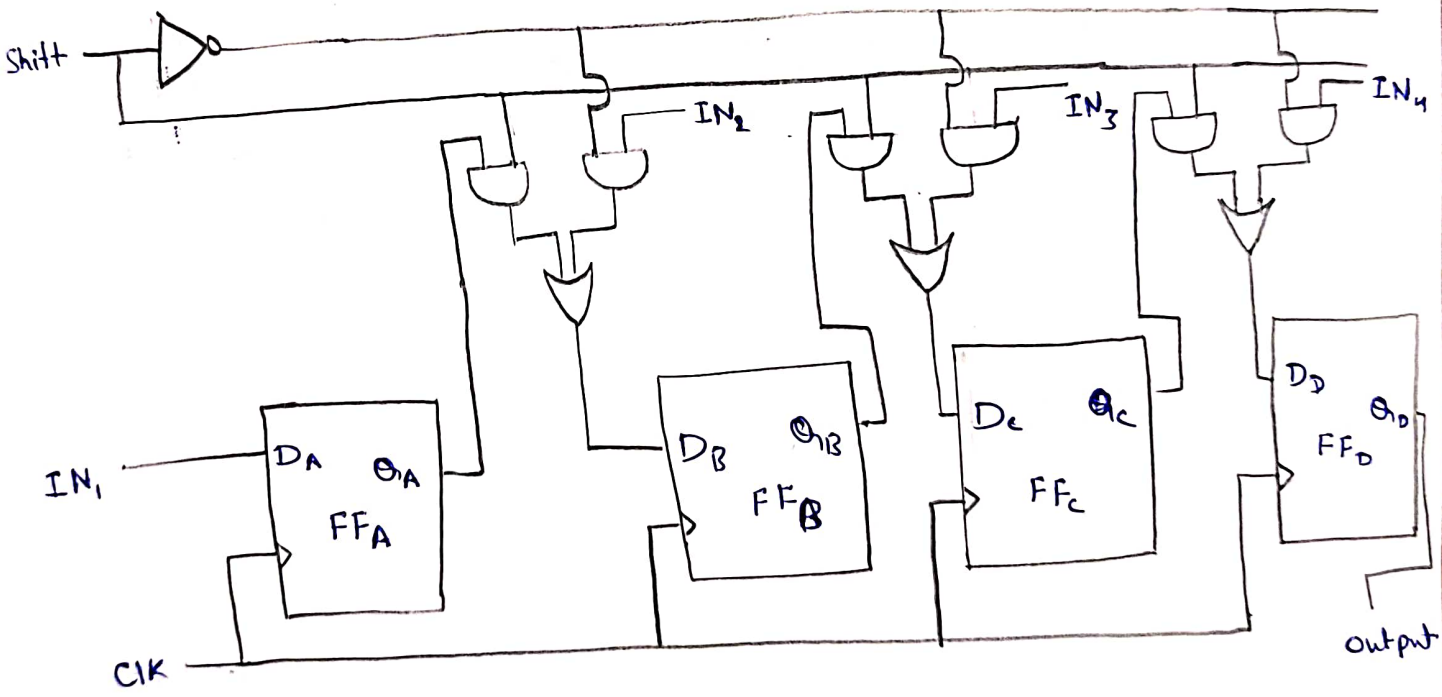
Now depending upon which one is greater between t_{or} and t_{and}, we can tell min & max. delay incurred for the two.

(6)

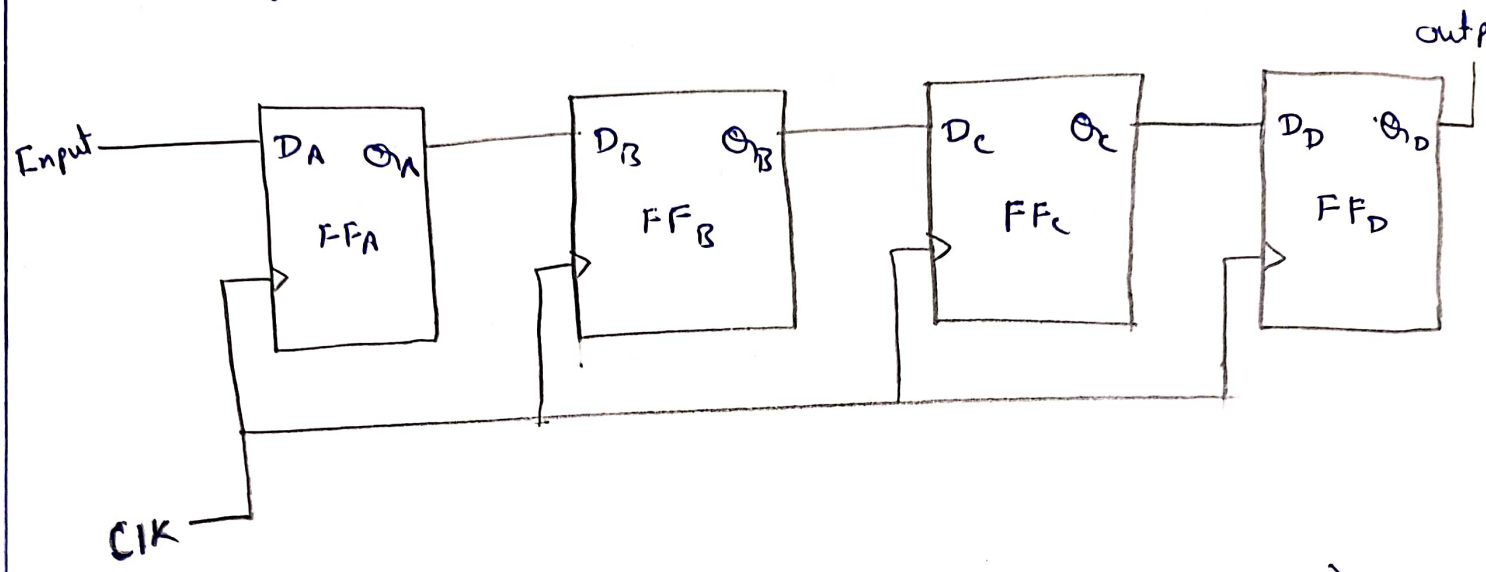
a) Circuit diagram for PIPO (Parallel input & parallel output) is given below :



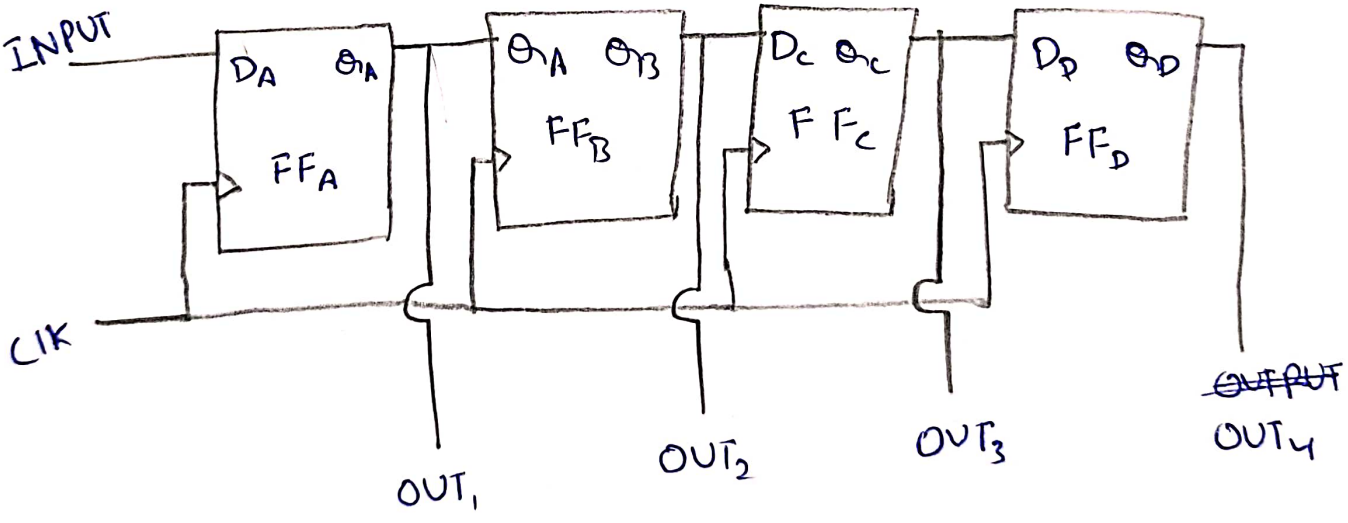
c) ~~Circuit~~ Circuit diagram for PISO (Parallel - input & serial out)



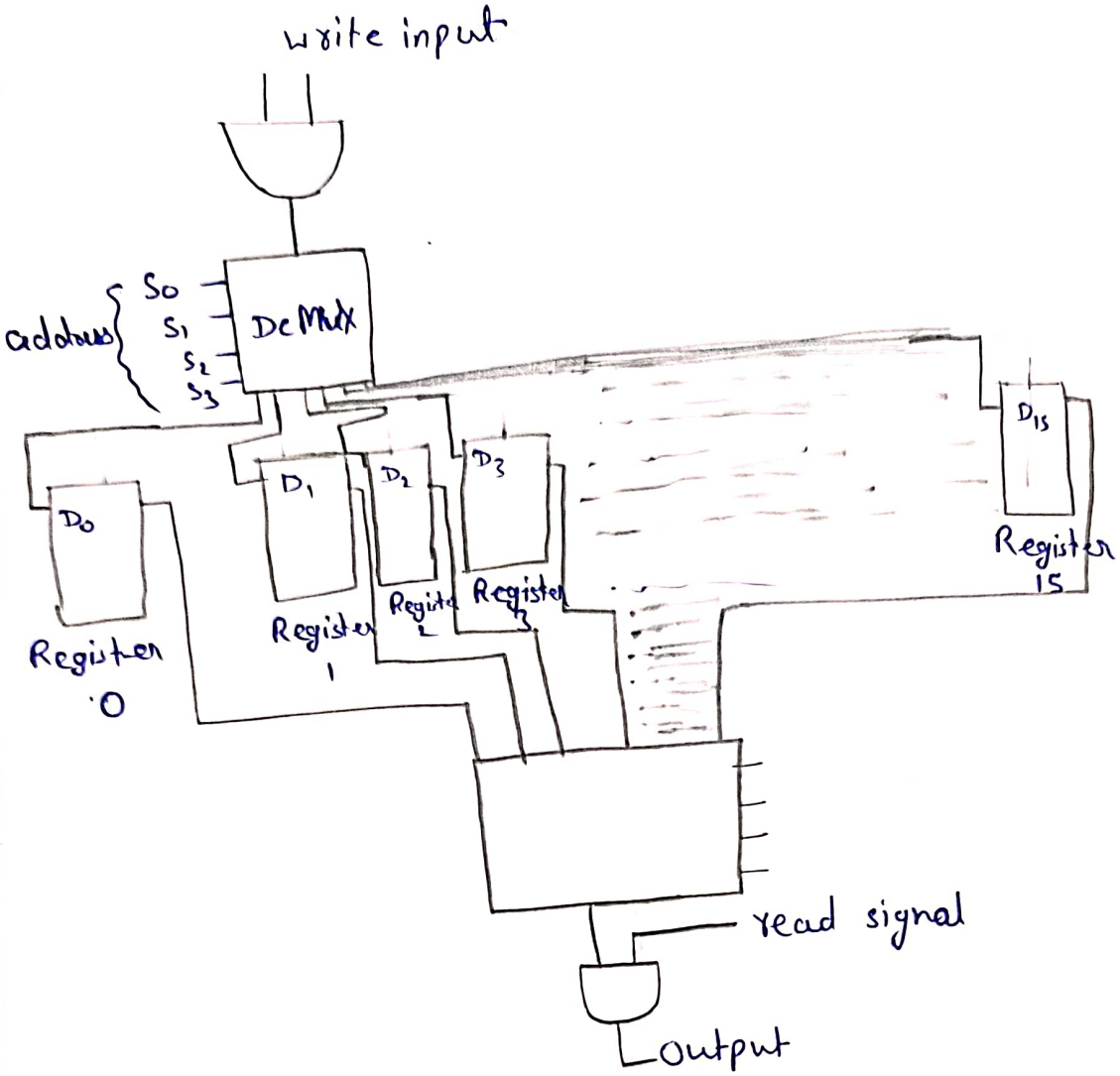
a) Circuit diagram for SISO (serial input & serial output)



b) Circuit diagram for SIPO (serial-input & parallel out)



(e)



For adding another control signal 'Read 1', another set of address lines add to 1, we have to use two multiplexer in addition to previous circuits to read two registers simultaneously