

EXPERIMENT-10,11

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Problem 1:

Aim:

Do the following with CMOS and TTL inverter

- To investigate the relationship between the input and output voltages of an inverter.
- To determine the range of input voltages over which the output voltage of an inverter will remain stable.
- To determine the power consumption of an inverter when driven by a square wave signal.

Material Required:

IC4069(CMOS), IC7404(TTL), breadboard, DC supply bench, DSO, function generator.

Theory:

CMOS Inverter(IC4069)

The complementary metal-oxide-semiconductor CMOS inverter consists of two transistors, one n-channel and one p-channel, that are connected in a complementary fashion. When the input voltage is high, the n-channel transistor turns on, and the p-channel transistor turns off. High output voltage allows current to flow from the power supply to the output. When the input voltage is low, the p-channel transistor turns on, and the n-channel transistor turns off. Low output voltage allows current to flow from the ground to the output.

TTL (IC7404) Inverter

The TTL inverter consists of several transistors connected in a complex circuit. When there is a high input voltage, the transistors are biased to allow current to flow from the power supply to the output; this causes the output voltage to be high. When the input voltage is low, the transistors are biased to allow current to flow from the ground to the output. This causes the output voltage to be low.

The gain of an inverter is given by the ratio of change in o/p Voltage (ΔV_{out}) to change in i/p Voltage (ΔV_{in}) ,

$$A = \frac{\Delta V_{out}}{\Delta V_{in}}$$

Transfer Characteristics

The transfer characteristics of an inverter are a plot of the output voltage versus the input voltage. The transfer characteristics of a CMOS inverter are typically a steep curve with a high gain. The transfer characteristics of a TTL inverter are typically a more gradual curve with a lower gain.

Noise Margin

An inverter's noise margin measures its ability to tolerate noise on the input signal. The noise margin is the difference between o/p voltage and i/p voltage. There are two types of noise margins: High-level noise margin (NM_H) and Low-level noise margin (NM_L).

$$NM_H = V_{OHmin} - V_{IH}$$

$$NM_L = V_{IL} - V_{OLmax}$$

- V_{OHmin} is the minimum high-level output voltage.
- V_{OLmax} is the minimum high-level output voltage.
- V_{IH} is the minimum high-level input voltage.
- V_{IL} is the maximum low-level input voltage.

Frequency Range

To determine the operational frequency range of the inverter, a square wave with a 50% duty cycle is applied to the input. The frequency is gradually increased until distortion occurs in the output waveform. The maximum fundamental frequency at which the inverter is considered operational is $V_{OHmax} \sim 90\%$ of V_{dd} and V_{OLmin} is 10% above 0.

Dynamic Power Dissipation

The dynamic power dissipation of an inverter is the power that is consumed by the inverter when it is switching. The dynamic power dissipation is proportional to the frequency of the input signal and the square of the output voltage swing. A load capacitor of 100 nF is added to the output. The dynamic power dissipation is measured at different frequencies, specifically at $f_{max} / 20, f_{max} / 10, f_{max} / 5,$

$$P_{dynamic} = \frac{1}{2} C_L (V_{dd})^2 f$$

Procedure:

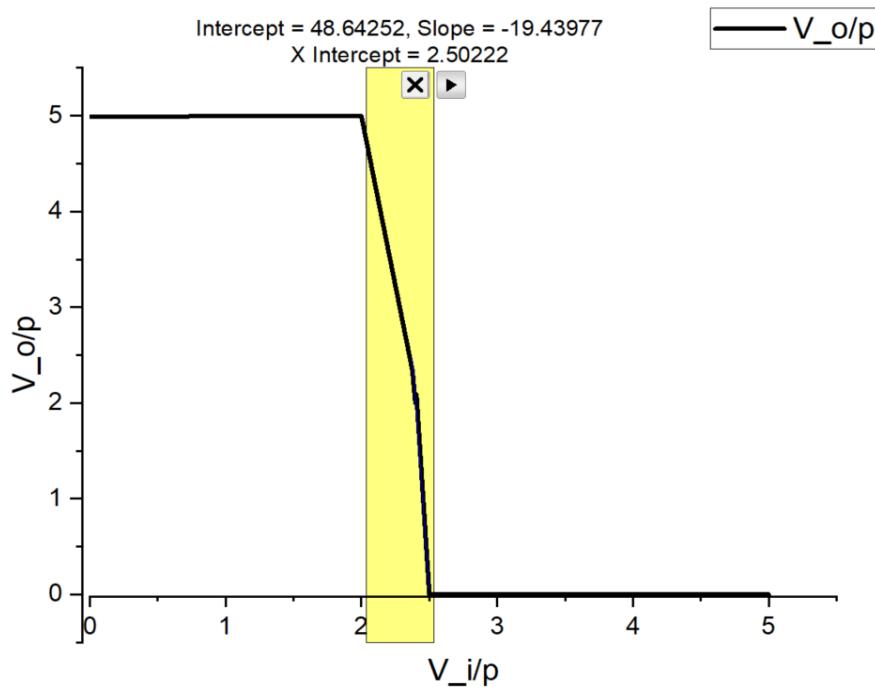
- Vary the input from 0 V to supply Voltage (V CC in case of TTL, V DD in case of CMOS) and measure the output voltage. Draw the transfer characteristics of the inverter and calculate the gain. Extract the noise margin of the inverter.
- Feed a square wave (50% duty cycle) into the input of the inverter with voltage levels 0 to V_{dd} . Plot the input and inverted output on the DSO. Now, increase the frequency. You will start seeing distortion in the output. The maximum fundamental frequency where the inverter is said to be operational is where the $V_{OH_max} \sim 90\%$ of V_{dd} and V_{OH_min} is 10% above 0.
- Place a load capacitor of 100 nF at the output. Find the dynamic power dissipation across the load capacitor at $f_{max} / 20, f_{max} / 10, f_{max} / 5.$

Observations:

For Part(A):

IC4069:

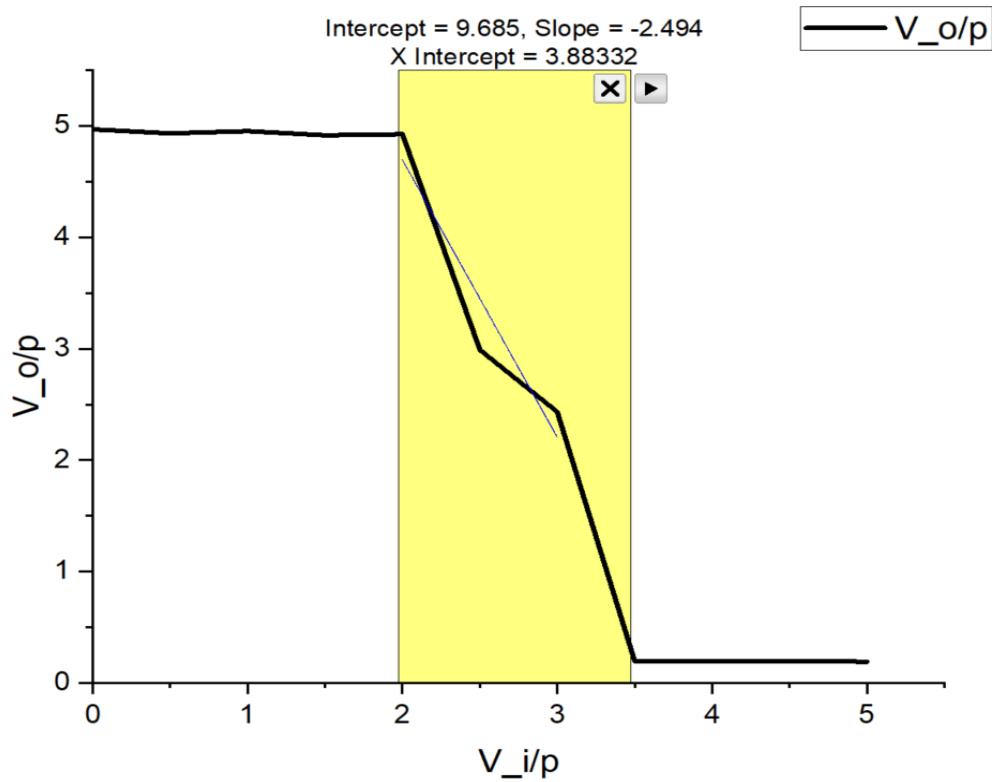
V_i/p	V_o/p
0	4.989
1	4.996
1.5	4.996
2	4.996
2.375	2.342
2.398	2.003
2.405	2.087
2.5	2E-5
4	2E-5
4.5	2E-5
5	2E-5



Gain is -19.439

IC7404:

V_i/p	V_o/p
0	4.971
0.5	4.935
1	4.955
1.5	4.918
2	4.927
2.5	2.99
3	2.433
3.5	0.1927
4	0.1909
4.5	0.194
5	0.1877



Gain is -2.494

Calculation for Gain:

- Gain for IC4069:

$$A = -19.43$$

- Gain for IC7404:

$$A = -2.494$$

Calculation for noise margin:

- Noise margin for IC4069 Case 1:

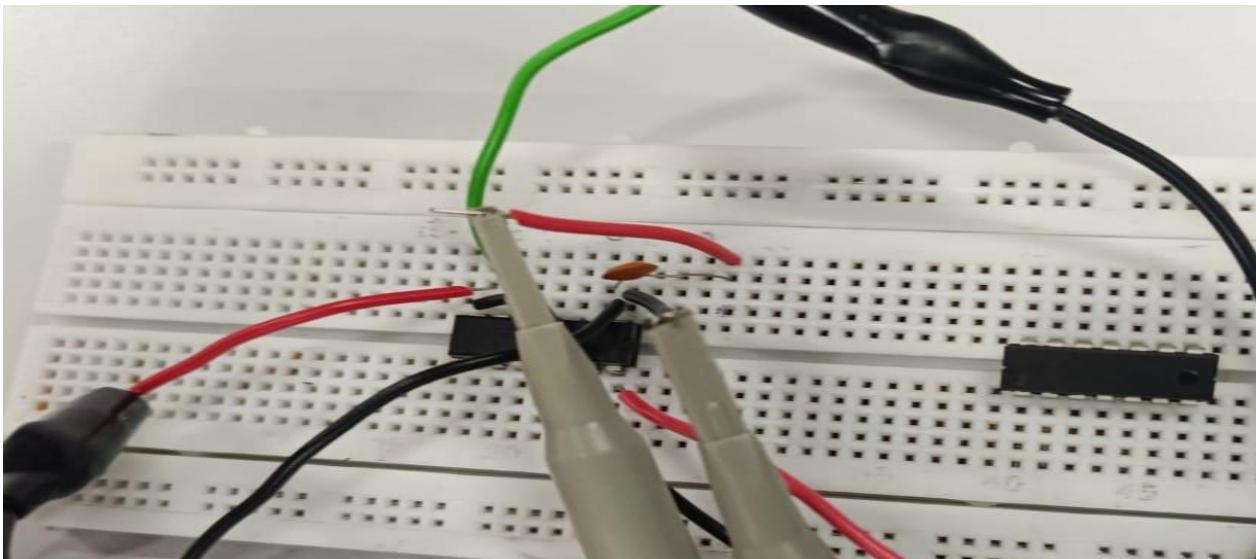
$$NM_H = V_{OHmin} - V_{IH} = 2.003 - 2.405 = -0.402$$

$$NM_L = V_{IL} - V_{OLmax} = 2.5 - 0.00002 = 2.49998$$

- Noise margin for IC7404:

$$NM_H = V_{OHmin} - V_{IH} = 2.433 - 3.5 = -1.067$$

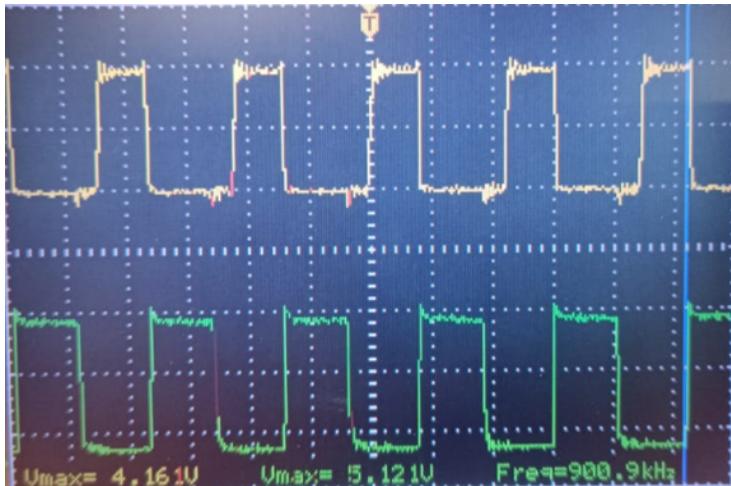
$$NM_L = V_{IL} - V_{OLmax} = 3 - 0.194 = 2.806$$



For Part(B):

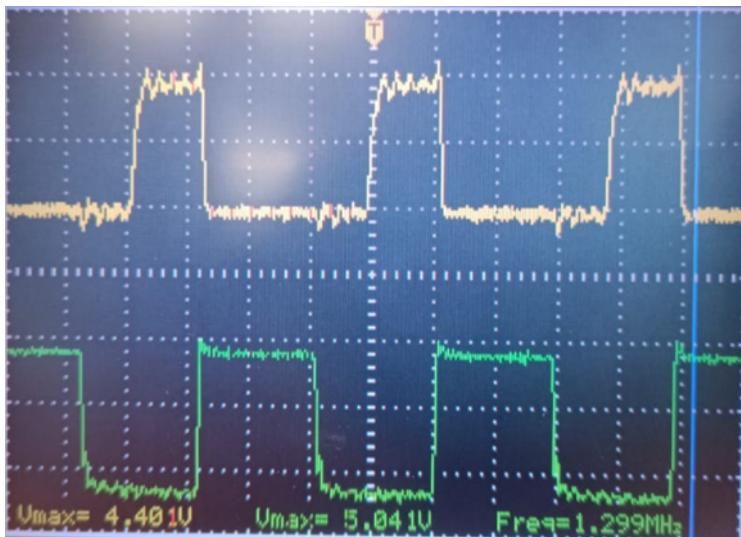
CMOS:

The input and output signals from the experimental readings are as follows:



$$V_{in} = 5.121V$$

$$V_{out} = 4.16V$$



$$V_{in} = 5.041V$$

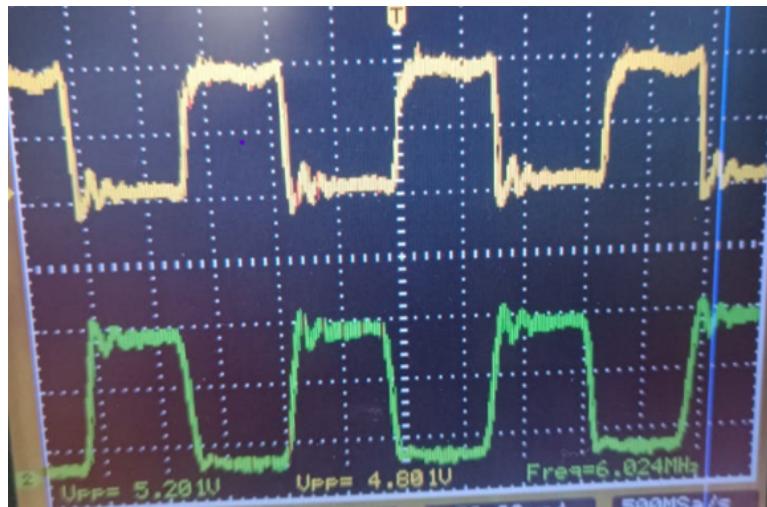
$$V_{out} = 4.401V$$

This is the frequency where the signal gets distorted

$$F = 1.299MHz$$

$$V_{max} \text{ of o/p} = 90\% \text{ of } V_{max} \text{ of o/p} = 0.9 * 5.041 = 4.539 V$$

TTL:



$$V_{in} = 5.201V$$

$$V_{out} = 4.801V$$

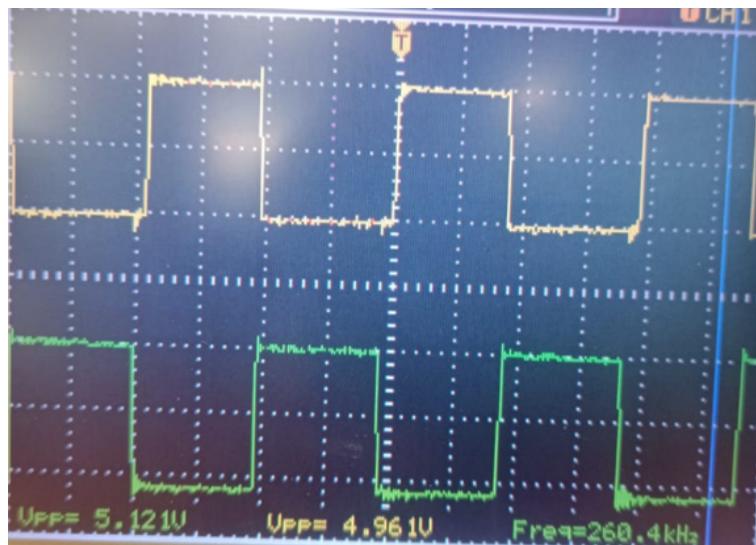
This is the frequency where the signal gets distorted

$$F = 6.024\text{MHz}$$

$$V_{max} \text{ of o/p} = 90\% \text{ of } V_{max} \text{ of o/p} = 0.9 * 5.201 = 4.7 \text{ V}$$

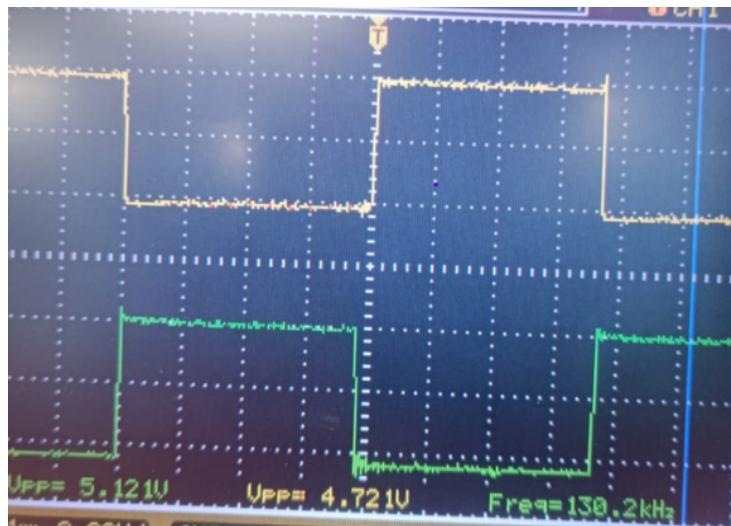
For Part(C):

CMOS:



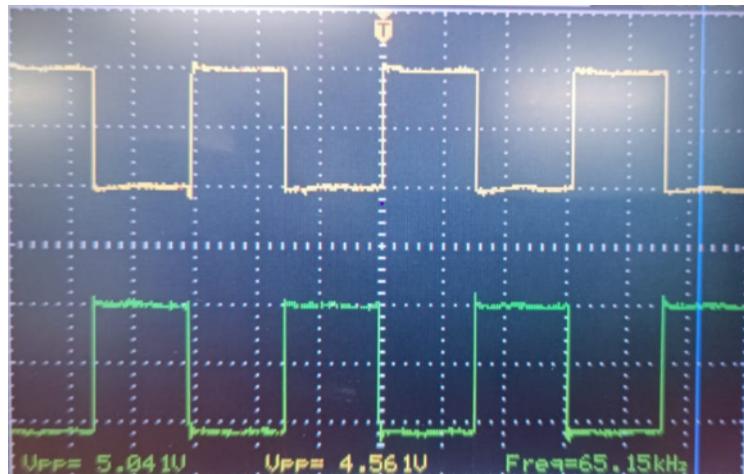
$$\frac{F_{max}}{5} = \frac{1.3MHz}{5} = 260.4KHz$$

$$P_{dynamic} = \frac{1}{2} (100nF)(5V)^2 (260.4KHz) = 0.3255 W$$



$$\frac{F_{max}}{10} = \frac{1.3MHz}{10} = 130.2KHz$$

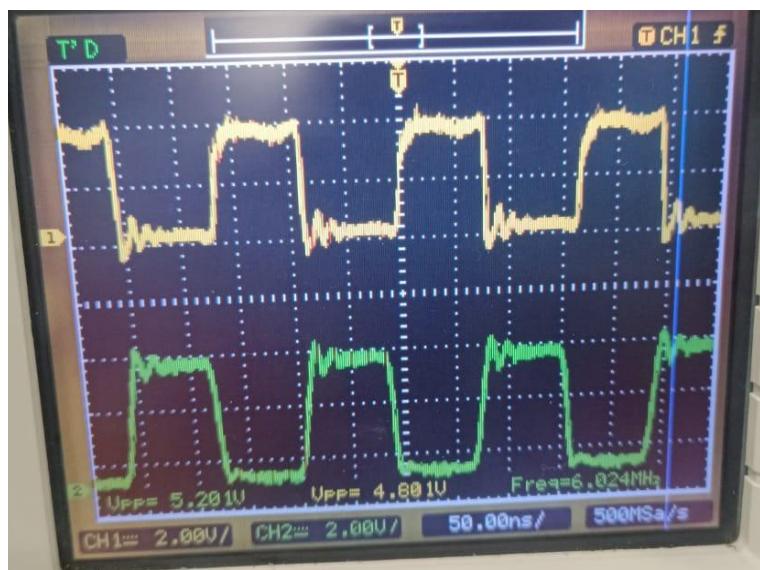
$$P_{dynamic} = \frac{1}{2} (100nF)(5V)^2 (130.2KHz) = 0.16275 W$$



$$\frac{F_{max}}{20} = \frac{1.3MHz}{20} = 65.15KHz$$

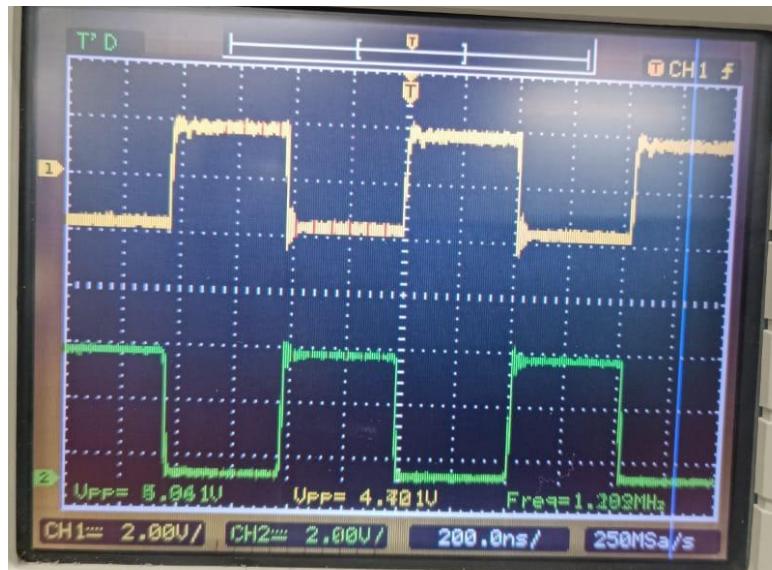
$$P_{dynamic} = \frac{1}{2} (100nF)(5V)^2 (65.15KHz) = 0.081375 W$$

TTL:



$$\frac{F_{max}}{5} = 6.024 \text{ MHz}$$

$$P_{dynamic} = \frac{1}{2} (100nF)(5V)^2 (6.024 \text{ MHz}) = 7.53 \text{ W}$$



$$\frac{F_{max}}{10} = 1.299 \text{ MHz}$$

$$P_{dynamic} = \frac{1}{2} (100nF)(5V)^2 (1.299 \text{ MHz}) = 1.623 \text{ W}$$



$$\frac{F_{max}}{20} = 599.5 \text{ KHz}$$

$$P_{dynamic} = \frac{1}{2} (100nF)(5V)^2 (599.5 \text{ KHz}) = 0.74 \text{ W}$$

Problem 2:

Aim:

To Construct a ring oscillator using CMOS and TTL inverter

Material Required:

IC4069(CMOS), IC7404(TTL), breadboard, DC supply bench, DSO, function generator.

Theory:

In a ring oscillator, a series of inverters are connected in a loop to form a closed feedback path, resulting in a sustained oscillation of the phase around the loop. The number of inverters in the loop is odd, ensuring the total phase shift is 360 degrees. The frequency of the oscillation is dependent on the propagation delay of the inverters

The propagation delay is the time it takes for a signal to propagate through an inverter. The rise time is when the output voltage rises from 10% to 90% of its final value. The fall time is when the output voltage falls from 90% to 10% of its final value.

$$t_r = t_f = \frac{1}{3.3nf}$$

The propagation delay increases as the supply voltage decreases. This is because the transistors in the inverter operate slower at lower voltages. The minimum supply voltage is the voltage at which the oscillator stops working. The transistors cannot switch on and off properly at lower voltages.

$$t_{pd} = \frac{T_{osc}}{n} = \frac{1}{2nf}$$

T_{osc} is the period of oscillation,
n is the number of inverters

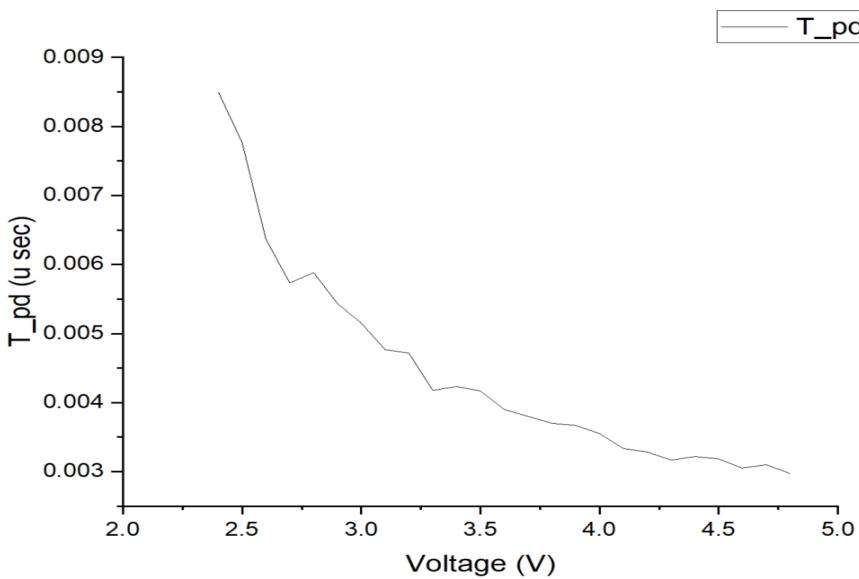
Procedure:

- Cascade an odd number of inverters (n = 3 and 5) and loop back from last to first (with V_{dd}). Watch them oscillating.
- From the oscillation frequency, find out the propagation delay, rise time, and fall time of the inverter and compare it with the datasheet.
- Repeat the above measurement for successively reduced supply voltages (in steps of 0.1 V_{dd} example, $V_{dd} - 0.1$, $V_{dd} - 0.2$ etc.). Plot the propagation delay vs supply voltage. What is the lowest supply voltage for which you can observe the ringing of the oscillator?

Observations:

For n=3, IC4069, the

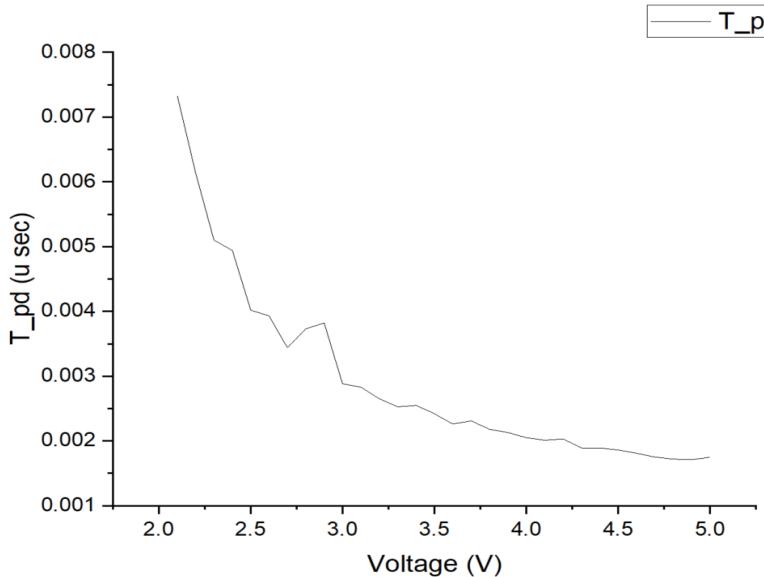
T_rise n sec	T_fall n sec	Freq MHz	Voltage V	T_pd u sec
0.00515	0.00515	19.61	2.4	0.0085
0.00471	0.00471	21.46	2.5	0.00777
0.00386	0.00386	26.18	2.6	0.00637
0.00347	0.00347	29.07	2.7	0.00573
0.00357	0.00357	28.33	2.8	0.00588
0.00329	0.00329	30.67	2.9	0.00543
0.00312	0.00312	32.36	3	0.00515
0.00289	0.00289	34.97	3.1	0.00477
0.00286	0.00286	35.34	3.2	0.00472
0.00253	0.00253	39.91	3.3	0.00418
0.00257	0.00257	39.37	3.4	0.00423
0.00253	0.00253	40	3.5	0.00417
0.00236	0.00236	42.74	3.6	0.0039
0.0023	0.0023	43.86	3.7	0.0038
0.00224	0.00224	45.05	3.8	0.0037
0.00222	0.00222	45.45	3.9	0.00367
0.00215	0.00215	46.95	4	0.00355
0.00202	0.00202	50	4.1	0.00333
0.00199	0.00199	50.76	4.2	0.00328
0.00192	0.00192	52.65	4.3	0.00317
0.00195	0.00195	51.81	4.4	0.00322
0.00193	0.00193	52.36	4.5	0.00318
0.00185	0.00185	54.64	4.6	0.00305
0.00188	0.00188	53.76	4.7	0.0031
0.0018	0.0018	56.1	4.8	0.00297



Lowest supply voltage for which you can observe the ringing of the Oscillator is 2.4V

For n=5, IC4069, the

T_rise n sec	T_fall n sec	Freq MHz	Voltage V	T_pd u sec
0.00444	0.00444	13.64	2.1	0.00733
0.00372	0.00372	16.29	2.2	0.00614
0.00309	0.00309	19.61	2.3	0.0051
0.00299	0.00299	20.24	2.4	0.00494
0.00244	0.00244	24.88	2.5	0.00402
0.00238	0.00238	25.45	2.6	0.00393
0.00208	0.00208	29.07	2.7	0.00344
0.00226	0.00226	26.8	2.8	0.00373
0.00231	0.00231	26.18	2.9	0.00382
0.00175	0.00175	34.7	3	0.00288
0.00171	0.00171	35.34	3.1	0.00283
0.00161	0.00161	37.75	3.2	0.00265
0.00153	0.00153	39.6	3.3	0.00253
0.00155	0.00155	39.22	3.4	0.00255
0.00147	0.00147	41.32	3.5	0.00242
0.00137	0.00137	44.25	3.6	0.00226
0.0014	0.0014	43.29	3.7	0.00231
0.00132	0.00132	45.89	3.8	0.00218
0.00129	0.00129	46.95	3.9	0.00213
0.00124	0.00124	48.78	4	0.00205
0.00122	0.00122	49.75	4.1	0.00201
0.00123	0.00123	49.26	4.2	0.00203
0.00115	0.00115	52.9	4.3	0.00189
0.00115	0.00115	52.9	4.4	0.00189
0.00113	0.00113	53.76	4.5	0.00186
0.0011	0.0011	55.25	4.6	0.00181
0.00106	0.00106	57.15	4.7	0.00175
0.00104	0.00104	58.14	4.8	0.00172
0.00104	0.00104	58.48	4.9	0.00171
0.00106	0.00106	57.2	5	0.00175

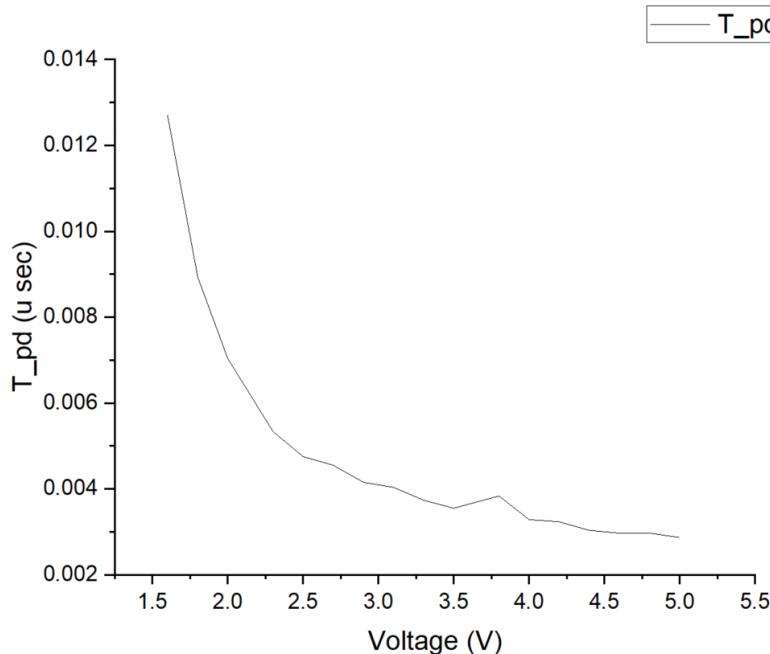


Lowest supply voltage for which you can observe the ringing of the

Oscillator is 2.1V

For n=3, IC7404

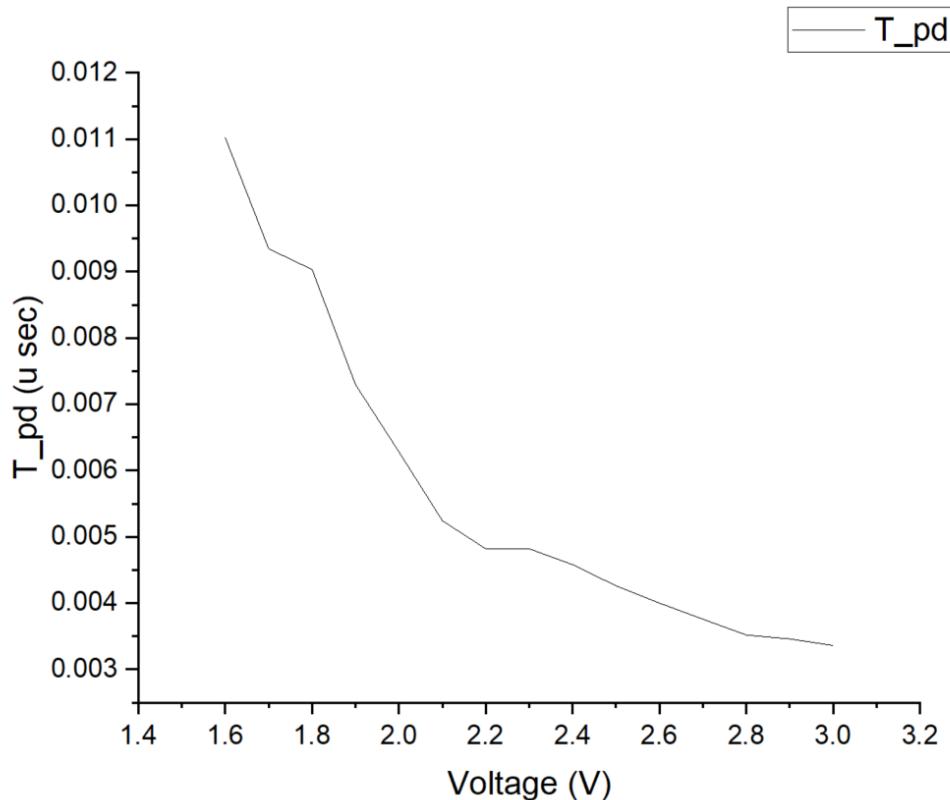
T_rise n sec	T_fall n sec	Freq MHz	Voltage V	T_pd u sec
0.0077	0.0077	13.12	1.6	0.0127
0.00541	0.00541	18.66	1.8	0.00893
0.00426	0.00426	23.7	2	0.00703
0.00323	0.00323	31.25	2.3	0.00533
0.00288	0.00288	35.09	2.5	0.00475
0.00276	0.00276	36.63	2.7	0.00455
0.00252	0.00252	40.13	2.9	0.00415
0.00244	0.00244	41.32	3.1	0.00403
0.00226	0.00226	44.64	3.3	0.00373
0.00215	0.00215	46.95	3.5	0.00355
0.00232	0.00232	43.48	3.8	0.00383
0.00199	0.00199	50.76	4	0.00328
0.00196	0.00196	51.55	4.2	0.00323
0.00184	0.00184	54.95	4.4	0.00303
0.0018	0.0018	56.15	4.6	0.00297
0.0018	0.0018	56.14	4.8	0.00297
0.00174	0.00174	58.14	5	0.00287



Lowest supply voltage for which you can observe the ringing of the Oscillator is 1.6V

For n=5, IC7404

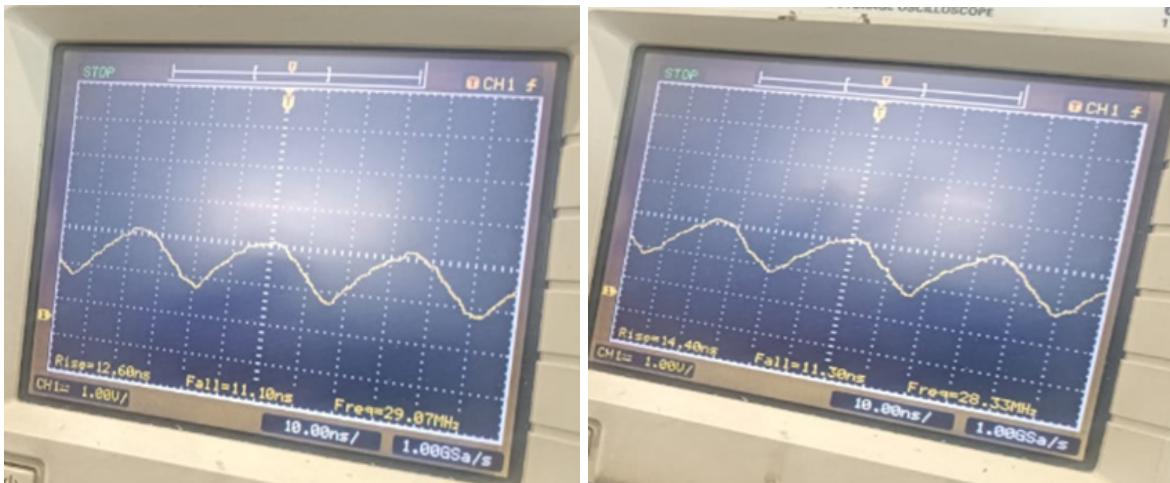
T_rise n sec	T_fall n sec	Freq MHz	Voltage V	T_pd u sec
0.00668	0.00668	9.07	1.6	0.01103
0.00566	0.00566	10.7	1.7	0.00935
0.00547	0.00547	11.07	1.8	0.00903
0.00442	0.00442	13.7	1.9	0.0073
0.00381	0.00381	15.92	2	0.00628
0.00318	0.00318	19.08	2.1	0.00524
0.00292	0.00292	20.75	2.2	0.00482
0.00292	0.00292	20.75	2.3	0.00482
0.00278	0.00278	21.83	2.4	0.00458
0.00258	0.00258	23.47	2.5	0.00426
0.00242	0.00242	25	2.6	0.004
0.00228	0.00228	26.6	2.7	0.00376
0.00213	0.00213	28.41	2.8	0.00352
0.0021	0.0021	28.9	2.9	0.00346
0.00204	0.00204	29.76	3	0.00336



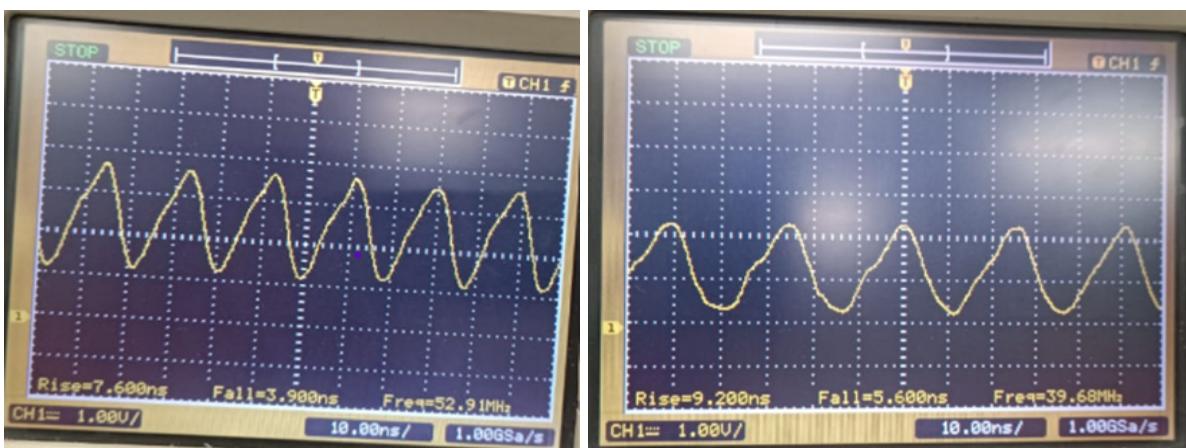
Lowest supply voltage for which you can observe the ringing of the Oscillator is 1.6V

Readings:

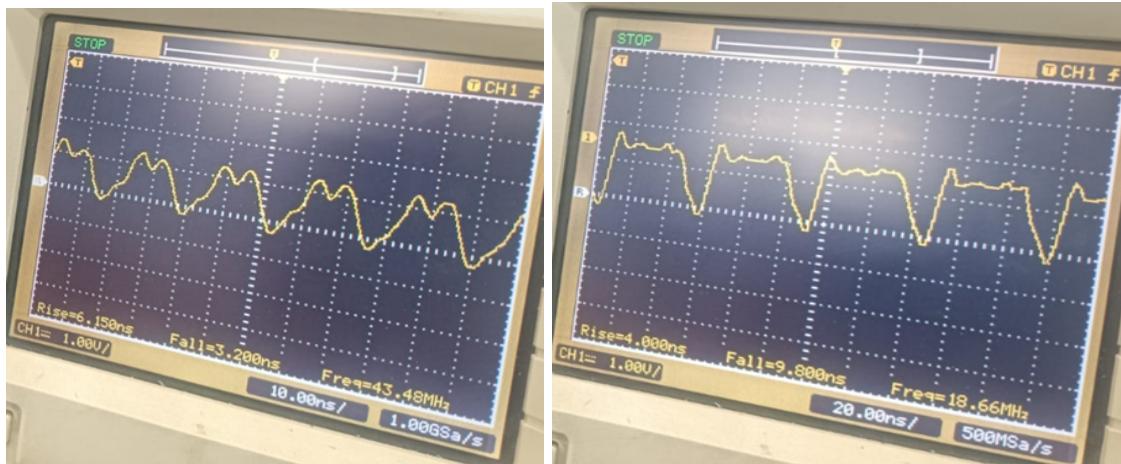
- n=3, IC4069:



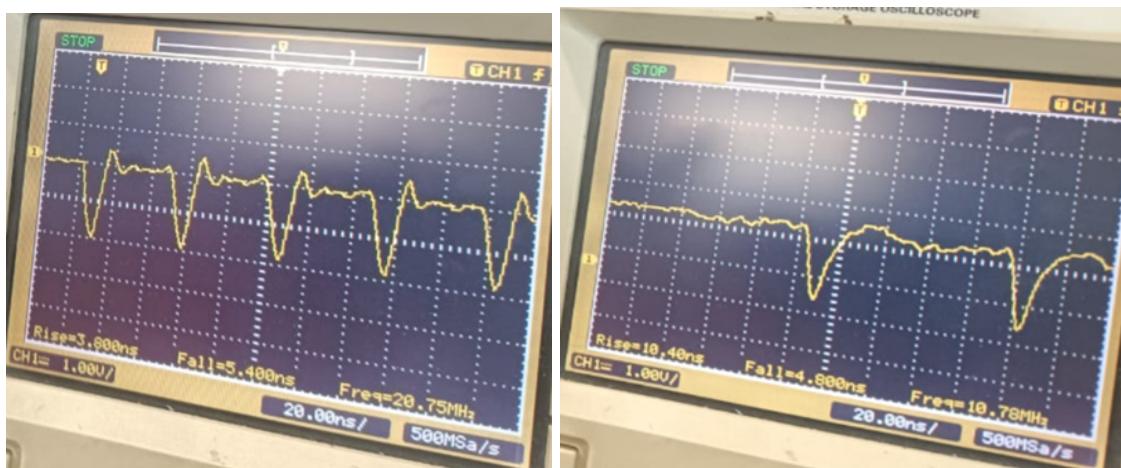
- n=5, IC4069:



- n=3, IC4069:



- n=5, IC4069:



Problem 3:

Aim:

To construct a 1-bit SRAM cell using CMOS inverters and to demonstrate its read and write operations.

Material Required:

Breadboard, CMOS Inverter(IC4069), MOSFET, DC supply, multimeter

Theory:

Static RAM (SRAM) is a type of random-access memory (RAM) that retains data as long as power is supplied. Unlike dynamic RAM (DRAM), which requires periodic refreshes to maintain data retention, SRAM cells are bistable, meaning they have two stable states that can be used to represent a binary 0 or 1.

A 1-bit SRAM cell typically consists of a cross-coupled pair of inverters, forming a bistable latch. The stability of this latch allows it to store a binary value (0 or 1) until explicitly changed. The cell is sensitive to both READ and WRITE operations.

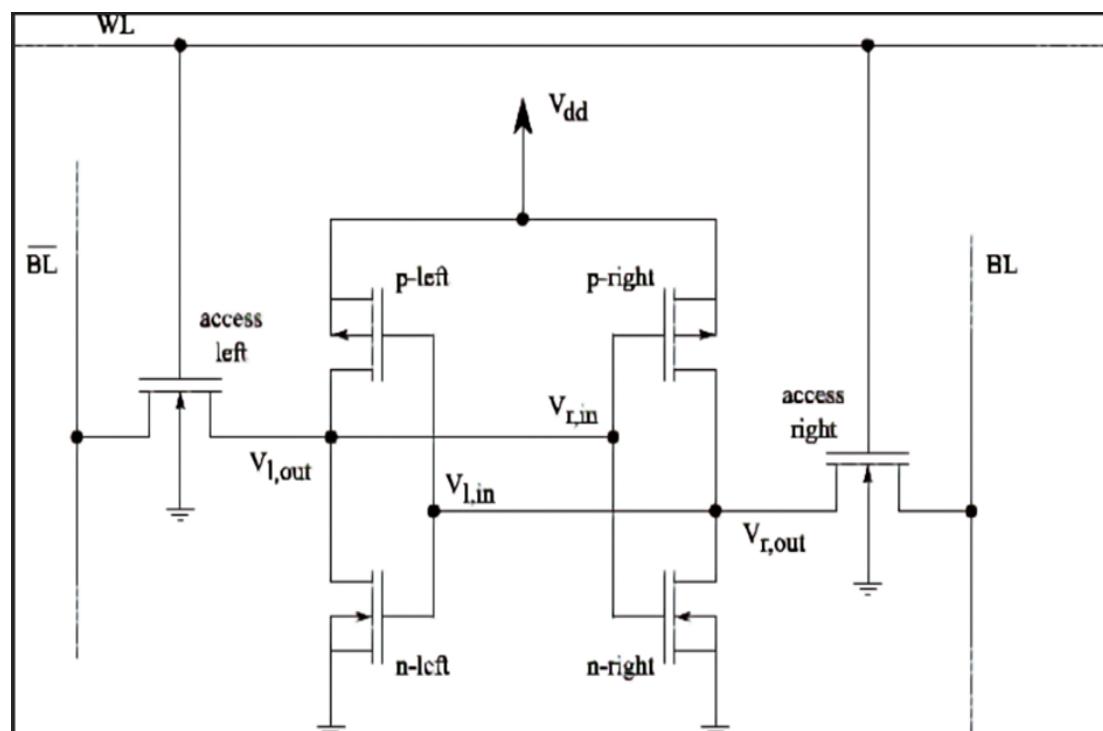
The fundamental element of an SRAM cell is the bistable latch. The bistable latch comprises two CMOS (Complementary metal-oxide-semiconductor) inverters that are cross-connected in a feedback cycle. The cross-connect ensures that one inverter's condition affects the other's condition, resulting in a stable binary memory element.

The READ operation involves accessing the stored value without altering it. This is done by activating the word line, which enables the pass transistors connected to the bit lines. The bit lines are then pre-charged to a high voltage, and sense amplifiers amplify the voltage

difference between the two-bit lines. The amplified voltage represents the stored value latched by other transistors.

The WRITE operation explicitly changes the stored value to 0 or 1. This is done by activating the word line and driving the appropriate bit line to a high or low voltage while the other is held at the opposite voltage. The cross-coupled inverters then latch onto the new state, overwriting the previous value.

Procedure:

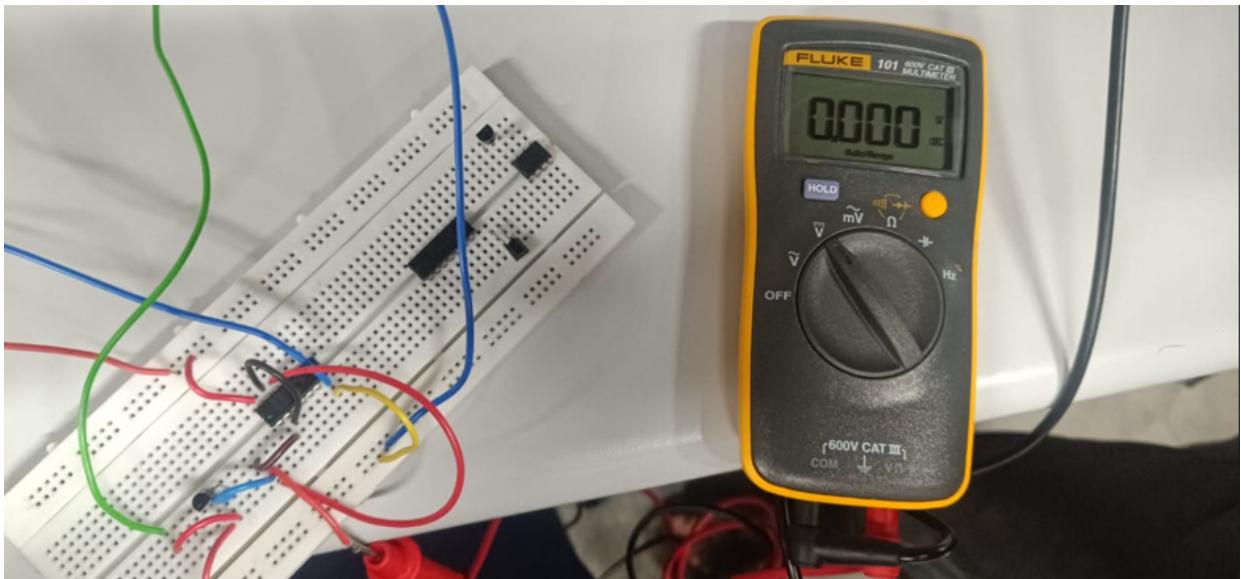


Observations:

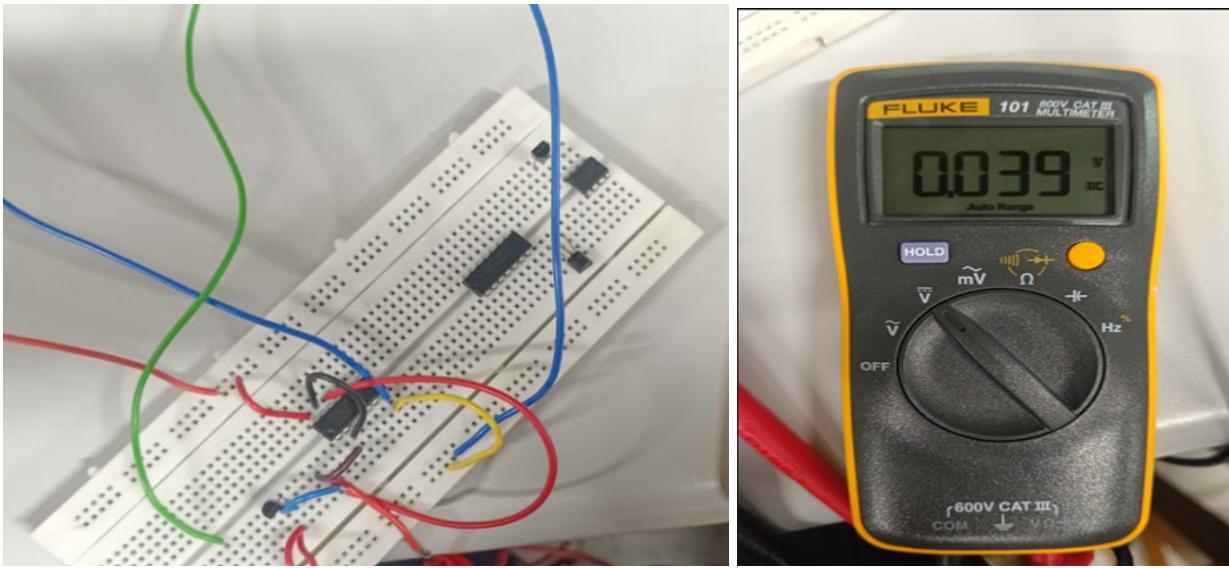
Reading:

Case-1:

- $V_{\text{source}} = 0V$, $V_{\text{gate}} = 5V$



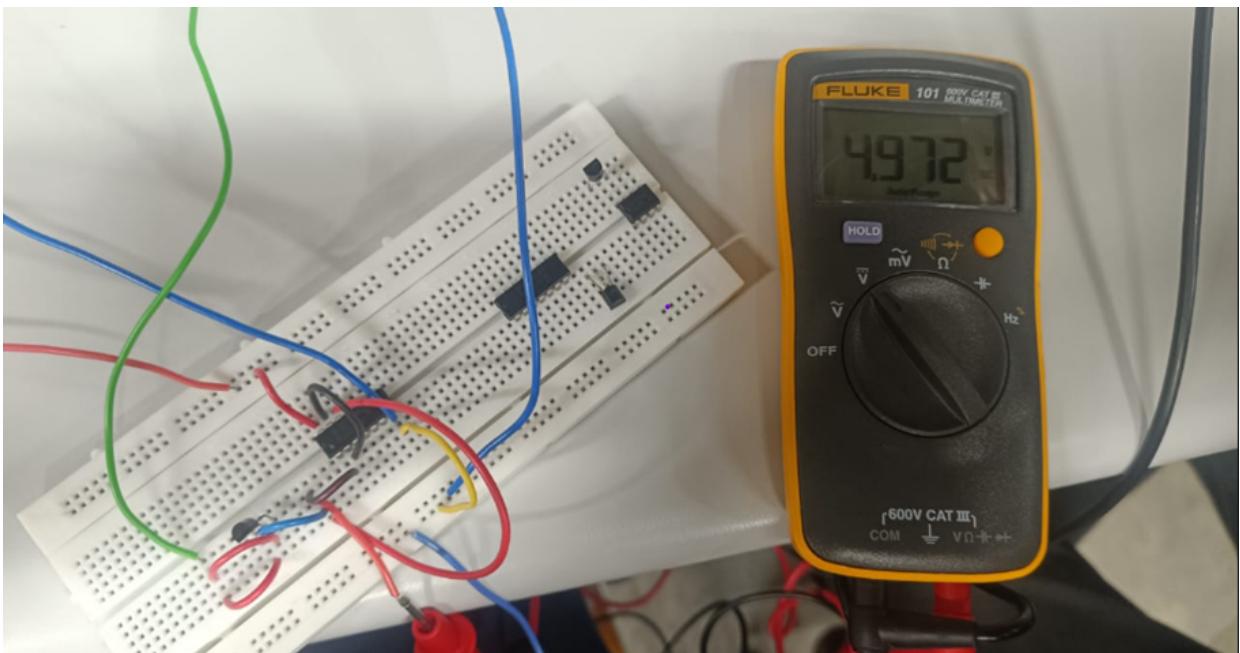
- $V_{\text{source}} = 0V$, $V_{\text{gate}} = 5V$



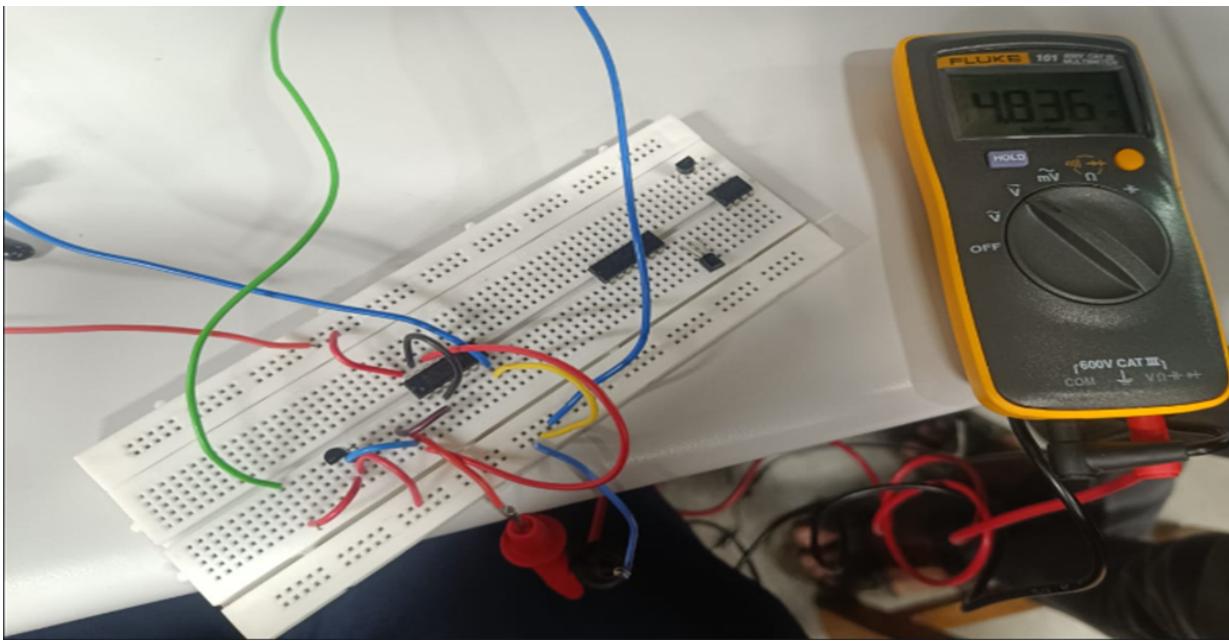
We read the value of state the value of 0 from the state terminal through the drain terminal and even when the gate terminal's voltage is made 0, The Bi-stable Latch still retains the value of the V_{source}

Case-2:

- $V_{\text{source}} = 5V, V_{\text{gate}} = 5V$



- $V_{\text{source}} = 5V, V_{\text{gate}} = 0V$



we read the value of state the value of 1 from the state terminal through the drain terminal and even when the gate terminal's voltage is made 1, The Bi-stable Latch still retains the value of the value of the V_{source}