**CME 435 Project**

Jason Wong

11200941

December 16, 2019

**Introduction**

All the scripts necessary to run the checks are located in the bin directory.

To run the scripts:

Phases 1-7: ./phase1\_top.csh

Phase 8: ./phase8\_coverage.csh (-l, -f)

Phase 9: ./phase9\_testcases.csh (-l, -t test\_sanity/test\_max\_payload/test\_min\_payload)

Regression Test: ./regression\_test.csh (-fc, -cc)

**Design Features to be Verified**

The input port protocol is as follows:

* The device samples inputs and updates the output on the negative edge of the clock
* Inputs are applied to the device at the positive edge of clock
* If valid\_in is not set (current input is not valid), then new input can be applied at any time (valid\_in should be set when data is applied)
* If valid\_in is set, then data at the receive port can be changed when rcv\_rdy is set to 1 (meaning device has read the input signals data and addr)

The output port protocol is as follows:

* The device transfers data from an input port to the output port indicated on the addr line of input port
* Output port signal addr\_out is set to the number of the input port where the data was received
* Device updates output port signals data\_out and addr\_out outputs on the negative edge of the clock
* If valid\_out is not set, then device can write to the output at any time
* If valid\_out is set, then device can write to an output port if data\_rd signal is set (meaning last data applied was read)

**Test Cases**

* The sanity check test case involves having the addr\_in and port\_in be random and cyclic so that there is no overlap in which ports the data is sent too.
* As for the maximum payload test case the constraint is to have the data\_in payload set to be 255 to see if the
* The minimum payload test case is forcing the data\_in generated to be at 0.

**Embedded Bugs**

* Reset error due to assertions checking if the reset is high when data\_out, addr\_out and valid\_out is low.
* Unfortunately, I did not have the time to complete the assertions so i only found one bug with reset.

**Error Injections**

* Sending to ports that are invalid, such as port 5.
* Driving more than one packet to the same port at the same time.

**Coverage Holes**

* Once I added in assertions the coverage bins went to zero. I’m not sure how to fix this problem.
* For the maximum payload it is not 100% coverage because of the data\_in is set as 255.
* For the minimum payload it is not 100% coverage since data\_in is set as 0 so it only goes to the low bin.
* For the sanity check it is not 100% since it is only driven to port 0.
* As for the valid\_in is not 100% since it is never set high in the testbench.

**Testbench Performance**

* It tests the ports if it goes to 0:3 and the max and min data\_in.
* Tests the addr\_in to see if data is sent to the ports between 0:3.
* The testbench itself is not fully complete since it does not have all the assertions to find the DUT bugs.
* As for the reusability, configurability and scalability I used a lot of code from my lab 5 to transition in the DUT for this project.
* The effectiveness is not the greatest since the tests could have been more extensive.