ARM PrimeCell™

Color LCD Controller (PL110)

Technical Reference Manual

ARM

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Color LCD Controller (PL110)
Technical Reference Manual

Release information

Change history

Date	Issue	Change
August 1999	A	First release
26 August 1999	B	Minor corrections to Chapter 4. Changes to Appendix A, Tables A-5 and A-6 added.
8 September 1999	C	Figs 2-3 to Fig 2-8 inserted. Changes to Tables A-5 and A-6.
1 December 2000	D	Errata changes to Fig 2-6, Table 3-2, 3-9, 3-14, and A-5. Section 1.1.6 and Fig 1-1 added.

Proprietary notice

Document confidentiality status

This document is Open Access. This document has no restriction on distribution.

Product status

The information in this document is Final (information on a developed product).

ARM web address

`http://www.arm.com`

Preface

This preface introduces the ARM PrimeCell Color LCD Controller (PL110) and its reference documentation. It contains the following sections:

About this document

This document is a technical reference manual for the ARM PrimeCell Color LCD Controller (PL110).

Intended audience

This document has been written for experienced hardware and software engineers who might or might not have experience of ARM products.

Organization

This document is organized into the following chapters:

Chapter 1 *Introduction*

Read this chapter for an introduction to the PrimeCell CLCDC and its features.

Chapter 2 *Functional Overview*

Read this chapter for a description of the major functional blocks of the PrimeCell CLCDC.

Chapter 3 *Programmer's Model*

Read this chapter for a description of the PrimeCell CLCDC registers and programming details.

Chapter 4 *Programmer's Model for Test*

Read this chapter for a description of the logic in the PrimeCell CLCDC for functional verification and production testing.

Appendix A *ARM PrimeCell Color LCD Controller (PL110) Signal Descriptions*

Read this appendix for details of the PrimeCell CLCDC signals.

Typographical conventions

The following typographical conventions are used in this document:

bold Highlights ARM processor signal names within text, and interface elements such as menu names. Can also be used for emphasis in descriptive lists where appropriate.

italic Highlights special terminology, cross-references and citations.

`typewriter` Denotes text that can be entered at the keyboard, such as commands, file names and program names, and source code.

`type`writer Denotes a permitted abbreviation for a command or option. The underlined text can be entered instead of the full command or option name.

`typewriter italic`
Denotes arguments to commands or functions where the argument is to be replaced by a specific value.

`typewriter bold`
Denotes language keywords when used outside example code.

Further reading

This section lists publications by ARM Limited.

ARM publications

This document contains information that is specific to the ARM PrimeCell Color LCD Controller (PL110). Refer to the following documents for other relevant information:

AMBA Specification (Rev 2.0) (ARM IHI 0011).
ARM PrimeCell CLCDC PL110 Design Manual (PL110 DDES 0000).
ARM PrimeCell CLCDC PL110 Integration Manual (PL110 INTM 0000).

Feedback

ARM Limited welcomes feedback both on the ARM PrimeCell Color LCD Controller (PL110), and on the documentation.

Feedback on this document

If you have any comments on about this document, please send email to `errata@arm.com` giving:

- the document title
- the document number
- the page number(s) to which your comments refer
- a concise explanation of your comments.

General suggestions for additions and improvements are also welcome.

Feedback on the ARM PrimeCell CLCDC (PL110)

If you have any comments or suggestions about this product, please contact your supplier giving:

- the product name
- a concise explanation of your comments.

Contents
ARM PrimeCell Color LCD Controller (PL110) Technical Reference Manual

Chapter 1
Introduction

This chapter introduces the ARM PrimeCell Color LCD Controller (PL110) and contains the following section:

- *About the ARM PrimeCell Color LCD Controller (PL110)* on page 1-2.

1.1 About the ARM PrimeCell Color LCD Controller (PL110)

The ARM PrimeCell *Color Liquid Crystal Display Controller* (CLCDC) is an *Advanced Microcontroller Bus Architecture* (AMBA) master-slave module that connects to the *Advanced High-performance Bus* (AHB). The PrimeCell CLCDC is an AMBA-compliant *System-on-a-Chip* (SoC) peripheral that is developed, tested and licensed by ARM.

The PrimeCell CLCDC is a reusable soft-IP block that has been developed with the prime aim of reducing time-to-market for ASIC development.

The PrimeCell CLCDC provides all the necessary control signals to interface directly to a variety of color and monochrome LCD panels.

1.1.1 Features of the PrimeCell Color LCD Controller

The principal features of the PrimeCell CLCDC are:

- compliance to the *AMBA Specification (Rev 2.0)* onwards for easy integration into SoC implementation
- dual 16-deep programmable 32-bit wide FIFOs for buffering incoming display data
- supports single and dual panel mono *Super Twisted Nematic* (STN) displays with 4 or 8-bit interfaces
- supports single and dual-panel color and monochrome STN displays
- supports *Thin Film Transistor* (TFT) color displays
- resolution programmable up to 1024 x 768
- 15 gray-level mono, 3375 color STN, and 32K color TFT support
- 1, 2 or 4 *bits-per-pixel* (bpp) palettized displays for mono STN
- 1, 2, 4 or 8 bpp palettized color displays for color STN and TFT
- 16 bpp true-color non-palettized, for color STN and TFT
- 24 bpp true-color non-palettized, for color TFT
- programmable timing for different display panels
- 256 entry, 16-bit palette RAM, arranged as a 128 x 32-bit RAM physically
- frame, line and pixel clock signals
- AC bias signal for STN, data enable signal for TFT panels
- patented gray-scale algorithm
- supports little and big-endian, as well as WinCE data formats.

1.1.2 Programmable parameters

The following key parameters can be programmed:

- horizontal front and back porch
- horizontal synchronization pulse width
- number of pixels per line
- vertical front and back porch
- vertical synchronization pulse width
- number of lines per panel
- number of panel clocks per line
- signal polarity, active HIGH or LOW
- AC panel bias
- panel clock frequency
- bits-per-pixel
- display type, STN mono/color or TFT
- STN 4 or 8-bit interface mode
- STN dual or single panel mode
- little-endian, big-endian or WinCE mode
- interrupt generation event.

1.1.3 Target markets

The markets to which the PrimeCell CLCDC is addressed are primarily in the portable segment. Typical applications for the PrimeCell CLCDC include:

- *Personal Digital Assistant* (PDA)
- ultra-sub notebook computer
- smart-phone
- hand-held, portable color games terminal.

1.1.4 LCD panel resolution

The PrimeCell CLCDC can be programmed to support a wide range of panel resolutions such as:

- 320 x 200, 320 x 240
- 640 x 200, 640 x 240, 640 x 480
- 800 x 600
- 1024 x 768.

1.1.5 Types of LCD panel supported

The PrimeCell CLCDC supports the following types of LCD panel:

- active matrix TFT panels with up to 24-bit bus interface
- single-panel monochrome STN panels (4-bit and 8-bit bus interface)
- dual-panel monochrome STN panels (4-bit and 8-bit bus interface per panel)
- single-panel color STN panels, 8-bit bus interface
- dual-panel color STN panels, 8-bit bus interface per panel.

1.1.6 Number of colors supported

The number of colors supported by the different types of panels are described in:

- *TFT panels*
- *Color STN panels*
- *Mono STN panels* on page 1-5.

TFT panels

TFT panels support one or more of the following color modes:

- 1 bpp, palettized, 2 colors selected from available colors.
- 2 bpp, palettized, 4 colors selected from available colors.
- 4 bpp, palettized, 16 colors selected from available colors.
- 8 bpp, palettized, 256 colors selected from available colors.
- 16 bpp, direct 5:5:5 RGB, with one bpp not normally being used. This pixel is still output, and can be used as a *bright* bit to connect to the *Least Significant Bit* (LSB) of R, G and B components of a 6:6:6 TFT panel.
- 24 bpp, direct 8:8:8 RGB, providing over 16 million colors.

Each 16-bit palette entry is composed of five bpp (RGB) plus a common intensity bit. This gives better memory utilization and performance compared with a full six bpp structure. The total amount of colors supported can be doubled from 32K to 64K if the intensity bit is used and applied to all three color components simultaneously. Refer to Appendix A *ARM PrimeCell Color LCD Controller (PL110) Signal Descriptions* for more information.

Color STN panels

Color STN panels support one or more of the following color modes:

- 1 bpp, palettized, 2 colors selected from 3375
- 2 bpp, palettized, 4 colors selected from 3375
- 4 bpp, palettized, 16 colors selected from 3375

- 8 bpp, palettized, 256 colors selected from 3375
- 16 bpp, direct 4:4:4 RGB, with 4 bpp not being used.

Mono STN panels

Mono STN panels support one or more of the following modes:

- 1 bpp, palettized, 2 gray scales selected from 15
- 2 bpp, palettized, 4 gray scales selected from 15
- 4 bpp, palettized, 16 gray scales selected from 15.

Greater than four bpp for mono panels can be programmed, but using these modes does not make sense, since the maximum number of gray scales supported on the display is 15.

1.1.7 LCD powering up and powering down sequence support

The PrimeCell CLCDC (PL110) allows the following power up sequence to be performed:

1. Vdd is simultaneously applied to the SoC (that contains the PrimeCell CLCDC PL110 peripheral) and panel display driver logic. The signals **CLLP**, **CLCP**, **CLFP**, **CLAC**, **CLD[23:0]** and **CLLE** are held LOW (inactive).

2. When Vdd is stabilized, a 1 is written to the LcdEn bit within the LCDControl Register. This enables the signals **CLLP**, **CLCP**, **CLFP**, **CLAC** and **CLLE** into their active states, but the **CLD[23:0]** signals remain in a LOW (inactive) state.

3. When the signals in (2) have stabilized, where appropriate, the contrast voltage VEE (this is not controlled or supplied by the PrimeCell CLCDC) is then applied.

4. If required, a software timer routine, can be used to provide the minimum display specific delay time between application of the control signals and power to the panel display. On completion of the software timer routine, power is applied to the panel by writing a 1 to the LcdPwr bit within the LcdControl register, which in turn, sets the **CLPOWER** signal HIGH and enables the **CLD[23:0]** signals into their active state. The **CLPOWER** signal is expected to be used to gate the power to the LCD panel.

The power down sequence is the reverse of the above four stages and must be strictly followed, this time, writing the respective register bits with 0.

The power up and power down sequences are shown in Figure 1-1 on page 1-6.

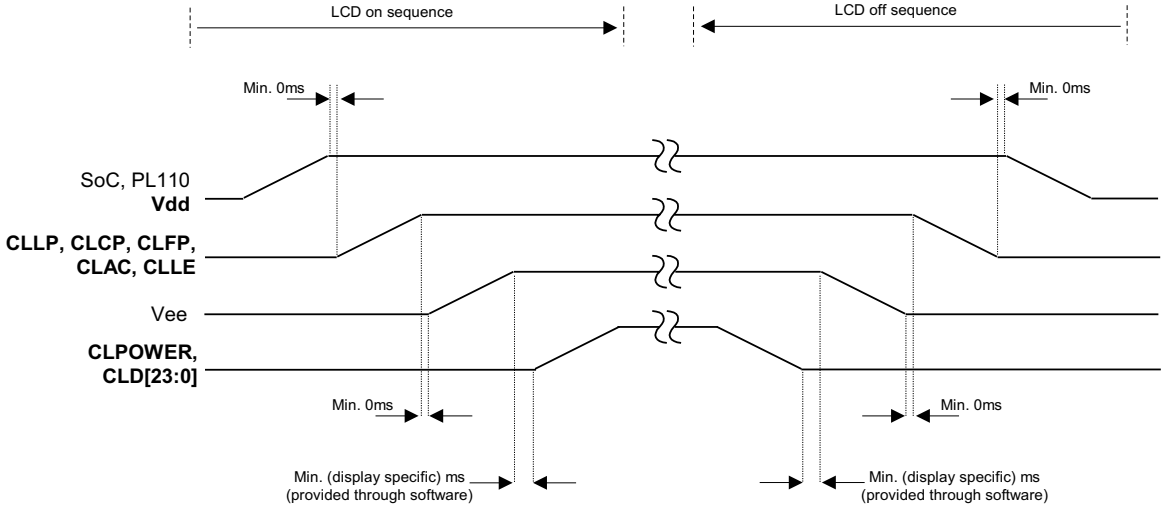

Figure 1-1 Power up and power down sequences

Chapter 2
Functional Overview

This chapter describes the major functional blocks of the ARM PrimeCell CLCDC (PL110) and contains the following sections:

2.1 ARM PrimeCell Color LCD Controller (PL110) overview

The PrimeCell CLCDC performs translation of pixel-coded data into the required formats and timings to drive a variety of single/dual mono and color LCDs.

Support is provided for passive *Super Twisted Nematic* (STN) and active *Thin Film Transisto*r (TFT) LCD display types.

STN displays STN display panels require algorithmic pixel pattern generation to provide pseudo gray scaling on mono, or color creation on color displays.

TFT displays TFT display panels require the digital color value of each pixel to be applied to the display data inputs.

Packets of pixel coded data are fed, via the AMBA AHB interface, to two independent, programmable, 32-bit wide, DMA FIFOs which act as input data flow buffers.

The buffered pixel coded data is then unpacked via a pixel serializer.

Dependent upon the LCD type and mode, the unpacked data may represent:

- an actual true display gray or color value
- an address to a 256 x 16 bit wide palette ram gray or color value.

In the case of STN displays, either a value obtained from the addressed palette location or the true value is passed to the gray scaling generators. The hardware coded gray scale algorithm logic sequences the addressed pixels activity over a programmed number of frames to provide the effective display appearance.

For TFT displays, either an addressed palette value or true color value is passed directly to the output display drivers, bypassing the gray scaling algorithmic logic.

Besides data formatting, the PrimeCell CLCDC provides a set of programmable display control signals, which include:

- LCD panel power enable
- pixel clock
- horizontal and vertical synchronization pulses
- display bias.

The PrimeCell CLCDC generates individual interrupts for:

- upper or lower panel DMA FIFO underflow
- base address update signification
- vertical compare
- bus error.

There is also a single combined interrupt that is raised when any of the individual interrupts become active.

A simplified block diagram of the PrimeCell CLCDC is shown in Figure 2-1.

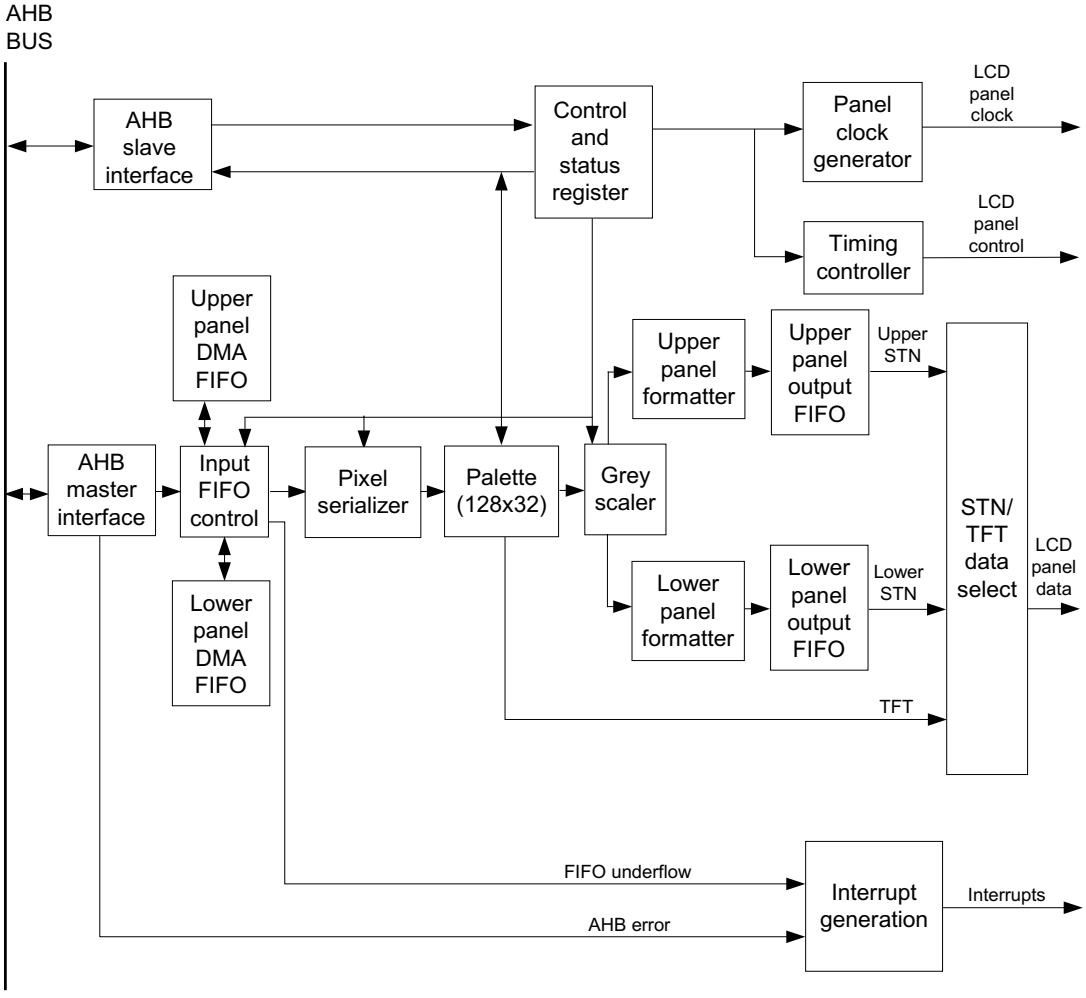

Figure 2-1 Block diagram of the PrimeCell CLCDC

2.2 AMBA AHB interface

The AMBA AHB interface comprises the following blocks:

- *AMBA AHB slave interface*
- *AMBA AHB master interface*.

2.2.1 AMBA AHB slave interface

The AMBA AHB slave interface connects the PrimeCell CLCDC to the AMBA AHB bus and provides CPU accesses to the registers and palette RAM. For more information on AMBA AHB slave interfaces, refer to the *AMBA Specification (Rev 2.0)*.

The following features are supported by the PrimeCell CLCDC AMBA AHB slave interface:

- standard write and read AMBA AHB accesses
- INCR4, INCR8 and undefined length WORD bursts only
- OKAY response only.

2.2.2 AMBA AHB master interface

The AMBA AHB master interface transfers display data from a selected slave (memory) to the PrimeCell CLCDC DMA FIFOs. It can be connected directly to the AMBA AHB system bus or to the AMBA AHB port of a memory controller, such as an SDRAM controller.

The inherent AMBA AHB master interface state machine performs the following functions:

- Loads the upper panel base address into the AMBA AHB address incrementer on recognition of a new frame.
- Monitors both the upper and lower DMA FIFO levels and asserts **HBUSREQM** to request display data from memory, filling them to above the programmed water mark. **HBUSREQM** is re-asserted when there are at least four locations available within either FIFO (dual panel mode).
- Checks for 1KB boundaries during fixed-length bursts, appropriately adjusting the address in such occurrences.
- Generates the address sequences for fixed-length and undefined bursts.
- Controls the handshaking between the memory and DMA FIFOs. It inserts busy cycles if the FIFOs have not completed their synchronization and updating sequence.

- Fills up the DMA FIFOs, in dual panel mode, in an alternating fashion from a single **HBUSREQM** request and subsequent **HGRANTM**.
- Asserts the **CLCDMBEINTR** interrupt if an error occurs during an active burst.
- Responds to retry commands by restarting the failed access.

2.2.3 Dual DMA FIFOs and associated control logic

The pixel data accessed from memory is buffered by two DMA FIFOs which can be independently controlled to cover single and dual panel LCD types. Each FIFO is 16 words deep by 32 bits wide and can be cascaded to form an effective 32-word deep FIFO in single panel mode. The input ports of the FIFOs are connected to the AMBA AHB interface and the output port feeds the pixel serializer.

Synchronization logic is used to transfer the pixel data from the AMBA AHB **HCLK** domain to the **CLCDCLK** clock domain, the DMA FIFOs being clocked by the former.

The water level marks within each FIFO are set such that each FIFO requests data when at least four locations become available.

An interrupt signal is asserted if an attempt is made to read either of the two DMA FIFOs when they are empty, in other words an underflow condition has occurred.

2.2.4 Pixel serializer

This block reads the 32-bit wide LCD data from output port of the DMA FIFO and extracts 24, 16, 8, 4, 2 or 1 BPP data, depending on the current mode of operation. The PrimeCell CLCDC supports big-endian, little-endian and WinCE data formats. In dual panel mode, data is alternately read from the upper and lower DMA FIFOs. Dependent upon the mode of operation the extracted data may be used to point to a color/grayscale value in the palette ram or may actually be a true color value that can be directly applied to an LCD panel input.

Figure 2-2 on page 2-6 through to Figure 2-7 on page 2-8 show the structure of the data in each DMA FIFO word corresponding to the endianness and bpp combinations. For each of the three supported data formats, the required data for each panel display pixel must be extracted from the data word.

The nomenclature used in the figures is:

- *Little Endian Byte, Little Endian Pixel* (LBLP) order
- *Big Endian Byte, Big Endian Pixel* (BBBP) order
- *Little Endian Byte, Big Endian Pixel* (LBBP) order (this is the WinCE format).

	DMA FIFO OUTPUT BITS															
bpp	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	p31	p30	p29	p28	p27	p26	p25	p24	p23	p22	p21	p20	p19	p18	p17	p16
2	p15		p14		p13		p12		p11		p10		p9		p8	
	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
4	p7				p6				p5				p4			
	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
8	p3								p2							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
16	p1															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
24	p0															
									23	22	21	20	19	18	17	16

Figure 2-2 LBLP, DMA FIFO output bits 31 to 16

	DMA FIFO OUTPUT BITS															
bpp	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	p15	p14	p13	p12	p11	p10	p9	p8	p7	p6	p5	p4	p3	p2	p1	p0
2	p7		p6		p5		p4		p3		p2		p1		p0	
	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
4	p3				p2				p1				p0			
	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
8	p1								p0							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
16	p0															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
24	p0															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Figure 2-3 LBLP, DMA FIFO output bits 15 to 0

bpp	DMA FIFO OUTPUT BITS															
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	p0	p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15
2	p0		p1		p2		p3		p4		p5		p6		p7	
	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
4	p0				p1				p2				p3			
	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
8	p0								p1							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
16	p0															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
24	p0															
									23	22	21	20	19	18	17	16

Figure 2-4 BBBP, DMA FIFO output bits 31 to 16

bpp	DMA FIFO OUTPUT BITS															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	p16	p17	p18	p19	p20	p21	p22	p23	p24	p25	p26	p27	p28	p29	p30	p31
2	p8		p9		p10		p11		p12		p13		p14		p15	
	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
4	p4				p5				p6				p7			
	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
8	p2								p3							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
16	p1															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
24	p0															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Figure 2-5 BBBP, DMA FIFO output bits 15 to 0

bpp	DMA FIFO OUTPUT BITS															
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	p24	p25	p26	p27	p28	p29	p30	p31	p16	p17	p18	p19	p20	p21	p22	p23
2	p12		p13		p14		p15		p8		p9		p10		p11	
	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
4	p6				p7				p4				p5			
	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
8	p3								p2							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
16	p1															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
24	p0															
									23	22	21	20	19	18	17	16

Figure 2-6 LBBP, DMA FIFO output bits 31 to 16

bpp	DMA FIFO OUTPUT BITS															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	p8	p9	p10	p11	p12	p13	p14	p15	p0	p1	p2	p3	p4	p5	p6	p7
2	p4		p5		p6		p7		p0		p1		p2		p3	
	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
4	p2				p3				p0				p1			
	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
8	p1								p0							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
16	p0															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
24	p0															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Figure 2-7 LBBP, DMA FIFO output bits 15 to 0

2.2.5 RAM palette

The RAM-based palette is a 256 x 16 bit dual port RAM physically structured as 128 x 32 bit. This allows two entries to be written into the palette from a single word write access. The least significant bit of the serialized pixel data is used to select between upper and lower halves of the palette RAM. Which half is selected depends on the byte ordering mode. In little-endian mode, the LSB being set selects the upper half, but in big-endian, the lower half of the palette is selected. WinCE byte ordering is little-endian, so the former case applies.

Pixel data values can be written and verified via the AMBA AHB slave interface. For information on the numbers of colors supported, please refer to *Number of colors supported* on page 1-4.

The palette RAM is a dual port RAM with independent controls and addresses for each port. Port1 is used as a read/write port and is connected to the AMBA AHB slave interface. The palette entries can be written and verified through this port. Port2 is used as a read-only port and is connected to the unpacker and gray scaler. Table 2-1 shows the bit representation of each word in the palette.

Table 2-1 Palette data storage

Bit	Name	Description
31	I	Intensity/unused
30:26	B[4:0]	Blue palette data
25:20	G[4:0]	Green palette data
19:16	R[4:0]	Red palette data
15	I	Intensity/unused
14:10	B[4:0]	Blue palette data
9:5	G[4:0]	Green palette data
4:0	R[4:0]	Red palette data

For mono STN mode only the red palette field bits (4:1) are used. However, in STN color mode the green and blue [4:1] are also used.

The red and blue pixel data can be swapped to support BGR data format via a control register bit.

In 16 and 24 bpp TFT mode, the palette is bypassed and the output of the pixel serializer is used as the TFT panel data.

2.2.6 Gray scaler

A patented gray scale algorithm drives mono and color STN panels. This provides 15 gray scales for mono displays. In the case of STN color displays, the three color components (red, green and blue) are *gray scaled* simultaneously which results in 3375 (15 x 15 x 15) colors being available. The gray scaler transforms each 4-bit gray value into a sequence of activity-per-pixel over several frames, relying to some degree on the display characteristics, to give the representation of gray scales and color.

2.2.7 Upper and lower panel formatters

Each formatter consists of three 3-bit (red, green and blue) shift left registers. Red, green and blue pixel data bit values from the gray scaler are concurrently shifted into the respective registers. When enough data is available, a byte is constructed by multiplexing the registered data to the correct bit position to satisfy the RGB data pattern of LCD panel. The byte is transferred to the 3-byte FIFO, which has enough space to store eight color pixels.

2.2.8 Panel clock generator

The output of the panel clock generator block is the panel clock. This is a divided down version of **CLCDCLK**. It can be programmed in the range **CLCDCLK/**2 to **CLCDCLK/**33 to match the bpp data rate of the LCD panel.

2.2.9 Timing controller

The primary function of the timing controller block is to generate the horizontal and vertical timing panel signals. It also provides panel bias/enable signal. These timings are all register programmable via the AMBA AHB slave interface.

2.2.10 Interrupt generation

The PrimeCell CLCDC provides four individually maskable interrupts and a single combined interrupt. The single combined interrupt is asserted if any of the combined interrupts are asserted and unmasked.

2.2.11 Bus architecture

The PrimeCell CLCDC incorporates a master interface and can be connected directly onto the main system AHB bus, or alternatively to an AMBA AHB port of a memory controller, such as an SDRAM controller.

In addition to the AMBA AHB master interface, there is also an AMBA AHB slave interface for programming registers within the device. The slave interface and the master interface are separate AMBA AHB slaves and masters. This means that the PrimeCell CLCDC can be connected up in one of two ways:

- It can be built such that the master interface and the slave interface connect to a single multi-master AMBA AHB bus interface.
- The master interface can connect directly to a memory controller (for example a SDRAM controller) with an AMBA AHB slave interface, while the slave interface connects to the AMBA AHB bus.

These two arrangements are shown in Figure 2-8 on page 2-11 and Figure 2-9 on page 2-12.

AMBA AHB supports a wide range of on-chip bus sizes, from eight bits up to 1024 bits. The PrimeCell CLCDC master and slave interfaces are implemented as 32-bit data bus devices only.

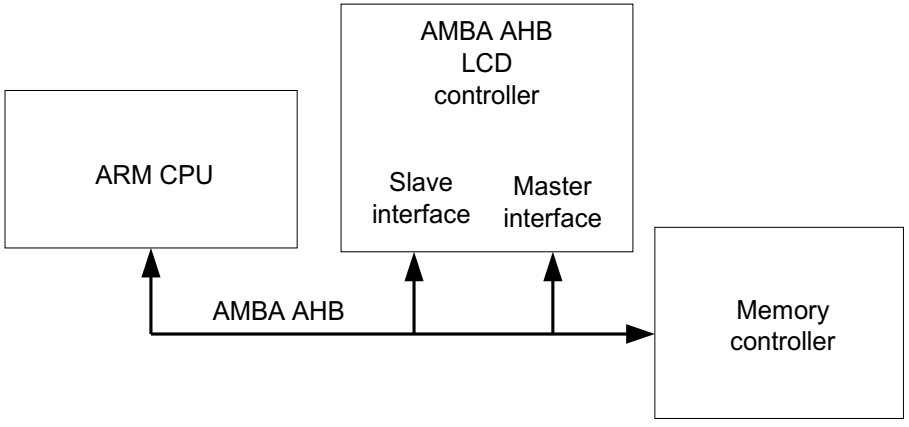

Figure 2-8 Single AMBA AHB bus architecture

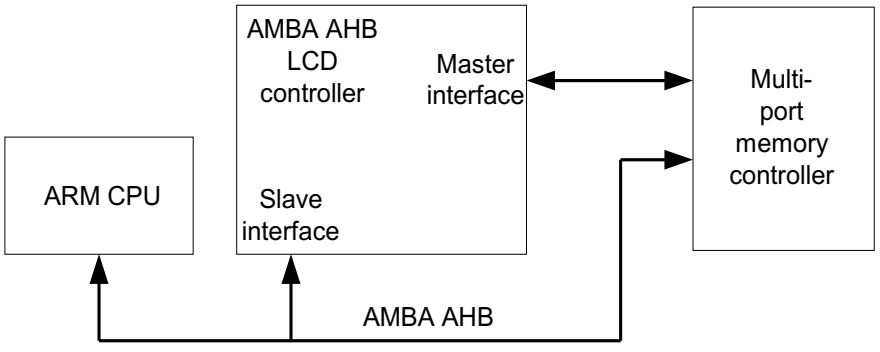

Figure 2-9 Dual-bus AMBA AHB architecture

Chapter 3
Programmer's Model

This chapter describes the ARM PrimeCell Color LCD Controller (PL110) registers and provides details needed when programming the microcontroller. It contains the following sections:

3.1 About the programmer's model

The base address of the ARM PrimeCell CLCDC is not fixed and can be different for any particular system implementation. However, the offset of any particular register from the base address is fixed.

The following locations are reserved, and must not be used during normal operation:

- locations at offsets 0x030 through 0x1FC are reserved for possible future extensions
- locations at offsets 0x400 through 0x7FF are reserved for test purposes.

The PrimeCell CLCDC registers are shown in Table 3-1.

Table 3-1 PrimeCell CLCDC register summary

Address	Type	Width	Reset value	Name	Description
CLCDC Base + 0x00	Read/write	32	0x00000000	LCDTiming0	Horizontal axis panel control
CLCDC Base + 0x004	Read/write	32	0x00000000	LCDTiming1	Vertical axis panel control
CLCDC Base + 0x08	Read/write	27	0x0000000	LCDTiming2	Clock and signal polarity control
CLCDC Base + 0x0C	Read/write	17	0x00000	LCDTiming3	Line end control
CLCDC Base + 0x010	Read/write	32	0x0000000	LCDUPBASE	Upper panel frame base address
CLCDC Base + 0x14	Read/write	32	0x00000000	LCDLPBASE	Lower panel frame base address
CLCDC Base + 0x18	Read/write	5	0x00000000	LCDINTRENABLE	Interrupt enable mask
CLCDC Base + 0x1C	Read/write	16	0x0000	LCDControl	LCD panel pixel parameters
CLCDC Base + 0x20	Read/write	5	0x00000000	LCDStatus	Raw interrupt status
CLCDC Base + 0x024	Read	5	0x00000000	LCDInterrupt	Final masked interrupts

Table 3-1 PrimeCell CLCDC register summary (continued)

Address	Type	Width	Reset value	Name	Description
CLCDC base + 0x28	Read	32	X	LCDUPCURR	LCD upper panel current address value
CLCDC base + 0x2C	Read	32	X	LCDLPCURR	LCD lower panel current address value
CLCDC base + 0x030 – 0x1FC	-	-	-	-	Reserved
CLCDC base + 0x200 - 0x3FC	Read/write	32	-	LCDPalette	256 x 16-bit color palette

3.2 Register descriptions

The following registers are described in this section:

For each of the register descriptions, the format of the title is:

Register name [bit width] (Offset from base).

3.2.1 LCDTiming0 [32] (+ 0x00)

LCDTiming0 is a read/write register that controls the:

- *Horizontal Synchronization pulse Width* (HSW)
- *Horizontal Front Porch* (HFP) period
- *Horizontal Back Porch* (HBP) period
- *Pixels-Per-Line* (PPL).

Table 3-2 shows the bit assignments for the LCDTiming0.

Table 3-2 LCDTiming0 register

Bit	Name	Type	Description
31-24	HBP	Read/write	Horizontal back porch, is the number of **CLCP** periods between the falling edge of **CLLP** and the start of active data. Program with value minus 1. The 8-bit HBP field is used to specify the number of pixel clock periods inserted at the beginning of each line or row of pixels. After the line clock for the previous line has been de-asserted, the value in HBP is used to count the number of pixel clocks to wait before starting the next display line. HBP can generate a delay of 1 to 256 pixel clock cycles.
23-16	HFP	Read/write	Horizontal front porch, is the number of **CLCP** periods between the end of active data and the rising edge of **CLLP**. Program with value minus 1. The 8-bit HFP field sets the number of pixel clock intervals at the end of each line or row of pixels, before the LCD line clock is pulsed. Once a complete line of pixels is transmitted to the LCD driver, the value in HFP is used to count the number of pixel clocks to wait before asserting the line clock. HFP can generate a period of 1 to 256 pixel clock cycles.
15-8	HSW	Read/write	Horizontal synchronization pulse width, is the width of the **CLLP** signal in **CLCP** periods. Program with value minus 1. The 8-bit HSW field specifies the pulse width of the line clock in passive mode, or the horizontal synchronization pulse in active mode.
7-2	PPL	Read/write	Pixels-per-line. Actual pixels-per-line = 16 * (PPL + 1). The PPL bit field specifies the number of pixels in each line or row of the screen. PPL is a 6-bit value that represents between 16 and 1024 PPL. PPL is used to count the number of pixel clocks that occur before the HFP is applied (program the value required divided by 16, minus 1).
1-0	-	Read/write	Reserved.

Horizontal timing restrictions

DMA requests new data at the start of a horizontal display line. Some time must be allowed for the DMA transfer and for the data to propagate down the FIFO path in the LCD interface. The data path latency forces some restrictions on the usable minimum values for horizontal porch width in STN mode. The minimum values are HSW = 2 and HBP = 2.

Single panel mode:

- HSW = 3
- HBP = 5

- HFP = 5
- *Panel Clock Divisor* (PCD) = 1 (**CLCDCLK**/3).

Dual panel mode:

- HSW = 3
- HBP = 5
- HFP = 5
- PCD = 5 (**CLCDCLK**/7).

If sufficient time is given at the start of the line (for example, setting HSW = 6, HBP = 10), data will not get corrupted for PCD = 4 (minimum value).

3.2.2 LCDTiming1 [32] (+ 0x04)

LCDTiming1 is a read/write register that controls the:

- number of *Lines-Per-Panel* (LPP)
- *Vertical Synchronization pulse Width* (VSW)
- *Vertical Front Porch* (VFP) period
- *Vertical Back Porch* (VBP) period.

Table 3-3 shows the bit allocations for the LCDTiming1.

Table 3-3 LCDTiming1 register

Bit	Name	Type	Description
31-24	VBP	Read/write	Vertical back porch is the number of inactive lines at the start of a frame, after vertical synchronization period. Program to zero on passive displays or reduced contrast will result. The 8-bit VBP field is used to specify the number of line clocks inserted at the beginning of each frame. The VBP count starts just after the vertical synchronization signal for the previous frame has been negated for active mode, or the extra line clocks have been inserted as specified by the VSW bit field in passive mode. After this has occurred, the count value in VBP sets the number of line clock periods inserted before the next frame. VBP generates from 0–255 extra line clock cycles.
23-16	VFP	Read/write	Vertical front porch is the number of inactive lines at the end of frame, before vertical synchronization period. Program to zero on passive displays or reduced contrast will result. The 8-bit VFP field is used to specify the number of line clocks to insert at the end of each frame. Once a complete frame of pixels is transmitted to the LCD display, the value in VFP is used to count the number of line clock periods to wait. After the count has elapsed the vertical synchronization (**CLFP**) signal is asserted in active mode, or extra line clocks are inserted as specified by the VSW bit-field in passive mode. VFP generates from 0–255 line clock cycles.
15-10	VSW	Read/write	Vertical synchronization pulse width is the number of horizontal synchronization lines. Must be small (for example, program to zero) for passive STN LCDs. Program to the number of lines required minus one. The higher the value the worse the contrast on STN LCDs. The 6-bit VSW field is used to specify the pulse width of the vertical synchronization pulse. The register is programmed with the number of line clocks in VSync minus one. Number of horizontal synchronization lines. Must be small (for example, program to zero) for passive STN LCDs. Program to the number of lines required minus one. The higher the value the worse the contrast on STN LCDs.
9-0	LPP	Read/write	Lines per panel is the number of active lines per screen. Program to number of lines required minus 1. The LPP field specifies the total number of lines or rows on the LCD panel being controlled. LPP is a 10-bit value allowing between 1 and 1024 lines. The register is programmed with the number of lines per LCD panel minus 1. For dual panel displays this register is programmed with the number of lines on each of the upper and lower panels.

3.2.3 LCDTiming2 [27] (+ 0x08)

LCDTiming2 is a read/write register that controls the CLCDC timing.

Table 3-4 LCDTiming2 register

Bit	Name	Type	Description
31-27	-	Read/write	Reserved.
26	BCD	Read/write	Bypass pixel clock divider. Setting this to 1 bypasses the pixel clock divider logic. This is mainly used for TFT displays.
25-16	CPL	Read/write	Clocks per line. This field specifies the number of actual CLCP clocks to the LCD panel on each line. This is the number of PPL divided by either 1 (TFT), 4 or 8 (for mono passive), $2\ ^2/_3$ (for color passive), minus one. This must be correctly programmed in addition to PPL for the LCD controller to work correctly.
15	-	Read/write	Reserved.
14	IOE	Read/write	Invert output enable: 0 = CLAC output pin is active HIGH in TFT mode 1 = CLAC output pin is active LOW in TFT mode. The *Invert Output Enable* (IOE) bit is used to select the active polarity of the output enable signal in TFT mode. In this mode, the CLAC pin is used as an enable that indicates to the LCD panel when valid display data is available. In active display mode, data is driven onto the LCD data lines at the programmed edge of CLCP when CLAC is in its active state.
13	IPC	Read/write	Invert panel clock: 0 = Data is driven on the LCDs data lines on the rising-edge of **CLCP** 1 = Data is driven on the LCDs data lines on the falling-edge of **CLCP**. The IPC bit is used to select the edge of the panel clock on which pixel data is driven out onto the LCD data lines.
12	IHS	Read/write	Invert horizontal synchronization: 0 = CLLP pin is active HIGH and inactive LOW 1 = CLLP pin is active LOW and inactive HIGH. The *Invert HSync* (IHS) bit is used to invert the polarity of the CLLP signal.
11	IVS	Read/write	Invert vertical synchronization: 0 = CLFP pin is active HIGH and inactive LOW 1 = CLFP pin is active LOW and inactive HIGH. The *Invert VSync* (IVS) bit is used to invert the polarity of the CLFP signal.

Table 3-4 LCDTiming2 register (continued)

Bit	Name	Type	Description
10-6	ACB	Read/write	AC bias pin frequency. The AC bias pin frequency is only applicable to STN displays, which require the pixel voltage polarity to be periodically reversed to prevent damage due to DC charge accumulation. Program this field with the required value minus one to apply the number of line clocks between each toggle of the AC bias pin (CLAC). This field has no effect if the PrimeCell CLCDC is operating in TFT mode, when the CLAC pin is used as a data enable signal.
5	CLKSEL	Read/write	This bit drives the **CLCDCLKSEL** signal, which is used as the select signal for the external LCD clock multiplexor.
4-0	PCD	Read/write	Panel clock divisor.[a] The five-bit PCD field is used to derive the LCD panel clock frequency **CLCP** from the CLCDCLK frequency, **CLCP =** CLCDCLK/(PCD+2). For mono STN displays with a four or eight-bit interface, the panel clock will be a factor of four and eight down on the actual individual pixel clock rate. For color STN displays, 2 $^{2}/_{3}$ pixels are output per **CLCP** cycle, hence the panel clock is 0.375 times. For TFT displays the pixel clock divider can be bypassed by setting the LCDTiming2[26] BCD bit.

a. The data path latency forces some restrictions on the usable minimum values for the panel clock divider in STN modes.
Single panel color mode: PCD = 1 (**CLCP** = CLCDCLK/3)
Dual panel color mode: PCD = 4 (**CLCP** = CLCDCLK/6)
Single panel mono 4-bit interface mode: PCD = 2(**CLCP** = CLCDCLK/4)
Dual panel mono 4-bit interface mode: PCD = 6(**CLCP** = CLCDCLK/8)
Single panel mono 8-bit interface mode: PCD = 6(**CLCP** = CLCDCLK/8)
Dual panel mono 8-bit interface mode: PCD = 14(**CLCP** = CLCDCLK/16)

3.2.4 LCDTiming3 [17] (+ 0x0C)

LCDTiming3 is a read/write register that controls the enabling of line-end signal **CLLE**. When enabled, a positive pulse. four **CLCDCLK** periods wide, is output on **CLLE** after a programmable delay, LED from the last pixel of each display line. If the line-end signal is disabled it is held permanently LOW. Table 3-5 shows the bit assignments for the LCDTiming3.

Table 3-5 LCDTiming3 register

Bit	Name	Type	Description
31 - 17	-	Read/write	Reserved.
16	LEE	Read/write	LCD Line end enable: 0 = **CLLE** disabled (held LOW) 1 = **CLLE** signal active.
15 - 7	-	Read/write	Reserved.
6 - 0	LED	Read/write	Line-end signal delay from the rising-edge of the last panel clock (CLCP). Program with number of **CLCDCLK** clock periods minus 1.

3.2.5 LCDUPBASE [32] (+ 0x10) and LCDLPBASE [32] (+ 0x14)

LCDUPBASE and LCDLPBASE are the color LCD DMA base address registers. They are read/write registers used to program the base address of the frame buffer. LCDUPBase is used for:

- TFT displays
- single panel STN displays
- the upper panel of dual panel STN displays.

LCDLPBase is used for the lower panel of dual panel STN displays.

The programmer must initialize LCDUPBase (and LCDLPBase for dual panels) before enabling the PrimeCell CLCDC.

Optionally the value can be changed mid-frame to allow double-buffered video displays to be created. These registers are copied to the corresponding current registers at each LCD vertical synchronization. This event causes the LNBU bit and an optional interrupt to be generated. The interrupt can be used to reprogram the base address when generating double-buffered video.

Bits [1:0] are zero value when read.

Table 3-6 and Table 3-7shows the bit assignment for the LCDUPBASE and the LCDLPBASE registers.

Table 3-6 LCDUPBASE register

Bit	Name	Type	Description
31-2	LCDUPBASE	Read/write	LCD upper panel base address. This is the start address of the upper panel frame data in memory and is word aligned.
1:0	-	-	Reserved.

Table 3-7 LCDLPBASE register

Bit	Name	Type	Description
31-2	LCDLPBASE	Read/write	LCD lower panel base address. This is the start address of the lower panel frame data in memory and is word aligned.
1:0	-	-	Reserved.

3.2.6 LCDINTRENABLE [5] (+ 0x18)

LCDINTRENABLE is the interrupt enable register. Setting of bits within this register enables the corresponding raw interrupt LCDStatus bit values to be passed to the LCDInterrupt register. Table 3-8 shows the bit assignment for the LCDINTRENABLE.

Table 3-8 LCDINTRENABLE register

Bit	Name	Type	Description
4	MBERRINTRENB	Read/write	AHB master error interrupt enable.
3	VCOMPINTRENB	Read/write	Vertical compare interrupt enable.
2	LNBUINTRENB	Read/write	Next base update interrupt enable.
1	FUFINTRENB	Read/write	FIFO underflow interrupt enable.
0	-	-	Reserved.

3.2.7 LCDControl [16] (+ 0x1C)

LCDControl is the control register. It is a read/write register that controls the mode in which the Primecell CLCDC operates. Table 3-9 shows the bit assignment for the LCDControl.

Table 3-9 LCDControl register

Bit	Name	Type	Description
31-17	-	Read/write	Reserved.
16	WATERMARK	Read/write	LCD DMA FIFO Watermark level: 0 = HBUSREQM is raised when either of the two DMA FIFOs have four or more empty locations. 1 = HBUSREQM is raised when either of the DMA FIFOs have eight or more empty locations.
15	LDmaFIFOTME	Read/write	LCD DMA FIFO test mode enable: 0 = DMA FIFO inaccessible to user 1 = DMA FIFO read/write access for FIFO RAM testing. (To be set only when LCD is disabled via bit 0 of this register).
14	-	Read/write	Reserved.
13-12	LcdVComp	Read/write	Generate interrupt at: 00 = start of vertical synchronization 01 = start of back porch 10 = start of active video 11 = start of front porch
11	LcdPwr	Read/write	LCD power enable: 0 = power not gated through to LCD panel and **CLD[23:0]** signals disabled, (held LOW) 1 = power gated through to LCD panel and **CLD[23:0]** signals enabled, (active). Refer to *LCD powering up and powering down sequence support* on page 1-5 for details on LCD power sequencing.
10	BEPO	Read/write	Big-endian pixel ordering within a byte: 0 = little-endian ordering within a byte 1= big-endian pixel ordering within a byte. The BEPO bit selects between little and big-endian pixel packing for 1, 2 and 4 bpp display modes, it has no effect on 8 or 16 bpp pixel formats. Refer to *Pixel serializer* on page 2-5 for more information on the data format.
9	BEBO	Read/write	Big-endian byte order: 0 = little-endian byte order 1 = big-endian byte order.

Table 3-9 LCDControl register (continued)

Bit	Name	Type	Description
8	BGR	Read/write	RGB of BGR format selection: 0 = RGB normal output 1 = BGR red and blue swapped.
7	LcdDual	Read/write	LCD interface is dual panel STN: 0 = single panel LCD is in use 1 = dual panel LCD is in use.
6	LcdMono8	Read/write	Monochrome LCD has an 8-bit interface. This bit controls whether monochrome STN LCD uses a 4 or 8-bit parallel interface. It has no meaning in other modes and must be programmed to zero. 0 = mono LCD uses 4-bit interface 1 = mono LCD uses 8-bit interface.
5	LcdTFT	Read/write	LCD is TFT: 0 = LCD is an STN display - use gray scaler 1 = LCD is TFT - do not use gray scaler.
4	LcdBW	Read/write	STN LCD is monochrome (black and white): 0 = STN LCD is color 1 = STN LCD is monochrome. This bit has no meaning in TFT mode.
3-1	LcdBpp	Read/write	LCD bits per pixel: 000 = 1 bpp 001 = 2 bpp 010 = 4 bpp 011 = 8 bpp 100 = 16 bpp 101 = 24 bpp (TFT panel only) 110 = reserved 111 = reserved.
0	LcdEn	Read/write	LCD controller enable: 0 = LCD signals **CLLP**, **CLCP**, **CLFP**, **CLAC**, and **CLLE** disabled (held LOW) 1 = LCD signals **CLLP**, **CLCP**, **CLFP**, **CLAC**, and **CLLE** enabled (active). Refer to *LCD powering up and powering down sequence support* on page 1-5 for details on LCD power sequencing.

3.2.8 LCDStatus [5] (+ 0x20)

LCDStatus is a read/write register. On a read it returns five bits that can generate interrupts when set. On writes to this register, a bit value of 1 will clear the interrupt corresponding to that bit. Writing a 0 will have no effect. Table 3-10 shows the bit assignment for the LCDStatus.

Table 3-10 LCDStatus register

Bit	Name	Type	Description
4	MBERROR	Read/clear	AMBA AHB master bus error status, set when the AMBA AHB master encounters a bus error response from a slave.
3	Vcomp	Read/clear	Vertical compare, set when one of the four vertical regions, selected via the LCDControl register, is reached.
2	LNBU	Read/clear	LCD next address base update, mode dependent, set when the current base address registers have been successfully updated by the next address registers. Signifies that a new next address can be loaded if double buffering is in use.
1	FUF	Read/clear	FIFO underflow, set when either the upper or lower DMA FIFOs have been read accessed when empty causing an underflow condition to occur.
0	-	-	Reserved.

3.2.9 LCDInterrupt [5] (+ 0x24)

LCDInterrupt is a read-only register. It is a bit-by-bit logical AND of the LCDStatus register and the LCDINTRENABLE register. Interrupt lines correspond to each interrupt. A logical OR of all interrupts is provided to the system interrupt controller. Table 3-11 shows the bit assignment for the LCDInterrupt.

Table 3-11 LCDInterrupt register

Bit	Name	Type	Description
4	MBERRORINTR	Read	AHB master error interrupt status bit.
3	VCOMPINTR	Read	Vertical compare interrupt status bit.
2	LNBUINTR	Read	LCD next base address update interrupt status bit.
1	FUFINTR	Read	FIFO underflow interrupt status bit.
0	-	-	Reserved.

3.2.10 LCDUPCURR [32] (+ 0x28) and LCDLPCURR [32] (+ 0x2C)

LCDUPCURR and LCDLPCURR are registers that contain an approximate value of the upper and lower panel data DMA addresses when read. The registers can change at any time and therefore can only be used as a mechanism for coarse delay.

Table 3-12 and Table 3-13 shows the bit assignment for the LCDUPCURR and LCDLPCURR registers.

Table 3-12 LCDUPCURR register

Bit	Name	Type	Description
32-0	LCDUPCURR	Read	Contains the approximate current upper panel data DMA address.

Table 3-13 LCDLPCURR register

Bit	Name	Type	Description
32-0	LCDLPCURR	Read	Contains the approximate current lower panel data DMA address.

3.2.11 LCDPalette [32] (+ 0x0200 - 0x3FC)

LCDPalette registers contain 256 palette entries organized as 128 locations of two entries per word.

Only TFT displays use all of the palette entry bits.

Each word location contains two palette entries. This means that 128 word locations are used for the palette. When configured for little-endian byte ordering, bits [15:0] are the lower numbered palette entry and [31:16] are the higher numbered palette entry. When configured for big-endian byte ordering this is reversed, as bits [31:16] are the low numbered palette entry and [15:0] are the high numbered entry.

Table 3-14 shows the bit assignment for the LCDPalette.

Table 3-14 LCDPalette register

Bit	Name	Type	Description
4:0	R[4:0]	Read/write	Red palette data. For STN displays, only the four MSBs (bits 4:1) are used. For monochrome displays only the red palette data is used. All the palette registers have the same bit fields.
9:5	G[4:0]	Read/write	Green palette data.
14:10	B[4:0]	Read/write	Blue palette data.
15	I	Read/write	Intensity bit, can be used as the LSB of the R, G and B inputs to a 6:6:6 TFT display, doubling the number of colors to 64K, where each color has two different intensities.
20:16	R[4:0]	Read/write	Red palette data.
25:21	G[4:0]	Read/write	Green palette data.
30:26	B[4:0]	Read/write	Blue palette data.
31	I	Read/write	Intensity/unused.

3.3 Interrupts

There are five interrupts generated by the PrimeCell CLCDC, four of these are individual maskable active HIGH interrupts:

- *CLCDMBEINTR*
- *CLCDVCOMPINTR*
- *CLCDLNBUINTR* on page 3-18
- *CLCDFUFINTR* on page 3-18.

The outputs are also output as a combined single interrupt CLCDINTR.

Each of the four individual maskable interrupts is enabled or disabled by changing the mask bits in the LCDINTRENABLE register.

Provision of individual outputs as well as a combined interrupt output allows the use of either a global interrupt service routine, or modular device drivers to handle interrupts.

The status of the individual interrupt sources can be read from the LCDStatus register.

3.3.1 CLCDMBEINTR

The master bus error interrupt is asserted when an ERROR response is received by the master interface during a transaction with a slave. When such an error is encountered, the master interface enters an error state and remains in this state until clearance of the error has been signalled to it. On completion of the respective interrupt service routine, the master bus error interrupt can be cleared by writing a 1 to the MBERROR bit within the LCDStatus register. This action releases the master interface from its ERROR state to the start of FRAME state, allowing a fresh frame of data display to be initiated.

3.3.2 CLCDVCOMPINTR

The vertical compare interrupt is asserted when one of four vertical display regions, selected via the LCD control register, is reached. The interrupt can be made to occur at the start of:

- vertical synchronization
- back porch
- active video
- front porch.

The interrupt can be cleared by writing a 1 to the VComp bit within the LCDStatus register.

3.3.3 CLCDLNBUINTR

The LCD next base address update interrupt is asserted when either the LCDUPBASE or the LCDLPBASE values have been transferred to the LCDUPCURR or LCDLPCURR incrementers respectively. This signals to the system that it is safe to update the LCDUPBASE or the LCDLPBASE registers with new frame base addresses if required.

The interrupt can be cleared by writing a 1 to the LNBU bit within the LCDStatus register.

3.3.4 CLCDFUFINTR

The FIFO underflow interrupt is asserted when internal data is requested from an empty DMA FIFO. Internally, individual upper and lower panel DMA FIFO underflow interrupt signals are generated and CLCDFUFINTR is the single combined version of these.

The interrupt can be cleared by writing a 1 to the FUF bit within the LCDStatus register.

Chapter 4
Programmer's Model for Test

This chapter describes the additional logic for functional verification and production testing. It contains the following sections:

4.1 Scan testing

The PrimeCell CLCDC has been designed to allow:

- the automatic insertion of scan test cells
- the use of *Automatic Test Pattern Generation* (ATPG).

This is the recommended method of manufacturing test.

During scan testing, the **SCANMODE** must be driven HIGH to allow bypassing of the DMS FIFOs. For normal use **SCANMODE** must be negated LOW.

4.2 Test registers

The PrimeCell CLCDC test registers are memory-mapped as shown in Table 4-1.

Table 4-1 Test registers memory map

Address	Type	Width	Reset value	Name	Description
CLCDBase + 0x400 -0x7FC	Read/write	32	-	LCDDMAFIFO	Provides access to the DMA FIFO via AHB interface.

Test access to the DMA FIFO is provided via the LCDDMAFIFO test register.

To enter test mode, the PrimeCell CLCDC must be disabled by clearing LCDControl[0] LCDEn bit to zero. Then set LCDControl[15} LDmaFIFOTME bit to 1. The FIFO can then be written and read via the AHB interface.

Appendix A
ARM PrimeCell Color LCD Controller (PL110) Signal Descriptions

This appendix describes the signals that interface with the ARM PrimeCell Color LCD Controller (PL110) and contains the following sections:

A.1 AMBA AHB slave interface signals

The following tables summarize the ARM PrimeCell Color LCD Controller signal list.

Table A-1 lists the AMBA AHB slave interface signals.

Table A-1 AMBA AHB slave interface signals

Signal name	Type	Source/ destination	Description
HCLK	Input	AMBA AHB bus	Bus clock. This clock times all bus transfers. All signal timings are related to the rising edge of **HCLK**.
HRESETn	Input	AMBA AHB bus	Bus reset signal. The bus reset signal is used to reset the system and the bus. This is an active LOW signal.
HSELCLCD	Input	Decoder	Device select signal.
HADDRS[10:2]	Input	AMBA AHB bus	Address bus.
HTRANSS[1:0]	Input	AMBA AHB bus	Indicates the type of the current transfer, which can be nonsequential, sequential, idle or busy.
HWRITES	Input	AMBA AHB bus	When HIGH this signal indicates a write transfer and when LOW a read transfer.
HWDATAS[31:0]	Input	AMBA AHB bus	Write data bus.
HRDATAS[31:0]	Output	AMBA AHB bus	Read data bus.

Table A-1 AMBA AHB slave interface signals (continued)

Signal name	Type	Source/ destination	Description
HREADYSin	Input	AMBA AHB bus	When HIGH this signal indicates that a transfer has finished on the bus. This signal may be driven LOW to extend the transfer.
HREADYSout	Output	AMBA AHB bus	When HIGH this signal indicates that the slave is ready for the next transfer. This signal may be driven LOW to extend the transfer.
HRESPS[1:0]	Output	AMBA AHB bus	The transfer response provides additional information on the status of a transfer. Only the OKAY response is supported.

A.2 AMBA AHB master interface signals

Table A-2 lists the AMBA AHB master interface signals.

Table A-2 AMBA AHB master interface signals

Signal name	Type	Source/ destination	Description
HADDRM[31:0]	Output	AMBA AHB bus	Address bus.
HTRANSM[1:0]	Output	AMBA AHB bus	Indicates the type of the current transfer, which can be nonsequential, sequential, idle or busy.
HWRITEM	Output	AMBA AHB bus	When HIGH this signal indicates a write transfer and when LOW a read transfer.
HSIZEM[2:0]	Output	AMBA AHB bus	Indicates the size of the transfer. Only word size accesses are supported.
HBURSTM[2:0]	Output	AMBA AHB bus	Indicates if the transfer forms a part of the burst. 4, 8 and 16 incrementing bursts are supported.
HRDATAM[31:0]	Input	AMBA AHB bus	Read data bus.
HREADYMin	Input	AMBA AHB bus	When HIGH this signal indicates that a transfer has finished on the bus. This signal may be driven LOW to extend the transfer.
HRESPM[1:0]	Input	AMBA AHB bus	The transfer response provides additional information on the status of a transfer. Only OKAY, ERROR, and RETRY responses are fully supported.
HPROT[3:0]	Output	AMBA AHB bus	The protection signals provide additional information about a bus access. They are primarily intended for use by any module that wishes to implement some level of protection.

Table A-2 AMBA AHB master interface signals (continued)

Signal name	Type	Source/ destination	Description
HLOCK	Output	Arbiter	When HIGH this signal indicates that the master requires locked access.
HBUSREQM	Output	Arbiter	Bus request. When HIGH this indicates that the bus master requires the bus.
HGRANTM	Input	Arbiter	Bus grant. This signal indicates that the bus master is currently the highest priority master. Ownership of the address/control signals changes at the end of a transfer when **HREADYMin** is HIGH, and this master gets access to the bus when both **HREADYMin** and **HGRANTM** are HIGH.

A.3 External pad interface signals

Table A-3 lists the output PAD interface signals.

Table A-3 External pad interface signals

Signal name	Type	Source/ destination	Description
CLPOWER	Output	PAD	LCD panel power enable.
CLLP	Output	PAD	Line synchronization pulse (STN)/horizontal synchronization pulse (TFT).
CLCP	Output	PAD	LCD panel clock.
CLFP	Output	PAD	Frame pulse (STN)/vertical synchronization pulse (TFT).
CLAC	Output	PAD	STN AC bias drive or TFT data enable output.
CLD[23:0]	Output	PAD	LCD panel data.
CLLE	Output	PAD	Line end signal.

A.4 On-chip signals

A free-running reference clock, **CLCDCLK**, must be provided. By default it is assumed to be asynchronous to **HCLK**.

The reset inputs are asynchronously asserted but synchronously removed for each of the clock domains within the PrimeCell CLCDC. This ensures that logic is reset even if clocks are not present, to avoid any static power consumption problems at power up. Each clock domain has an individual reset to simplify the process of inserting scan test cells.

The on-chip signals required in addition to the AMBA AHB signals are shown in Table A-4 .

Table A-4 On-chip signals

Signal name	Type	Source/ destination	Description
CLCDCLK	Input	Clock multiplexor	PrimeCell CLCDC reference clock.
nCLCDCLK	Input	Clock multiplexor	Inverse of PrimeCell CLCDC reference clock.
CLCDCLKSEL	Output	Clock multiplexor	PrimeCell CLCDC reference clocks select signal. It is driven by bit 5 of LCDTiming2 register and selects between **HCLK** or **CLCDCLK** as the source for the reference clocks.
CLCLKRESETn	Input	Reset multiplexor	PrimeCell CLCDC reset signal to the **CLCDCLK** domain, active LOW. The reset controller must use **HRESETn** to assert **CLCLKRESETn** asynchronously but negate it synchronously with **CLCDCLK**.
CLCDMBEINTR	Output	Interrupt controller	PrimeCell CLCDC master bus error interrupt, active HIGH.

Table A-4 On-chip signals (continued)

Signal name	Type	Source/ destination	Description
CLCDFUFINTR	Output	Interrupt controller	PrimeCell CLCDC FIFO underflow interrupt, active HIGH. A combined interrupt generated when either of the upper or lower panel DMA FIFOs underflow.
CLCDLNBUINTR	Output	Interrupt controller	PrimeCell CLCDC next base address update interrupt, active HIGH.
CLCDVCOMPINTR	Output	Interrupt controller	PrimeCell CLCDC vertical region compare interrupt, active HIGH.
CLCDINTR	Output	Interrupt controller	PrimeCell CLCDC interrupt, active HIGH. A single combined interrupt generated as an OR function of the four individually maskable interrupts above.
SCANMODE	Input	Test controller	PrimeCell CLCDC scan test hold input. This signal must be asserted HIGH to bypass the DMA FIFOs during scan testing.

A.5 LCD panel signal multiplexing details

The **CLLP**, **CLAC**, **CLFP**, **CLCP** and **CLLE** signals are common but the CLD[23:0] bus has eight modes of operation corresponding to:

- TFT 24-bit interface
- TFT 18-bit interface
- color STN single panel
- color STN Dual panel
- 4-bit mono STN single panel
- 4-bit mono STN dual panel
- 8-bit mono STN single panel
- 8-bit mono STN dual panel.

Note

CUSTN = Color upper panel STN, dual and/or single panel.
CLSTN = Color lower panel STN, single.
MUSTN = Mono upper panel STN, dual and/or single panel.
MLSTN = Mono lower panel STN, single.

Table A-5 shows which CLD[23:0] pins are used to supply the pixel data to the STN panel for each of the above modes of operation.

Table A-5 LCD STN panel signal multiplexing

External pin	Color STN single panel	Color STN dual panel	4-bit mono STN single panel	4-bit mono STN dual panel	8-bit mono STN single panel	8-bit mono STN dual panel
CLD[23]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
CLD[22]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
CLD[21]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
CLD[20]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
CLD[19]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
CLD[18}	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
CLD[17]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
CLD[16]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
CLD[15]	Reserved	**CLSTN[0]**	Reserved	Reserved	Reserved	**MLSTN[0]**
CLD[14]	Reserved	**CLSTN[1]**	Reserved	Reserved	Reserved	**MLSTN[1]**
CLD[13]	Reserved	**CLSTN[2]**	Reserved	Reserved	Reserved	**MLSTN[2]**
CLD[12]	Reserved	**CLSTN[3]**	Reserved	Reserved	Reserved	**MLSTN[3]**
CLD[11]	Reserved	**CLSTN[4]**	Reserved	**MLSTN[0]**	Reserved	**MLSTN[4]**
CLD[10]	Reserved	**CLSTN[5]**	Reserved	**MLSTN[1]**	Reserved	**MLSTN[5]**
CLD[9]	Reserved	**CLSTN[6]**	Reserved	**MLSTN[2]**	Reserved	**MLSTN[6]**
CLD[8]	Reserved	**CLSTN[7]**	Reserved	**MLSTN[3]**	Reserved	**MLSTN[7]**
CLD[7]	**CUSTN[0]**	**CUSTN[0]**	Reserved	Reserved	**MUSTN[0]**	**MUSTN[0]**
CLD[6]	**CUSTN[1]**	**CUSTN[1]**	Reserved	Reserved	**MUSTN[1]**	**MUSTN[1]**
CLD[5]	**CUSTN[2]**	**CUSTN[2]**	Reserved	Reserved	**MUSTN[2]**	**MUSTN[2]**
CLD[4]	**CUSTN[3]**	**CUSTN[3]**	Reserved	Reserved	**MUSTN[3]**	**MUSTN[3]**
CLD[3]	**CUSTN[4]**	**CUSTN[4]**	**MUSTN[0]**	**MUSTN[0]**	**MUSTN[4]**	**MUSTN[4]**

Table A-5 LCD STN panel signal multiplexing (continued)

External pin	Color STN single panel	Color STN dual panel	4-bit mono STN single panel	4-bit mono STN dual panel	8-bit mono STN single panel	8-bit mono STN dual panel
CLD[2]	CUSTN[5]	CUSTN[5]	MUSTN[1]	MUSTN[1]	MUSTN[5]	MUSTN[5]
CLD[1]	CUSTN[6]	CUSTN[6]	MUSTN[2]	MUSTN[2]	MUSTN[6]	MUSTN[6]
CLD[0]	CUSTN[7]	CUSTN[7]	MUSTN[3]	MUSTN[3]	MUSTN[7]	MUSTN[7]

Table A-6 shows which CLD[23:0] pins are used to supply the pixel data to the TFT panel for each of the above modes of operation.

Table A-6 LCD TFT panel signal multiplexing

External pin	TFT 24 bit	TFT 18 bit
CLD[23]	**BLUE[7]**	Reserved
CLD[22]	**BLUE[6]**	Reserved
CLD[21]	**BLUE[5]**	Reserved
CLD[20]	**BLUE[4]**	Reserved
CLD[19]	**BLUE[3]**	Reserved
CLD[18}	**BLUE[2]**	Reserved
CLD[17]	**BLUE[1]**	**BLUE[4]**
CLD[16]	**BLUE[0]**	**BLUE[3]**
CLD[15]	**GREEN[7]**	**BLUE[2]**
CLD[14]	**GREEN[6]**	**BLUE[1]**
CLD[13]	**GREEN[5]**	**BLUE[0]**
CLD[12]	**GREEN[4]**	Intensity bit
CLD[11]	**GREEN[3]**	**GREEN[4]**
CLD[10]	**GREEN[2]**	**GREEN[3]**
CLD[9]	**GREEN[1]**	**GREEN[2]**
CLD[8]	**GREEN[0]**	**GREEN[1]**
CLD[7]	**RED[7]**	**GREEN[0]**
CLD[6]	**RED[6]**	Intensity bit
CLD[5]	**RED[5]**	**RED[4]**
CLD[4]	**RED[4]**	**RED[3]**
CLD[3]	**RED[3]**	**RED[2]**

Table A-6 LCD TFT panel signal multiplexing (continued)

External pin	TFT 24 bit	TFT 18 bit
CLD[2]	**RED[2]**	**RED[1]**
CLD[1]	**RED[1]**	**RED[0]**
CLD[0]	**RED[0]**	Intensity bit

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