

right @ William C. Cheng

100

AILLASI SAGL

Process A

Processor

UMM

regs

Core

luner

100

irtual addr

Basic Idea: Address Translation

One level of indirection with a Memory Management Unit (MMU)

∪ wirtual address is translated into physical address via MMU

Process B

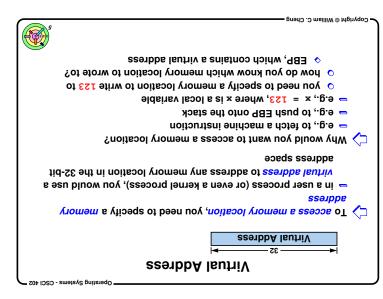
■ use a Memory Management Unit (MMU)

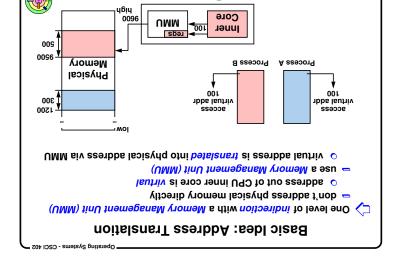
don't address physical memory directly
 address out of CPU inner core is virtual

цвіц

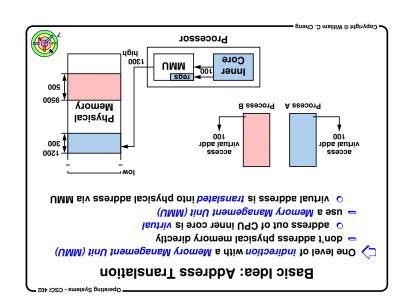
Метогу

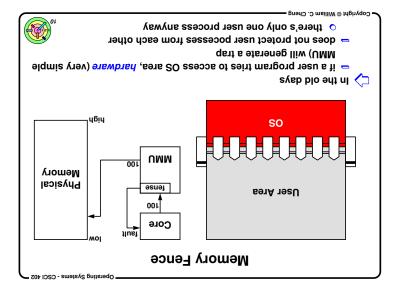
Physical

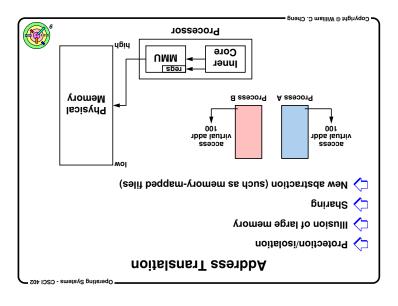


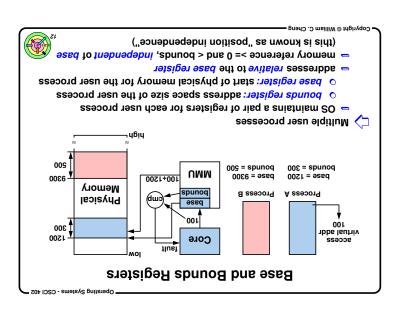


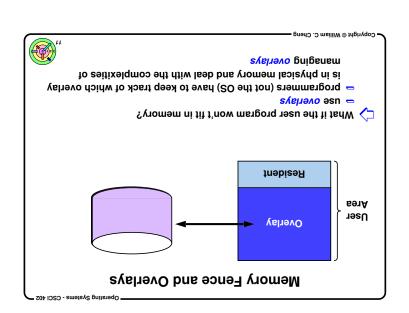
Processor

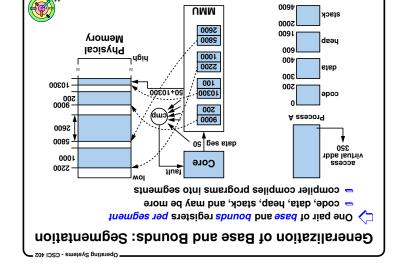


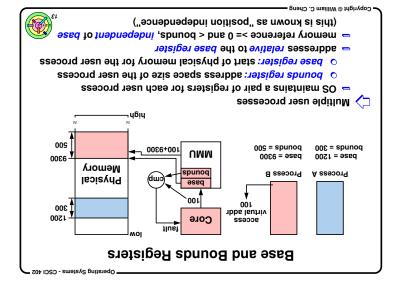


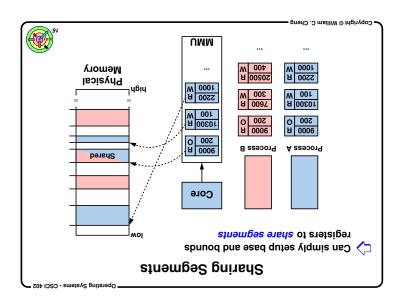


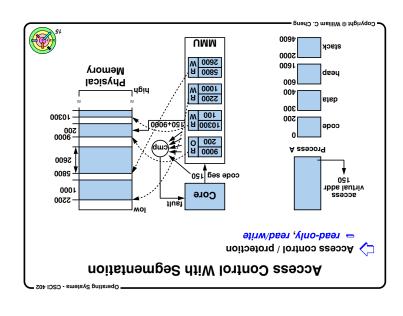


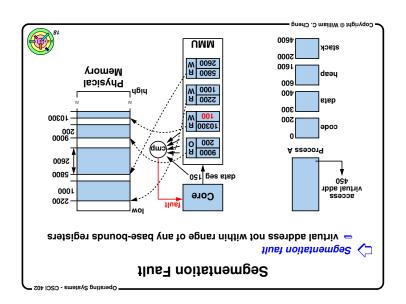


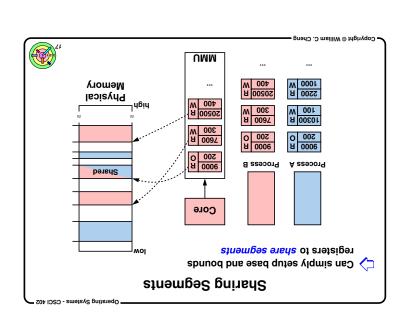


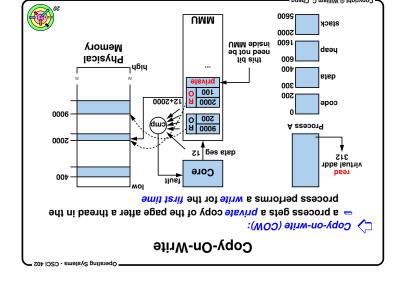


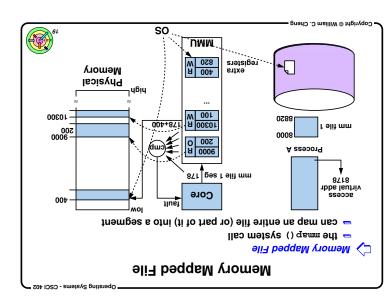


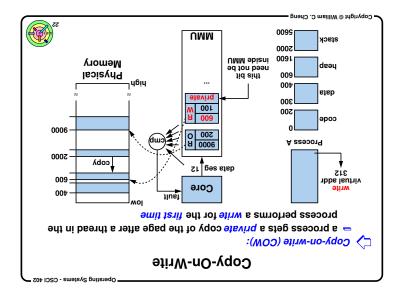


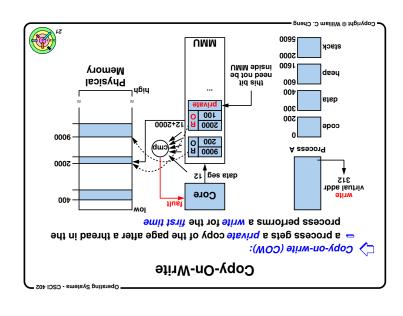


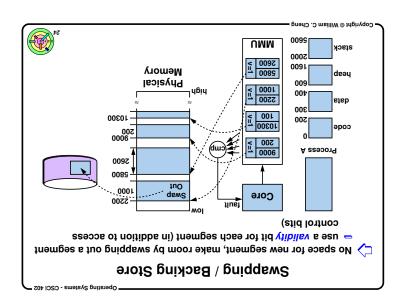


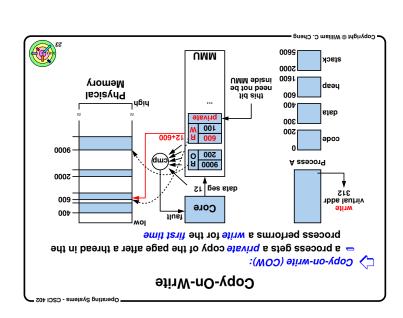


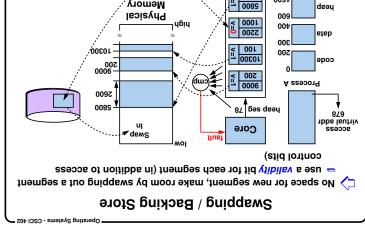


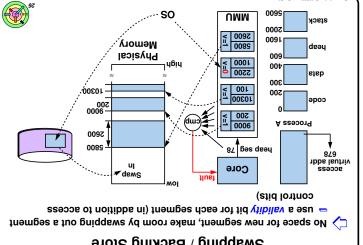


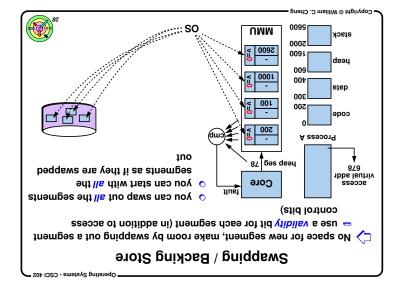


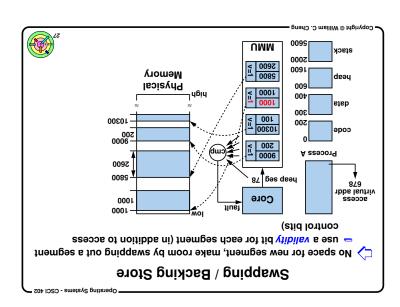












Memory

Physical

0006

5000

വെട്ട

1000 2200

10300

Core

= use a validity bit for each segment (in addition to access

🗘 No space for new segment, make room by swapping out a segment

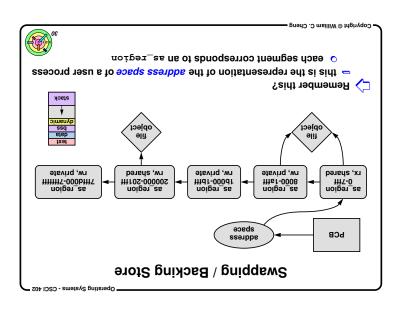
Swapping / Backing Store

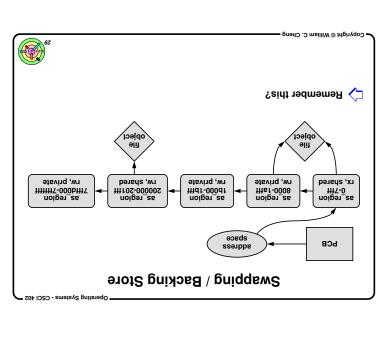
200

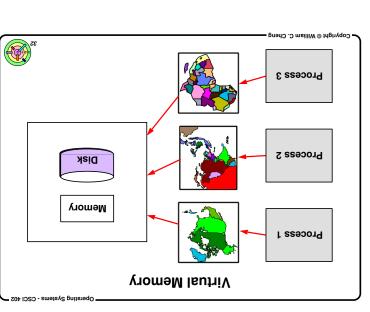
eteb

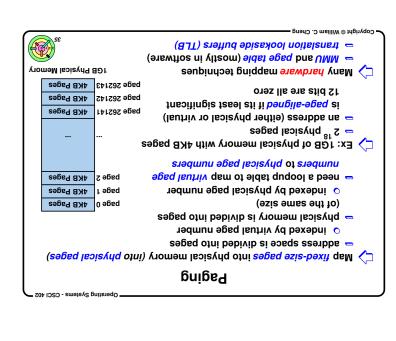
Process A

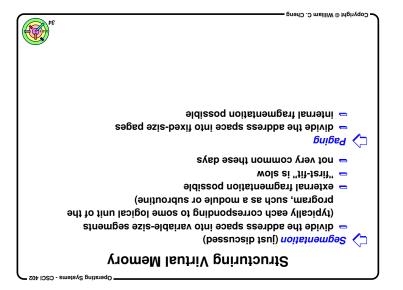
control bits)











about physical pages and their association with important kernel A page frame data structure / object is used to maintain information

Page Frames

Рһуѕіса! Метогу

4KB bages

Page Frame

"physical page" interchangeably

o we use "page frame" and

between page frames and

e there is a one-to-one mapping

- contains a physical page number

bhysical pages

data structures

