A 1GHz 0.56 pJ
4-bit Absolute-Value Detector for use in Neural Spike Sorting

Joani Bajlozi
Sanjana Sarda

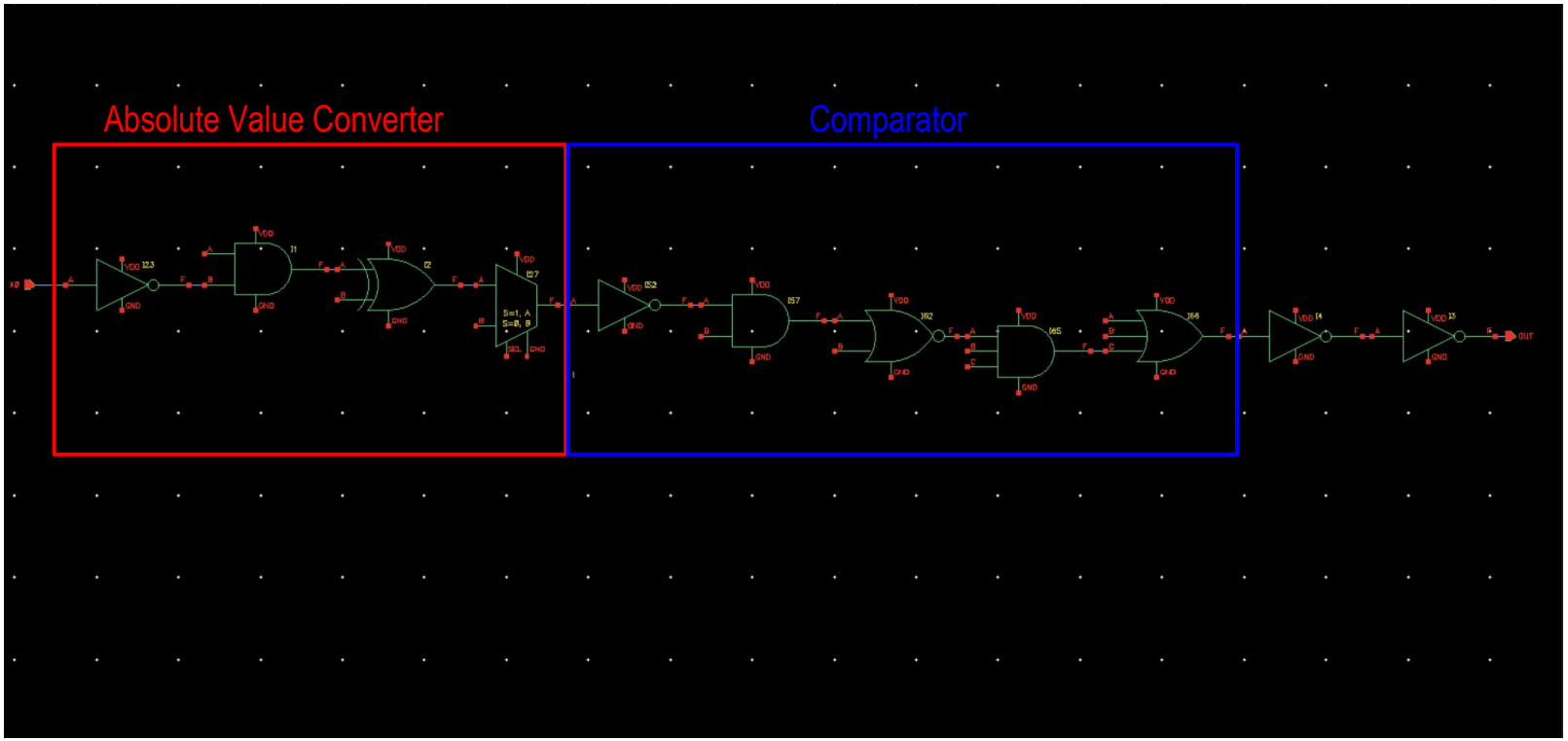
Design Summary

- A) Circuit topology: Optimized 3-bit Full Adder and 3-bit Comparator
- B) Circuit Style: Pass-Transistor Logic and Static CMOS
- C) WHY: Moderate Area and Fast, Regular Design

Schematic	Layout size	Energy	Verification
$t_{p\_X0 \rightarrow OUT}$ = 286.242 ps	X= 21µm, Y= 19.5µm	Sch E = 564 fJ	Func: Y
$t_{p\_X3 \rightarrow OUT}$ = 228.465 ps	A = 409.5µm^2	Layout E = 0.74 pJ	DRC: Y
t_p = 286.242 ps	AR = 1.078		LVS: Y

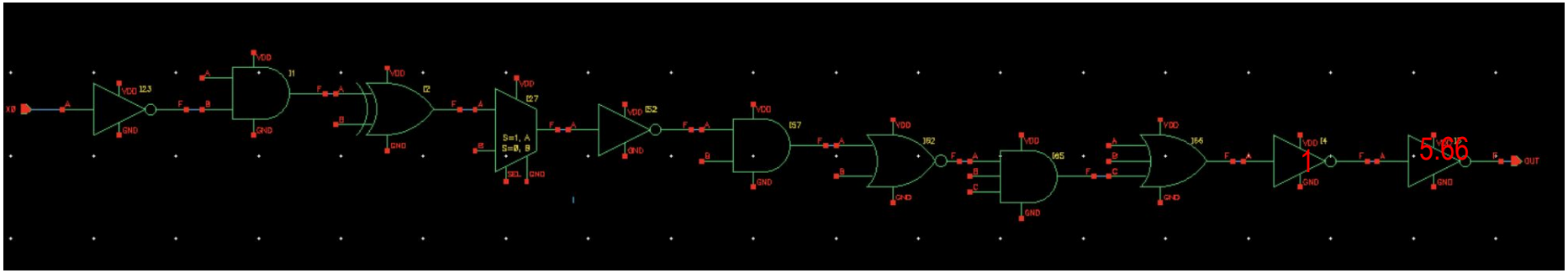
Critical Path Analysis

- **Block Diagram of Design**



Design Optimization

- Gate level critical path

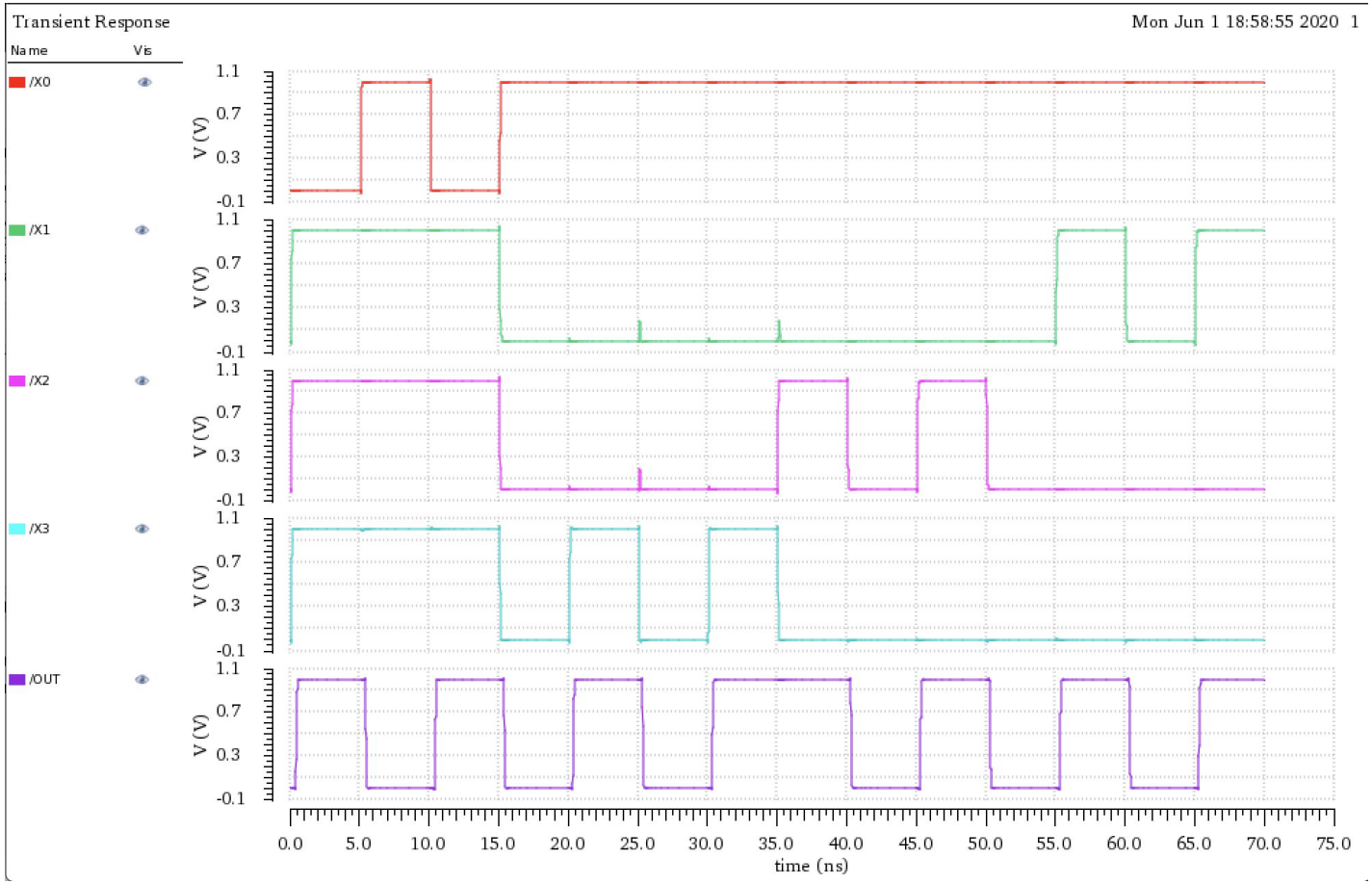


- MOS detail of gates, optimizations, and sizing strategy

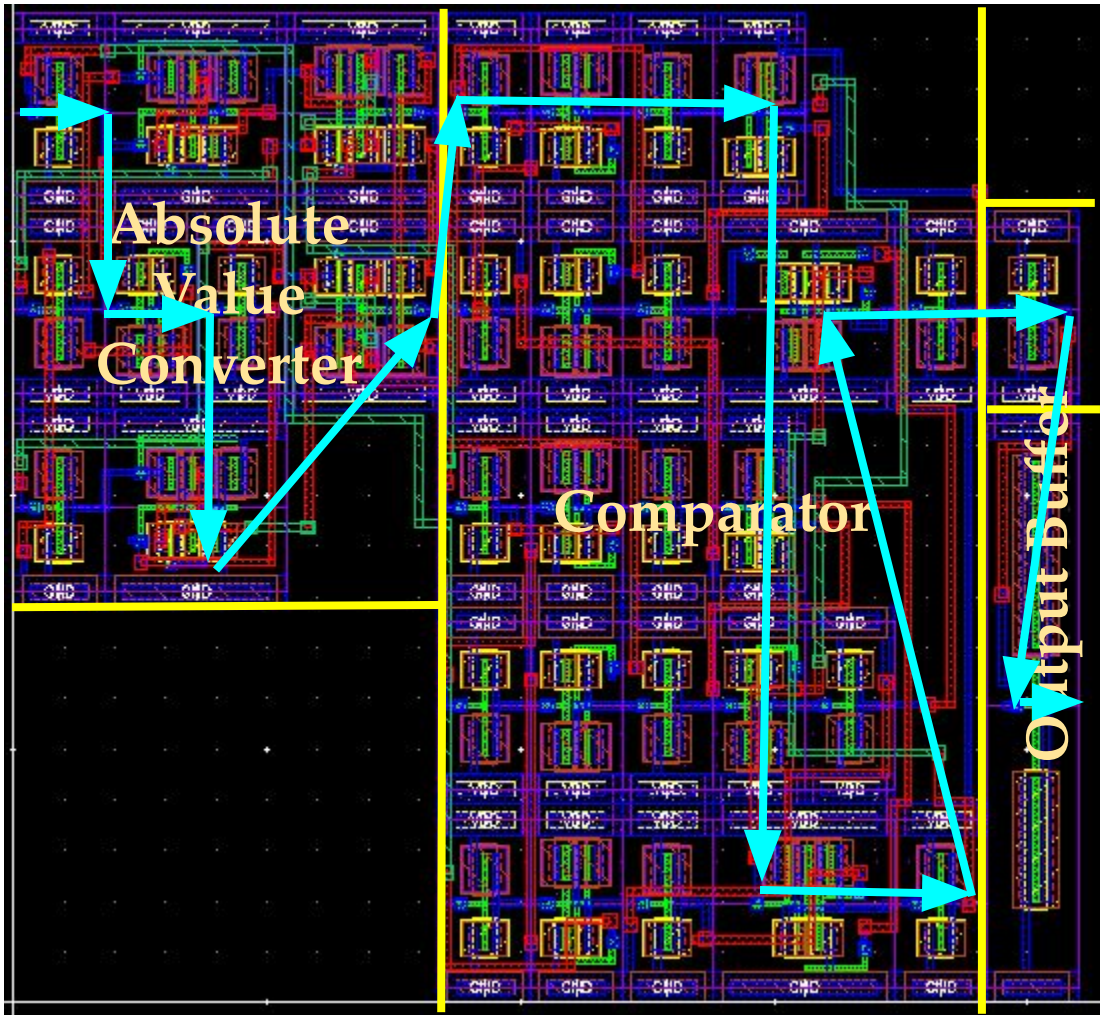
- Efficient logic design for 2's complement converter without a complex mirror adder structure
- Pass-transistor logic used for MUX and XOR to reduce overall circuit energy
- Output buffers used to isolate fan-in from fan-out and improve propagation delay

Functionality Check

- Relevant waveforms (input to output paths)



Absolute-Value Detector Layout



Size

Y = 19.5 µm

X = 21 µm

AR, Area

Aspect ratio: 1.078

Area: 409.5 µm^2

Density

Density: 82.7%

Discussion

- **Three most important features of your design**
  - Efficient Logic Structure with reduced fan-in for reduced layout area and improved propagation delay
  - Isolated Fan-in from Fan-out through the use of Output Buffers
  - Usage of pass-transistor logic for reduced power consumption

- **Given another chance, 3 things you would do different**
  - Improve propagation delay by further sizing analysis
  - Optimize critical path by analyzing transistor ordering
  - Improve layout design for reduced area and optimized critical path traversal