Printed Circuit Board Design, Measurement and Simulations (May 2022)

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***Abstract*— The purpose of this project was to design a Printed Circuit Board (PCB) whose channel provides the best signal quality with the minimum power supply noise. The software PADS provided the tools used to create the layers for the PCB layout. Additionally, the LineCalc feature from the ADS software was used to calculate the thickness of the traces used in PADS. After completing the layout, the Gerber files were obtained and sent to a free Design for Manufacturing (DFM) service to check for errors. Following the DFM check, measurements on the eye diagram at the far end of the signal line and power supply noise were done on the assembled PCB model. The results of these measurements were favorable as the height of the eye diagram proved minimal noise and jitter. These results were compared to the results obtained simulating the power delivery network (PDN) on the software ADS (Advanced Design System). Calculations of the network's RLC's were obtained through the PDN tool provided. This design was translated into a circuit in ADS that utilized the Input/Output Buffer Information Specification (IBIS) driver model. The resulting measurements of the eye height and jitter in these simulations' present slight deviations to the measurements done on the PCB.**

***Key Words*— Decoupling Capacitance, Eye Diagram, Jitter, PCB, PDN, Target Impedance, Signal Quality**

I. Introduction

THE field of electronic system packaging faces numerous obstacles on the pursuit of improving the performance of IC's in order to transmit high-quality signals, with minimal losses and noise distortions[1]. Designing and packaging electrical equipment that have the correct clock timing implementation is crucial for the overall performance of the equipment. Data can be lost if the proper signal timing is not enforced, conducing to poor and underwhelming performances. Additionally, during transmission of data, parasitic capacitances, crosstalk, signal reflections, skew, and jitter can affect the signal in the IC. To address these and other types of problems encountered in electrical packaging, engineers have sought out to employ different techniques that minimizes the effects of these obstacles. For example, designing an H-Tree clock distribution network [2] with matching impedances provided the ability of reducing the amount of crosstalk, skew, and reflections during the transmitter/receiver interactions. This technique mostly focuses on preserving signal transmission and integrity, but it does not do much when it comes to preserving power integrity. Voltages and current drops greatly affect the switching of transistors in IC's, reducing the signal speed and provoking the equipment to malfunction. On the onset of this problem, power delivery engineering was born.

When transistors in IC's draw current, the interconnects cause a DC voltage drop, leading to a DC offset. Additionally, AC noise is caused by the interconnects due to inductance provoking extra voltage drops, noise distortion, jitter, and overall power losses in the performance of the device. Power delivery engineering [3] has the goal of keeping the power supply voltage as close to V_{dd} , providing clean DC voltage with the required current to the switching transistors and reducing voltage drops and reduced noise. Within these recurrent events lies the motivation of the project; designing a PC board that can support 500 MHz signaling with minimal signal jitter and power supply noise. To create the layout of the PCB, the software PADS was utilized. Once the layout design passed inspection, the board was physically assembled with the purpose of conducting measurements of its eye diagram at the far end of its signal line. To compare the results obtained from the PCB, simulations of the power delivery network were done using ADS. This power delivery network was to be designed with the goal of obtaining its eye diagram [4], which helps to indicate the best point of sampling, as well as divulge the signal-to-noise ratio (SNR) at the sampling point, and measure jitter and distortion. To reduce the amount of noise on the signal in the simulations, a PDN tool calculator was used, which allowed for the calculation of the target impedance Z_T [5]. This tool also had the capability of calculating the equivalent series inductance/resistance of each decoupling capacitor, the equivalent parallel plate capacitance, and the amount of RLC branches needed on the PDN design. This project prepares future engineers with the tools and techniques that follow the present trend of the technology markets: improving the quality of signals while maintaining minimal losses of power and data during transmissions.

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II. Design

A. PCB Layout: LineCalc

The PCB to be designed is a 4-layer PC board that supports signaling at 500 MHz. The board was to have a 4:4 high speed buffer for test. The stack-up information pertaining the design of the PCB was provided. The design consisted of a top and bottom routing layer. The plane layers were distributed as follows: layer-2=PWR, layer-3=GND. The impedance of the design was set to 50 Ω. Additionally, the specifications for the relative permittivity and loss tangent of the dielectric were as follows: $\varepsilon_r = 4.5$, and tand = 0.025 respectively. This information, together with the dimensions of the thickness of the layers was the information needed to use LineCalc [6] and calculate the trace width of the transmission lines of the PC board.

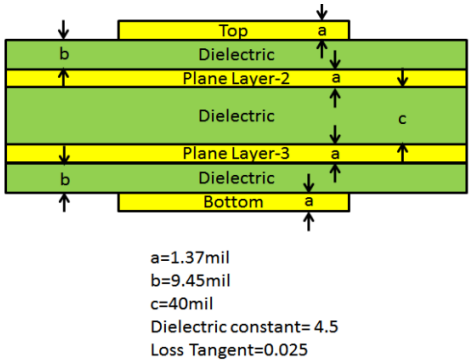

Figure 1. Stack-up information for the PCB design.

On LineCalc, the following parameters were specified:

LineCalc Parameter	***Value***
T	a = 1.37 mil
H	b = 9.45 mil
Cond	5.8×10^7
Frequency	500 MHz
Z_0	50 Ω

Figure 2. LineCalc parameters to calculate width of trace for transmission lines.

The parameters that were not mentioned were left with their default value. The result of the previous calculation resulted in a trace width of 16.412 mil. Calculating the right trace width corresponding to the specified characteristic impedance is important to maintain the signal integrity and its electronic response. After acquiring the width of the transmission of the lines, the design of the PCB layout can begin.

B. PCB Layout: Schematic

Once the trace width had been calculated, the designing of the PCB layout was initiated. The schematic containing the connections among the IC's and components were provided. The components on the left side of the schematic represent the signal inputs which are to be connected to the input pins on the chip designated as "U1". The components on the far right are the outputs, who are, in turn, connected to the output pins of U1.

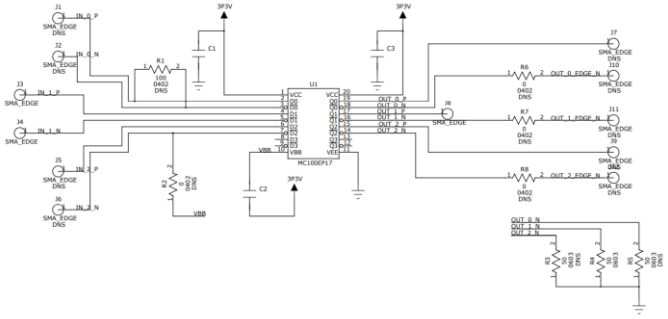

Figure 3. Schematic of the PCB layout.

Capacitors $C_1, C_2,$ and C_3 correspond to the decoupling capacitors that are to be implemented on the power delivery network simulations later. The resistor network on the bottom right correspond to the termination impedances of the lines. The pins J13 are where the power is connected to the power/ground plane, and J14 is the test point to check during the measurements for the eye diagram.

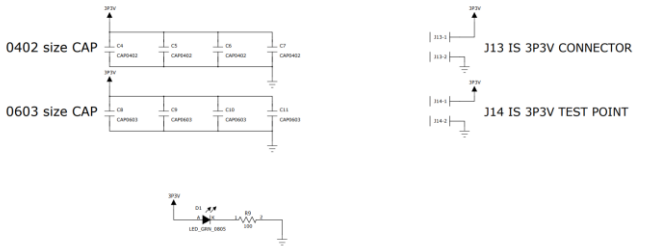

Figure 4. Decoupling capacitor networks.

Once understanding of the schematic was achieved, the next step was to create the layout using the software PADS.

C. PCB Layout: PADS

The previous schematics determine the design layout to follow when using PADS. Initially, the layout provided contain the dimensions of the board and within the SMA I/O components, as well as the U1 chip. The rest of the components were positioned outside the board with the purpose of being implemented on the layout following the convention of the schematic.

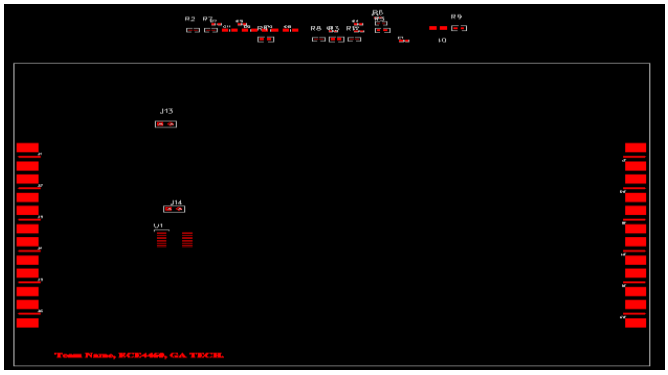

Figure 5. Initial PADS layout of PCB.

With the trace width already calculated, the settings of the

PADS were altered so that all traces were automatically set to 16.412 mils.

The input/output components followed the following convention: GND (box), Signal (lines), GND (box). This is relevant information for commencing routing of the components. The position of the components on the layout closely follows those in the schematic. When tracing, 90˚turns were avoided in favor of 45˚turns. The top layer was used to connect the inputs and outputs to their corresponding pins, as well as resistors and capacitors. This was done so because later in the design the incorporation of vias will connect the power and GND layers correspondingly.

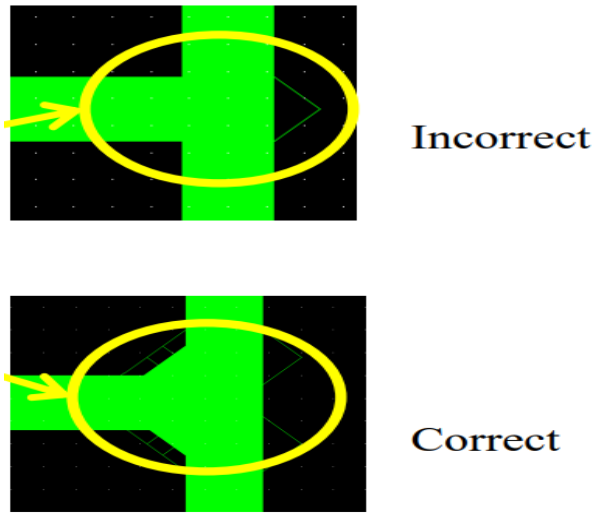

Figure 6. Example of 45˚trace turns.

When routing, crossing traces was avoided completely to reduce crosstalk. Additionally, the lengths of the traces were to match as close as possible; line length matching helps preserve the integrity of the signal and thus improves the performance of the device. To do this, PADS allows the traces to be selected individually to retrieve their lengths.

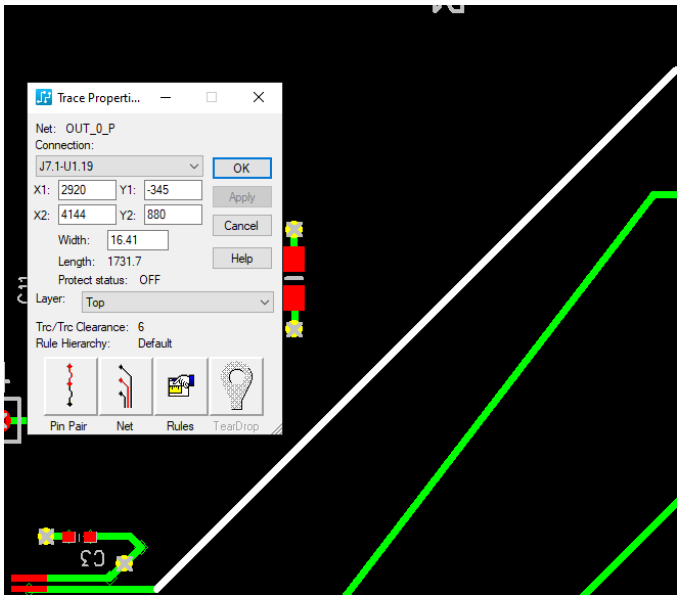

Figure 7. Properties of section of trace with corresponding length.

Once all the lengths are obtained, they are added up, and the total length of the trace is obtained. It is pertinent to point out that the length matching was implemented as follows: positive input signal J1-D0 (pin 2 of U1) must match the total length of the negative input signal J2-D0 (pin 3 of U1). The remaining input/output connections (D1, D2, Q0, Q1, Q2) mimic the same process as connection D0. Line matching, together with matching terminations [7] help reduce reflections of the signal, allowing for a voltage waveform that is above a set threshold voltage at the receiver.

Vias were used to connect the layers of power and GND to their corresponding components. Using vias allows for the ability to save tracing more transmission lines between the planes, but it increases the chances of reflections, discontinuities, losses, and crosstalk [8], degrading the quality of the signal. Given this fact, the usage of vias was limited as much as possible. On the design, vias were constrained mostly to connecting the signals and outputs to GND and power. Once the vias were connected, the PCB layout was completed, and the verification process begins.

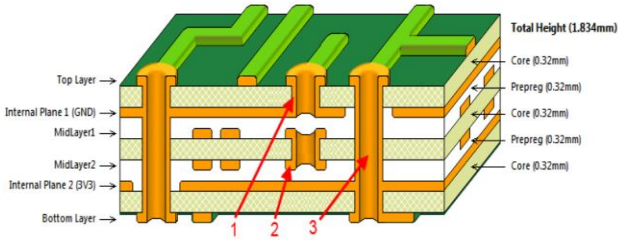

Figure 8. Example of vias interconnecting layers.

D. PCB Layout: Design Verification and DFM Check

Once settled on the final layout of the PCB, the design was submitted to clearance and connectivity checks. After passing both checks without errors, the design should be ready for manufacturing.

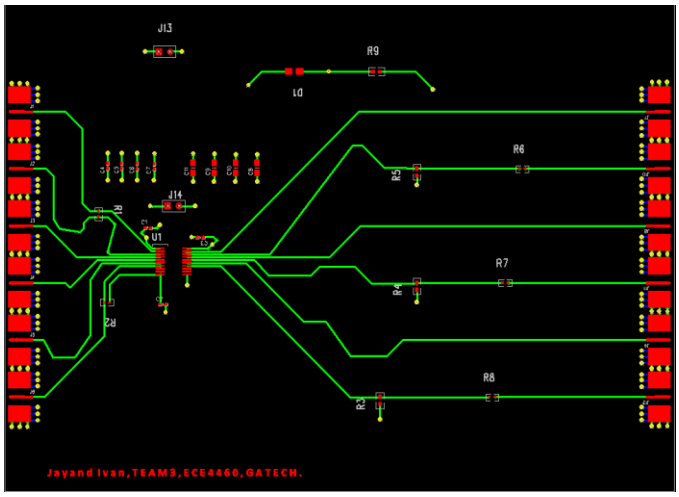

Figure 9. Final layout of the PCB.

To verify this is the case, PADS gives the option of downloading the Gerber files of the layout. These Gerber

files are the ones sent to the manufactures of the PCBs, and they contain the specification of the design. Once the Gerber files were obtained, they were uploaded to the GerberView software which provided a more detailed look into the layer and interconnections of the PCB layout. Once determined that there were no interconnections misplaced, misaligned, or crossing traces, the Gerber files were compiled one last time and submitted to the free DFM check site “my4pcb.com”.

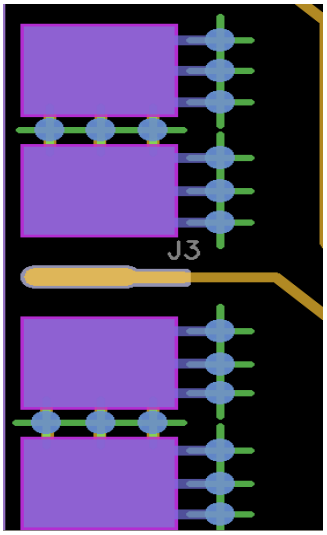

Figure 10. Gerber file view showing no misalignments of vias and connections.

After the site performs the check on the Gerber files, it sends the results giving it clearance for manufacturing.

What FreeDFM found on your design

Show Stoppers

We Found None!

Problems Automatically Fixed

Insufficient Inner Layer Annular Ring (4 violations)	1 2 3 4
Insufficient Silkscreen Line Width (56 violations)	1 2 3 4 5

Figure 11. DFM check results of the PCB layout.

With this result obtained, the design meets the requirements for fabrication, and finally, assembly.

E. PCB Assembly and Measurement Results

Once the board was manufactured and received, it was ready to assemble. All components on the schematic and layout were put together on the board following the design created on PADS. Once the assembly was completed, the PCB was connected to an oscilloscope to perform measurements on the eye diagram at the far end of the signal line and power supply noise when transmitting a pseudorandom binary sequence (PRBS) at 500 MHz.

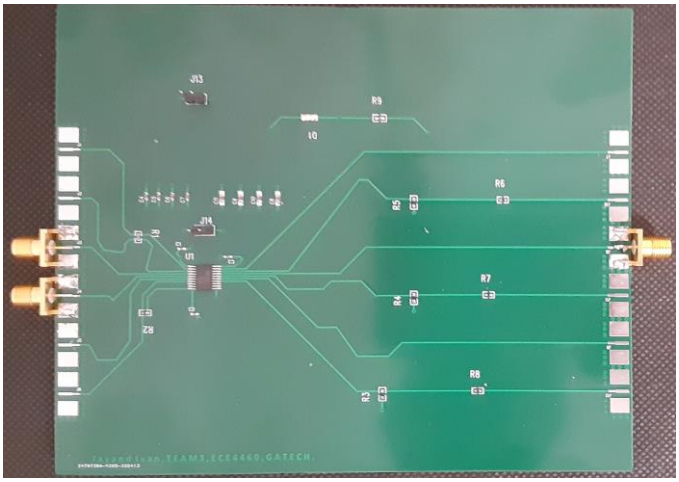

Figure 12. Assembled PCB.

The eye diagram [4] is useful to understand the signal quality of data waveforms. They indicate the best point for sampling, measuring jitter, and can divulge the signal-to-noise ratio of the waveform.

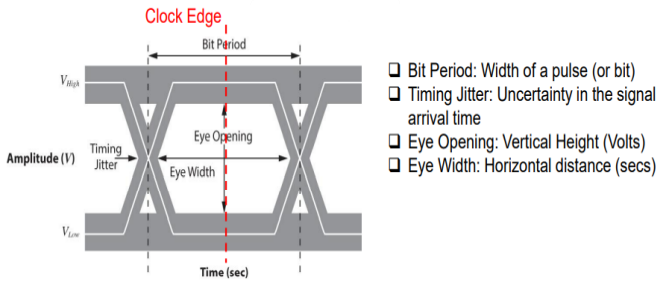

Figure 13. Example of ideal eye diagram and its components.

The results obtained from the eye diagram analysis performed on the PCB showed measurements that are close to those encountered in ideal eye diagrams. The eye height, or amplitude between the zero and one level of the eye, measured was 0.767 V.

Figure 14. Eye diagram measured of the PCB.

Additionally, measurements on the peak-to-peak jitter and signal-to-noise ratio obtained from the test performed on the

PCB demonstrated acceptable results. The peak-to-peak jitter, which measures the difference between the longest and shortest cycle of the clock, was 0.066 ns. This result is close to the ideal case of 0 s. The peak-to-peak power supply noise amplitude was measured at 13.3 mV, and the SNR (signal-to-noise ratio) was 5.64 mV.

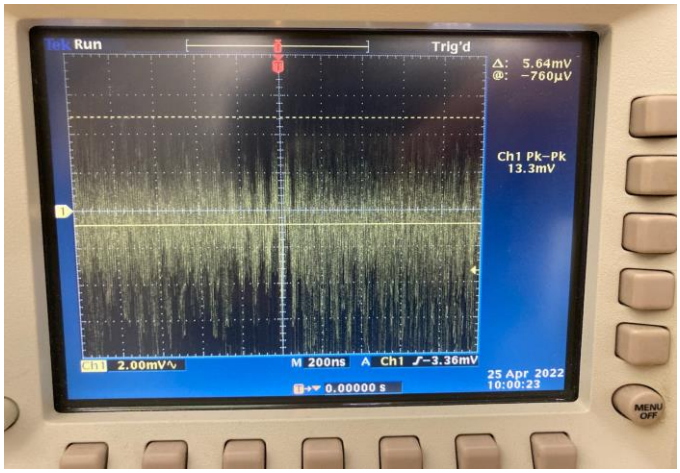

Figure 15. PCB measurement of SNR and p-p power supply noise amplitude.

The results obtained from testing the PCB are summarized on the following table:

Measurement	Value	Unit
Eye Height (Amplitude)	0.767	V
Peak-to-Peak Jitter	0.066	ns
Peak-to-Peak Power Supply Noise Amplitude	0.013	V
SNR	0.005	V

Figure 16. Summary of results obtained from PCB test.

These results prove favorable for the design and layout of the PCB; it demonstrates minimal power supply noise degrading the quality of the signal, and an amplitude that is close to the ideal 1 V. Other aspects of the eye diagram that shows the quality of the design is the eye crossing percentage [9, p.5-6], which provides a clear indication of how well the system's data pulse symmetry is performing. Ideally, the crossing percentage should be at 50%, which the eye diagram clearly exhibits. Based on the measurements obtained, the design of the PCB was successful in achieving its goals and requirements.

F. ADS Simulations Results

The model used to simulate the printed circuit board can be seen in the following image.

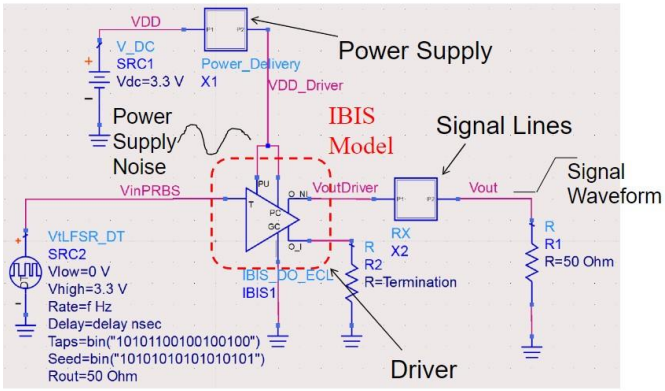

Figure 17. Circuit Schematic Used to Represent the Printed Circuit Board

In this schematic, a differential driver is used, with one of its ends terminated, to create a single ended driver. A pseudorandom bit stream is supplied to the input of the chip, which is represented by an IBIS model.

The power delivery network shown can be represented by either a one- or two-dimensional model. In this simulation, the one-dimensional model was utilized due to time constraints. The schematic for the model can be seen in the figure below.

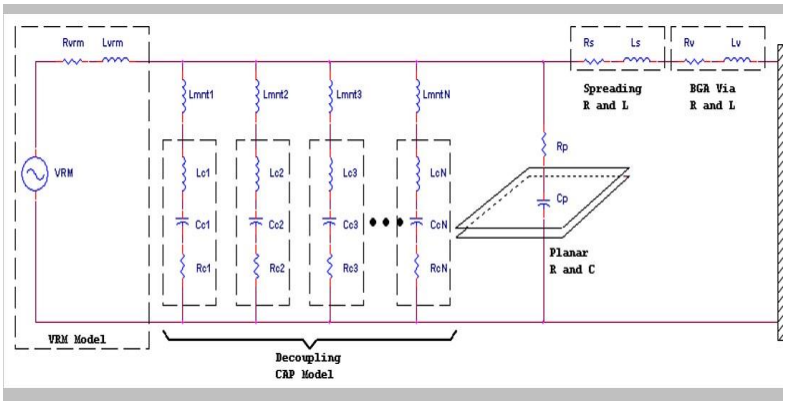

Figure 18. Schematic For the Power Delivery Network Used for the one-dimensional model

The focus of the simulations conducted was to measure the signal noise and generate the eye diagrams to analyze jitter and distortion.

There were two different circuit models created for the simulation, one of which incorporated decoupling capacitors, and the other that did not. The purpose behind integrating decoupling capacitors into a circuit is to ensure that the actual impedance does not exceed the target impedance before the target frequency is reached. As capacitors have different resonance frequencies depending on their value, specific combinations will be capable of decreasing the impedance, but this applies only at lower frequencies.

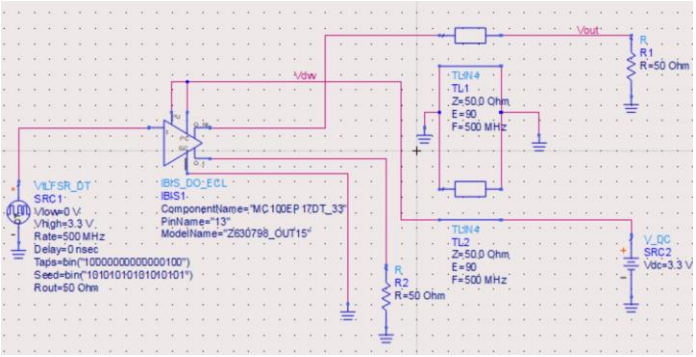

Figure 19. Ideal Model of Schematic Without the Use of Decoupling Capacitors

The image above is the schematic representation created without the use of decoupling capacitors to model the printed circuit board. Simulations were completed to measure the power supply noise as well as generate the eye diagram, which can be seen in the proceeding figures.

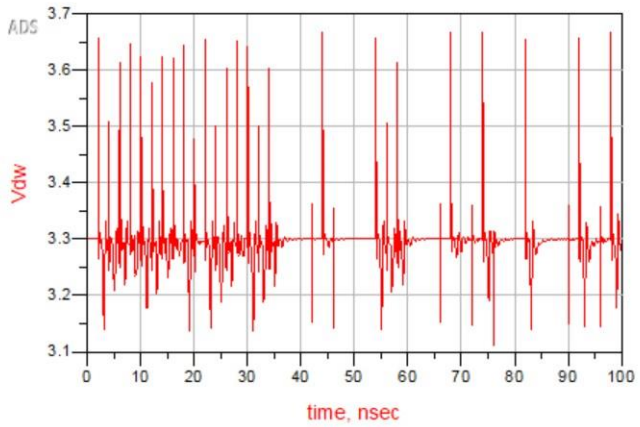

Figure 20. Power Supply Noise plot of Ideal Circuit Schematic

In this figure, the power supply noise varies from approximately 3.1 volts to 3.7 volts. The amount of noise present is significant as the voltage magnitude consistently fluctuates about 0.6 volts, which presents problems as a constant voltage is desired.

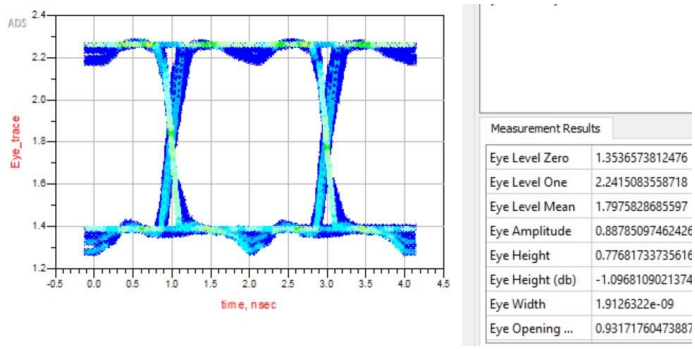

Figure 21. Eye Diagram For Schematic Without the Use of Decoupling Capacitors

This graph showcases an eye diagram with a mean of about 1.8, a height of 0.77, and a width of about 1.91 nanoseconds.

The eye jitter, peak to peak, was found to be 84.3 picoseconds and the jitter RMS was 19.01 picoseconds.

The second simulation that was completed incorporated the power delivery network and decoupling capacitors to reduce the power supply noise as well as produce an eye diagram with less distortion and jitter. The following schematics were used to create the model for the printed circuit board.

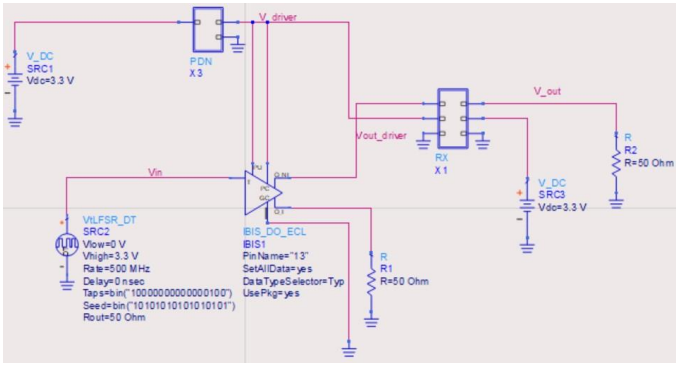

Figure 22. Circuit Schematic for Model Incorporating Decoupling Capacitors

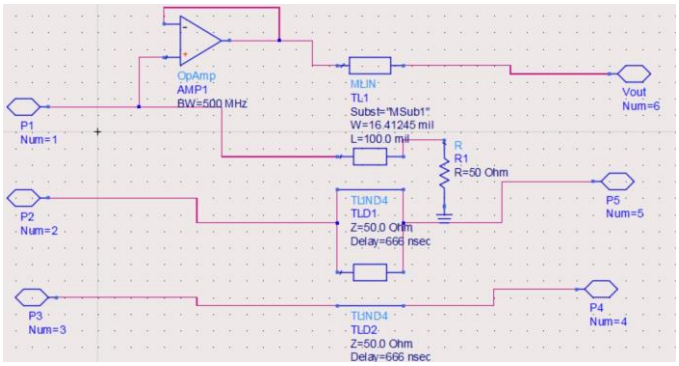

Figure 23. Signal Distribution Network

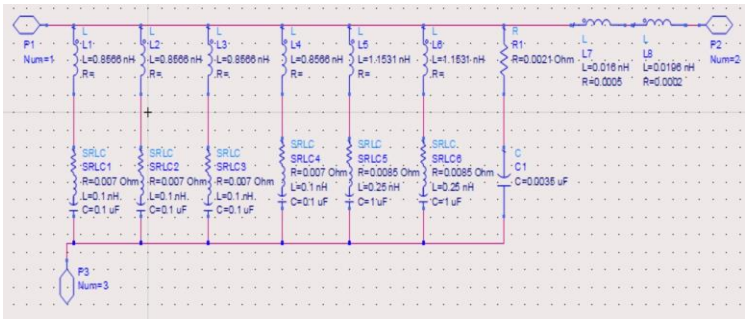

Figure 24. Power Delivery Network

The decoupling capacitors can be seen in parallel, each represented as a RLC circuit. The values for the decoupling capacitors used for the power delivery network can be found in the proceeding table.

Capacitor Value	0.1 uF	1 uF
Number of Capacitors	4	2
Equivalent ESR	0.007 ohms	0.0085 ohms
Equivalent ESL	0.1 nH	0.25 nH
Equivalent Lmnt	0.8566 nH	1.531 nH

Figure 25. Values of Decoupling Capacitors

These values were obtained through using a PDN tool provided by Altera in which specific values for the target impedance and frequency can be inputted and the corresponding values for the capacitors could be found using the provided library. The equations for the target impedance and resonance frequency are listed below:

$$Z_T = \frac{V_{DD} * ripple}{I_{max} * TransientCurrent} \quad (1)$$

$$f_r = \frac{1}{2\pi\sqrt{LC}} \quad (2)$$

The ideal combination that was found used four 0402 0.1 uF capacitors and two 0603 1 uF capacitors.
All other values obtained in the power delivery network, such as the plane capacitance and resistance, were also found using the same provided Excel spreadsheet as well as the dimensions of the PADs layout.
After having obtained the necessary values for the decoupling capacitors, the simulation was performed, and the following results were obtained.

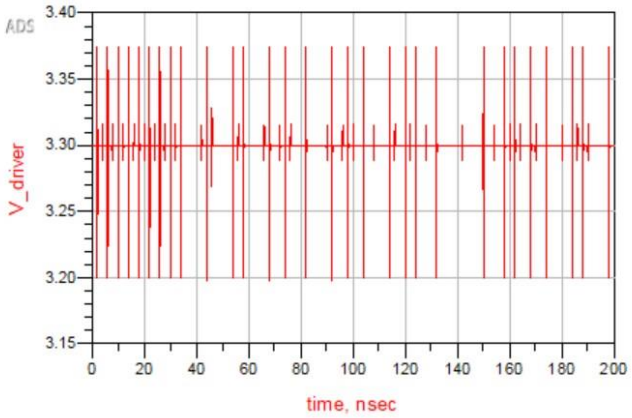

Figure 26. Power Supply Noise for Schematic Incorporating Decoupled Capacitors

In the image above, the noise ranges from a magnitude of about 3.2 volts to about 3.37 volts. Considering that the supply voltage is 3.3 volts, while the difference is noticeable, it is much less significant compared to the results obtained in figure 20. The noise range has been reduced substantially from 0.6 volts to less than 0.2 volts.

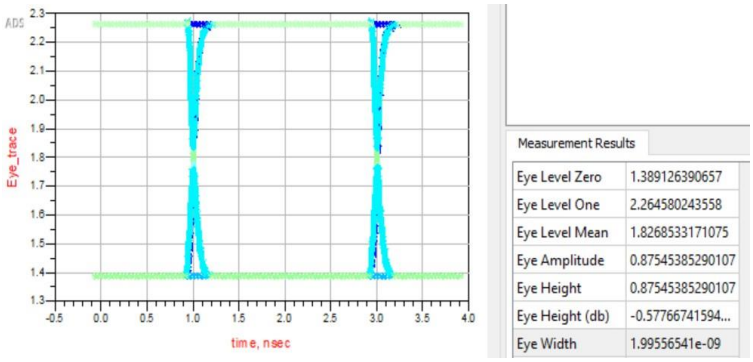

Figure 27. Eye Diagram After Incorporating Capacitors

When comparing the eye diagram to the previous simulation performed in figure 21, there is a very clear difference in the waveforms as, visually, the amount of distortion has decreased by a large margin and the jitter has clearly decreased as well. The measured values are listed here:

- Eye height: 0.875
- Eye level Mean: 1.827
- Eye jitter peak to peak: 8.869 picoseconds
- Eye jitter RMS: 4.468 picoseconds

When comparing these values once again to figure 21, there is noticeable improvement in all the categories. Jitter has decreased drastically by about 80 picoseconds and the eye height has increased, accomplishing the goal set out by incorporating decoupling capacitors into the simulation model.

G. Model to Hardware Correlation

The results obtained from the PCB test and the ADS simulations on the power distribution network were collected and compared. The following table contains a summary of the results:

Measurement	PCB Value	ADS Value	% Difference
Eye Height (Amplitude)	0.767 V	0.875 V	13.15%
Peak-to-Peak Jitter	66.0 ps	8.869 ps	152.616%
Peak-to-Peak Power Supply Noise Amplitude	0.013 V	0.016 V	20.69%
SNR	0.005 V	0.002 V	85.7143%

Figure 28. Table Outlining Values Obtained from the Simulation and Actual Measurement of the Printed Circuit Board

The differences between the results from the PCB testing and the simulations are noticeable. Discrepancies between the physical measurements and the simulations are likely due to the limitations of the one-dimensional model utilized for the power delivery network. As seen in the table above, the values that were obtained using the ADS simulation, apart from the peak-to-peak noise amplitude, were more favorable than what was measured from the printed circuit board. Since the one-dimensional model does not fully capture or represent the actual structure of the power delivery network, it would not incorporate the appropriate number of parasitic resistances that would be present during actual measurements. To obtain a

more precise representation of the PCB, a two-dimensional model could have been made, but for the purpose of this project, the one-dimensional model is accurate enough to simply obtain reasonable estimations for the predicted results of the PCB.

Although the simulations do not fully match the measurements obtained for the board, the physical performance of the PCB is suitable. The obtained supply noise levels are very low with a value of 5 millivolts and the peak-to-peak jitter and eye height are both respectable values. So, although the PCB did not perform as well as had been predicted by the simulations, the actual measurements obtained were still satisfactory and it is probable that the simulation performed obtained values that were too close to ideal to be expected.

III. Conclusion

The assembled PCB's performance was acceptable. In an ideal case, the eye height or amplitude should have a value of 1 V (distance between V_{LOW} and V_{HIGH}), while maintaining the peak-peak jitter close to 0 s. The measurements on the eye diagram obtained from the designed PCB showed that the board maintain an eye amplitude of approximately 0.8 V, with a peak-to-peak jitter of 0.066 ns. This implies that the board's signal quality, at 500 MHz, was somewhat comparable to those encountered in ideal performative conditions. The design of the simulated power distribution network also demonstrated favorable results. The measurements obtained from the eye diagram were 0.875 V for its amplitude, and 8.869 ps for the peak-to-peak jitter. Outcomes of both the physical PCB and the simulated power distribution network are substantially different, yet both of their performance capabilities meet the requirements of the design. Incorporating the parasitic series resistances and inductances into the power distribution network proved to be key in obtaining comparable results between both design approaches. The technique of keeping the response of the system below a set target frequency and impedance was instrumental in keeping the quantity of components of the network on a minimum without compromising performance.

Although the overall results obtained on the experiment are commendable, there are areas of improvements that can be addressed. Using a one-dimensional model for the PDN provides fitting results, but it presents limits in translating the entirety of the parasitic resistances real-life electric components experience. Using a two-dimensional model for the PDN should ameliorate this limitation of the design and provide more accurate measurements. Real-life devices are limited to the computational power and techniques available at the time. Additionally, resistance to the flow of heat through the leads, layers and transistors in devices result in heat generation [10] that can cause poor or failing performances. Incorporating a model that can translate this issue into the simulations of the PDN can improve the accuracy in design and execution of electrical components. Addressing these and other possible limitations is well within the present scope of power delivery engineering, and new developments on these subjects can be expected soon.

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