# **ECE 342: Electronic Circuits (Spring 2020)**

Department of Electrical and Computer Engineering University of Illinois at Urbana-Champaign

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# Homework 11 (Assigned: 4/24/2020; Due: 5/6/2020, 11:59pm)

1. Plot the loop gain Bode plot for the feedback systems with the following open-loop gain  $H_{OL}(s)$  and feedback factor f. Determine loop-gain phase margin for all parts.

(a) 
$$H_{OL}(s) = \frac{100}{1 + \frac{s}{10^5}}$$
;  $f = 1$ 

(b) 
$$H_{OL}(s) = \frac{200}{(1 + \frac{s}{10^4})(1 + \frac{s}{10^6})}$$
;  $f = 1$ 

- (c)  $H_{OL}(s)$  same as (b); but with f = 1/2
- (d)  $H_{OL}(s)$  same as (b); but with f = 1/4

(e) 
$$H_{OL}(s) = \frac{1000}{s(1 + \frac{s}{100})}$$
;  $f = 1/10$ 

- (f)  $H_{OL}(s)$  same as (e); but with f = 1/2
- (g)  $H_{OL}(s)$  same as (e); but with f = 1

2. Design the CMOS realization of the boolean expressions shown below.

(a) 
$$Y = \overline{A \cdot (B + C)}$$

(b) 
$$Y = \overline{(A + (B \cdot C))}$$

(c) 
$$Y = A \cdot B$$

(d) 
$$Y = A \cdot \overline{B + C}$$

(e) 
$$Y = \overline{A \cdot B + B \cdot C + C \cdot A}$$

(f) 
$$Y = \overline{((A \cdot B) + C) \cdot (D + E)}$$

(g) 
$$Y = \overline{((A+B)\cdot C + D\cdot E)}$$

(h) 
$$Y = \overline{A + B + C}$$

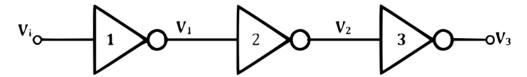
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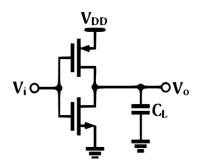
### 3. Consider the Inverter chain below:



Each inverter is identical to the others with  $V_{OH} = 1V$ ,  $V_{OL} = 0V$ ,  $NM_L = 0.3V$ ,  $NM_H = 0.5V$ .

- (a) Sketch a piecewise linear plot of the VTC(Voltage Transfer Function).
- (b) True of False: if  $V_i = V_{OL} + v_n$  with  $|v_n| < NM_L$ , then output  $V_3 = V_{OH}$ .
- (c) Determine  $V_3$  if  $V_i = V_{OL} + 0.4V$ . Is the output  $V_3$  correct? Does  $V_3 \in \{V_{OH}, V_{OL}\}$ ?
- (d) Determine  $V_3$  if  $V_i = V_{OL} + 0.45V$ . Is the output  $V_3$  correct? Does  $V_3 \in \{V_{OH}, V_{OL}\}$ ?
- (e) Which of the parts (b), (c), (d) demonstrate the noise-immunity property of the digital gates?
- (f) Which of the parts (b), (c), (d) demonstrate the restorative property of the digital gates?

### 4. Consider the CMOS inverter below:



Assume  $V_{DD}=5V,\,k'_n=150\mu A/V^2$  ,  $k'_p=75\mu A/V^2$  ,  $(W/L)n=1,\,V_{THp}=-0.5V,\,V_{THn}=0.7V,\,C_L=0.5pF.$ 

- (a) Determine the values of (W/L)p such that  $V_M$  is 2.5V, 1.5V and 3.5V.
- (b) If (W/L)p = 2, determine  $V_M$ ,  $t_{PLH}$ ,  $t_{PHL}$ , and the dynamic power dissipation  $P_D$  when operating at maximum switching frequency  $(P_{Dmax})$ .
- (c) If (W/L)p = 4 and (W/L)n = 2, then relative to your answer in part (b), how will  $V_M$ ,  $t_{PLH}$ ,  $t_{PHL}$  and  $P_{Dmax}$  change?