JN5169-001-M06-2

WiSN v5.0.0

Pin Assignment

Module Pin	Pin Function: Primary	Alternate Fucntion						Type	Signal Type	Description		Project WIRE NAME	DESCRIPTION		DEVICE Pin	DEVICE Name		Note	Connected to ...	Note 2
1	ADC1							I	3.3V	Analogue to Digital Input	←	ADC0 / ADC0_OUT	ADC 0-30V input on NEMA-pin4	←	Res.Divider (R601, R602, C601, D13) <- ADC0_IN <- P100.pin4		←	**Vjennic_adc_max = 2.4V**	**NEMA Socket Pin4**	Vnema_adc_in_max = 30V
2	DO0	SPICLK				PWM2		O	CMOS	DO0; SPI-bus Master Clock Output; PWM2 Output	←	J4	Test Jumper J4					**JTAG programming mode:** must be left floating high during reset to avoid entering JTAG programming mode.		The JN5169 will enter JTAG programming mode if SPICLK (DO0) is low after RESET
3	DO1	SPIMISO				PWM3		I/O	CMOS	SPI-bus Master_In, Slave_Out input; PWM3 iutput	←	PROG_L				**PROG_HEADER**		**UART programming mode:** leave pin floating high during reset to avoid entering UART programming mode or hold it low to program.	**J3 - PROG HEADER**	The JN5169 will enter UART programming mode if SPIMISO (DO1) is low after RESET.
4	DIO18	SPIMOSI						I/O	CMOS	SPI Master Out Slave In Output	→	GPS_RESET_L	GPS Reset							
5	DIO19	SPISEL0						I/O	CMSO	SPI Master Select Output 0	←	GPS_TIMEMARK	GPS Time Mark							
6	DIO0	ADO	SPISEL1	ADC3				I/O	CMOS	DIO0; antenna diversity odd output, SPI Master Select Output 1; ADC input 3	←	ADC2 / ADC2_OUT	ADC 0-10V input (**feedback of 0-10V_CH1** output on NEMA-pin2)	←	Res.Divider (R605, R606, C603) <- ADC2_IN / 0_10V_CH1_OUT					
7	DIO1	ADE	SPISEL2	ADC4	PC0			I/O	CMOS	DIO1; antenna diversity odd output; SPI Master Select Output 2; ADC input 4; Pulse Counter 0 Input	←	ADC3 / ADC3_OUT / V12P0	ADC for 12V Rail monitoring	←	Res.Divider (R48, R49, C28) <- ADC3_IN / V12P0	12V Rail				
8	DIO2*		RFRX	TIM0CK_GT	ADC5			I/O	CMOS	DIO2, Radio Receive Control Output or Timer0 Clock/Gate Input	---	*NOT CONNECTED*	*** DO NOT CONNECT *****	---	---	*KEEP OPEN*	---	** This pin is not connected for JN5169-001-M06-2 modules.*		
9	DIO3*		RFTX	TIM0CAP	ADC6			I/O	CMOS	DIO3, Radio Transmit Control Output or Timer0 Capture Input	---	*NOT CONNECTED*	*** DO NOT CONNECT *****	---	---	*KEEP OPEN*	---	** This pin is not connected for JN5169-001-M06-2 modules.*		
10	DIO4	CTS0	JTAG_TCK	TIM0OUT	PC0			I/O	CMOS	DIO4, UART 0 Clear To Send Input, JTAG CLK Input, Timer0 PWM Output, or Pulse Counter 0 input	→	RELAY	Relay Driver	→	Q4.pin1 (MOS Gate) -> K901.pin3 (coil pin)	ALZ12B12				
11	DIO5	RTS0	JTAG_TMS	PWM1	PC1			I/O	CMOS	DIO5; UART 0 Request To Send Output; JTAG Mode Select Input; PWM1 Output; Pulse Counter 1 Input	→	PRST_L / EnergyMeter.RESET_L	Power Meter Reset	→	U1.pinXX (TCLT1003 OPTO) -> U1.pinXX -> U6.pin18 (RESET_L)	78M6610+PSU/B00				
12	DIO6	**TXD0**	JTAG_TDO	PWM2				I/O	CMOS	DIO6, UART 0 Transmit Data Output, JTAG Data Output or PWM2 Output	→	TXD0 / EnergyMeter.RX	Power Meter UART	→	U9.pinXX (TCLT1003 OPTO) -> U9.pinXX -> U6.pin13 (SDI/**RX**/SDAi)	78M6610+PSU/B00			**J3 - PROG HEADER**	
13	DIO7	**RXD0**	JTAG_TDI	PWM3				I/O	CMOS	DIO7, UART 0 Receive Data Input, JTAG Data Input or PWM 3 Output	←	RXD0 / EnergyMeter.TX	Power Meter UART	←	U10.pinXX (TCLT1003 OPTO) <- U10.pinXX <- U6.pin12 (SDO/**TX**/SDAo)	78M6610+PSU/B00			**J3 - PROG HEADER**	
14	**DIO8**	TIM0CK_GT	PC1	PWM4				I/O	CMOS	DIO8, Timer0 Clock/Gate Input, Pulse Counter1 Input or PWM 4 Output	→	LED_RED	Led RED	→	D14					
15	**DIO9**	TIM0CAP	32KXTALIN	RXD1	32KIN			I/O	CMOS	DIO9, Timer0 Capture Input, 32K External Crystal Input, UART 1 Receive Data Input or 32K external clock Input	→	LED_BLUE	Led BLUE	→	D101					
16	**DIO10**	TIM0OUT	32KXTALOUT					I/O	CMOS	DIO10, Timer0 PWM Output or 32K External Crystal Output	→	LED_GREEN	Led GREEN	→						
17	**VDD**							P	3.3V	Supply Voltage	---	**V3P3**	**VCC 3V3**						**J3 - PROG HEADER**	
18	**GND**							GND	0V	Digital Ground	---	**GND**	**GND**						**J3 - PROG HEADER**	
19	DIO11	PWM1		TXD1				I/O	CMOS	DIO11, PWM1 Output or UART 1 Transmit Data Output	→	PWM0 / DAC0_IN	PWM0 to 0-10V Channel 1	→	U801.pin3 (OP.AMP) -> U801.pin1 -> DAC0_OUT / 0_10V_CH1_OUT -> **P100.pin2 (NEMA)**	LM2904DGKR	→		**NEMA Socket Pin2**	
20	DIO12	PWM2	CTS0	JTAG_TCK	ADO	SPISMOSI		I/O	CMOS	DIO12, PWM2 Output, UART 0 Clear To Send Input, JTAG CLK Input, Antenna Diversity Odd Output or SPI Slave Master Out Slave In Input	→	LSW_EN	LOAD SWITCH Enable							
21	DIO13	PWM3	RTS0	JTAG_TMS	ADE	SPISMISO		I/O	CMOS	DIO13, PWM3 Output, UART 0 Request To Send Output, JTAG Mode Select Input, Antenna Diversity Even output or SPI Slave Master In Slave Out Output	←	IRQ_I2C_DEV_L	I2C Interrupt							
22	**RESETN**							I	CMOS	Reset input	←	RESETN	Reset			to R201/ C203			**J3 - PROG HEADER**	
23	DIO14	SIF_CLK	TXD0	**TXD1**	JTAG_TDO	SPISEL1	SPISSEL	I/O	CMOS	DIO14, Serial Interface Clock, UART 0 Transmit Data Output, UART 1 Transmit Data Output, JTAG Data Output, SPI Master Select Output 1 or SPI Slave Select Input	→	TXD1	GPS_UART / DEBUG_UART	→	gps_blk.UART_GPS_RX J2.1	to: gps_blk / debug_uart			**J2 - UART1 DEBUG**	
24	DIO15	SIF_D	RXD0	**RXD1**	JTAG_TDI	SPISEL2	SPISCLK	I/O	CMOS	DIO15, Serial Interface Data or Intelligent Peripheral Data Out	←	RXD1	GPS_UART / *DEBUG_UART*	←	gps_blk.UART_GPS_TX J2.3	from: gps_blk / debug_uart			**J2 - UART1 DEBUG**	
25	DIO16	SPISMOSI	SIF_CLK	COMP1P				I/O	CMOS	DIO16, Comparator Positive Input, Serial Interface clock or SPI Slave Master Out Slave In Input	→	I2C_SCLK / I2C_JENIC_SCLK	I2C Clock	→		U7 (KX122-1037 Accelerom) U15 (APDS-9300 Light Sensor) U14 (ATSHA204A Crypto SHA) U16 (MC24C32 EEPROM)			**J3 - PROG HEADER**	
26	DIO17	SPISIMO	SIF_D	COMP1M				I/O	CMOS	DIO17, Comparator Negative Input, Serial Interface Data or SPI Slave Master In Slave Out Output	← →	I2C_SDA / I2C_JENIC_SDA	I2C Data	← →		U7 (KX122-1037 Accelerom) U15 (APDS-9300 Light Sensor) U14 (ATSHA204A Crypto SHA) U16 (MC24C32 EEPROM)			**J3 - PROG HEADER**	
27	VREF	ADC2						P; I	3.3V	Analogue peripheral reference voltage or ADC input 2	←	ADC1 / ADC1_OUT		←				NOT USED!!		

* These two pins are not connected for JN5169-001-M06-2 modules.