Routing IRQ to CPU

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Question 1: Linking TG0 interrupt to Core 0 signal

✓ Correct!

Provide the name of the register used to allocated the Timer0 of TG0 to an interrupt signal on Core 0.

```
INTERRUPT_CORE0_TG_T0_INT_MAP_REG
```

Question 2: Interrupt registers base address

✓ Correct!

Provide the base address of the interrupt registers.

Hint: the answer is expected in hexadecimal

```
0x600C_2000
```

Question 3: Timer0 interrupt register offset

✓ Correct!

Provide the offset of the Timer0 of TG0 interrupt for Core0.

Hint: the answer is expected in decimal as you would use it in a macro definition.

```
50
```

Question 4: Timer0 interrupt register definition

✓ Correct!

Define in a *C* macro the register used to allocated the Timer0 of TG0 to an interrupt signal on Core 0.

```
#define INTERRUPT_CORE0_TG_T0_INT_MAP_REG REG(S3_INTERRUPT)[50]
```

Question 5: Allocating Timer0 interrupt to Core0 signal

✓ Correct!

Write *C* code allocating Timer0 of TG0 to the interrupt signal 19 on Core 0.

```
INTERRUPT_CORE0_TG_T0_INT_MAP_REG = 19;
```

Soumettre