Timer generated IRQ: Configuration register

Question 1: Configuration register of TG0

✓ Correct!

Provide the name of the configuration register of the Timer Group 0 (TG0) as found in the reference manual of the ESP32S3 SoC.

```
TIMG_T0CONFIG_REG
```

Question 2: Base address of TG0 registers

✓ Correct!

Provide the base address of the TG0 registers.

```
0x6001_f000
```

Question 3: Macro definition of TG0 configuration register

✓ Correct!

Define the TG0 configuration register in a *C* macro.

Suppose that the base address defined in Question 2 is defined in a macro called S3_TIMERGROUP0

```
#define TIMG_T0CONFIG_REG REG(S3_TIMERGROUP0)[0]
```

Question 4: Timer configuration

✓ Correct!

Which bit do you have to set in order to use *XTAL_CLK* and increase the timer counter?

Enter the bit positions as a list of numbers separated by a single space. Order them in increasing order (i.e. from LSB to MSB)

```
9 30
```

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