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| Department of computer science & Engineering  University of Nebraska—Lincoln |
| Processor Building |
| Computer Organization Project |
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| This document will detail the building a processor and the group interactions that occur during that time |

Contents

[1. Introduction 3](#_Toc497320003)

[1.1 Purpose of this Document 3](#_Toc497320004)

[1.2 Definitions, Acronyms, Abbreviations 3](#_Toc497320005)

[1.2.1 Definitions 3](#_Toc497320006)

[1.2.2 Abbreviations & Acronyms 3](#_Toc497320007)

[2. Component Description 3](#_Toc497320008)

[2.1 Processor Design 3](#_Toc497320009)

[2.1.1 Processor Testing Strategy 3](#_Toc497320010)

[2.2 Current abilities 4](#_Toc497320011)

[2.3 Speed overview 4](#_Toc497320012)

[2.3.1 Speed Testing Strategy 4](#_Toc497320013)

[2.4 Componentry 4](#_Toc497320014)

[3 Group Experience 4](#_Toc497320015)

# Introduction

This document will describe our group experience in building a processor from scratch and will include all the componentry contained within, how fast it operates at each point of the project, and its current capabilities of the processor.

## Purpose of this Document

This project is intended for us to learn the inner workings of a processor and how they function and interact with each other as we learn how to build a processor from scratch.

## Definitions, Acronyms, Abbreviations

### Definitions

Arithmetic logic unit – a circuit used to perform arithmetic and logic operations.

Clock – the number of pulses per second that set the speed for the processor the standard unit measurements are MHz (Megahertz, millions of pulses per second) or GHz (Gigahertz, billions of pulses per second).

Decoder – A device that takes a specified number of inputs and outputs multiple unique outputs for each input.

Instruction Register – holds the instruction that is currently being operated.

Multiplexer – A device that selects one of several inputs and forwards that to a single output.

### Abbreviations & Acronyms

ALU – Arithmetic logic unit

IR – Instruction Register

Mux – Multiplexer

PS – Program Status

XOR – Exclusive or

# Component Description

The following section will entail the components contained within the processor at each point, the speed overview of the processor at each point, and the current capabilities of the processor at each point in the project

## 2.1 Processor Design

Implement Later

### Processor Testing Strategy

Implement Later

## Current abilities

The current capabilities of the processor in part II of the can currently operate the following instructions; ADD, SUB, AND, OR, XOR. Additionally, You can

## Speed overview

During Part two of the project the observed clock speed of the processor is at 5 GHz. See figure 1 for a current graphical representation of the testing of the speed.

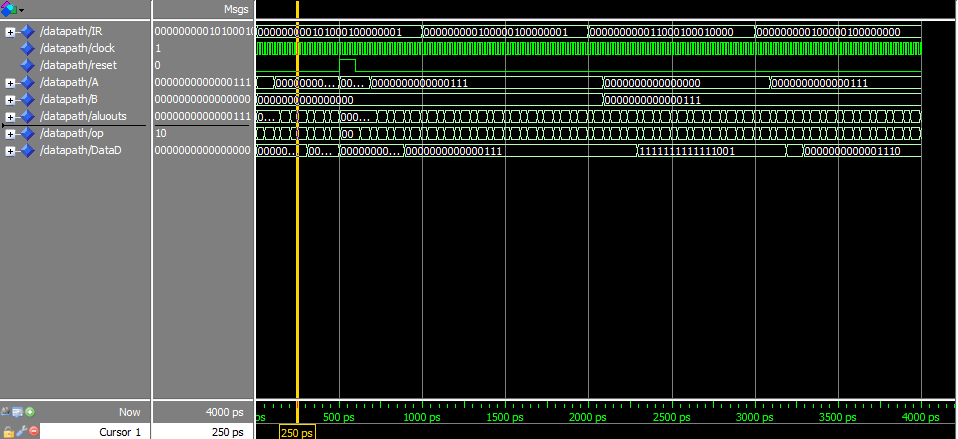


Figure 1: A graphical representation of the functioning of the processor as time progresses.

### Speed Testing Strategy

We tested our speed by using the model sim program. We first loaded a .do file containing varied test cases into the program and from there calculated the time required to operate.

## Componentry

The componentry currently contained within the processor are the following; Clock, Reset, Control Unit, Registers/Register file(s), ALU, Mux, Decoder, IR, PS (remains unused at present). Out of the components the clock and reset is automatically included as they already exist. There is are several 2-1, 3-1, and 16-1 Mux’s contained within the project so far, additionally there is a 4-16 decoder.

# Group Experience

At current the challenges in our group experience are setting up all the files in GitHub so that all project members have equal access to the files at any given time, which then comes with the challenge of making sure that all members remember to upload the updated version every time that anyone makes changes. Additionally, we had to update all of the components that we had created previously so that they would properly function together, which then led to the problem of our Mux’s not operating correctly, so we then had to adjust them solving the problems. As we began testing we had several problems regarding the operation of our processor which then led to another round of further adjusting and refining of each of the modules, so the processor could work. From there after we confirmed that it worked, we extensively tested the current processor to ensure that the processor could handle all the instructions it needs to handle at Part II of the project.