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| Department of computer science & Engineering  University of Nebraska—Lincoln |
| Processor Building |
| Computer Organization Project |
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| This document will detail the building a processor and the group interactions that occur during that time |

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# Introduction

This document will describe our group experience in building a processor from scratch and will include all the componentry contained within, how fast it operates at each point of the project, and its current capabilities of the processor.

## Purpose of this Document

This project is intended for us to learn the inner workings of a processor and how they function and interact with each other as we learn how to build a processor from scratch.

## Definitions, Acronyms, Abbreviations

### Definitions

Arithmetic logic unit – a circuit used to perform arithmetic and logic operations.

Clock – the number of pulses per second that set the speed for the processor the standard unit measurements are MHz (Megahertz, millions of pulses per second) or GHz (Gigahertz, billions of pulses per second).

Decoder – A device that takes a specified number of inputs and outputs multiple unique outputs for each input.

Instruction Register – holds the instruction that is currently being operated.

Multiplexer – A device that selects one of several inputs and forwards that to a single output.

### Abbreviations & Acronyms

addi – an assembly command that adds a specified value and a value in a register and stores that result in another register

ALU – Arithmetic logic unit

ARM – Advanced RISC Machines

b – branch to the location specified following this command

bal – branch and link, it’s an assembly command stores address of next instruction in 1st operator and then jumps to the address in the 2nd operator.

cmp – an assembly command that performs a comparison between two arguments by signed subtraction of 2ndarg – 1starg

IR – Instruction Register

jr – jump register

lw – load word

Mux – Multiplexer

PS – Program Status

RISC – Reduced Instruction Set Computer

sw – store word

xor – Exclusive or

# Component Description

The following section will entail the components contained within the processor at each point, the speed overview of the processor at each point, and the current capabilities of the processor at each point in the project

## Current capabilities

The current capabilities of the processor in phase IV are that it can currently operate all of the previously mentioned instructions listed. Additionally, the processor can handle ARM-like conditional instruction execution.

## Speed overview

During phase IV of the project the observed clock speed of the processor is around 3.8GHz.

### Speed Testing Strategy

We tested our speed by using the model sim program. We first loaded a .do file containing varied test cases into the program and from there calculated the time required to operate.

## Componentry

The componentry added during phase IV into the processor is the following items. The ability to have ARM-like conditional instruction execution in addition to adding I/O functionality, such as Slider switches, push Buttons, the 7-segment display, and the green LEDS. The addition of these components will require adjustments to the control unit, for the execution of the commands, as well as adding the I/0 interface in the data path.

# Group Experience

The following will detail the experiences that the group has encountered during each phase of the project.

## Phase IV

During phase IV the largest challenge that was faced was having all the I/O function as specified since implementing it appears straightforward but unexpected complications crop up and cause things to malfunction. After fixing all errors and ensuring that everything functions correctly, additional testing occurred and no further complications arose and testing was completed.