Verification Strategy:

For part 2:
For verification of part 2, I have enabled output on pin 7 of PORT C. I have also enabled CLK_OUT on pin 7 of PORT A. By toggling pin 7 of PORT C, I will be able to deduce the cpu frequency. I will then use the logic analyzer to compare it to CLK_OUT, which I have prescaled by a factor of 2. Since the toggle is inside a while loop, each period of the toggling output will be four clock cycles. Thus, if prescaler division does not affect the CPU, the difference in frequency will be a factor of eight, otherwise it will be a factor of 4.

For part 3:
Verification is trivial, as it is only the measurement of the frequency of the toggling pin (PC 7). This I can do with the oscilloscope.

For part 4:
Same as part 3, I can measure the frequency of CLK_OUT at PA 7 with the oscilloscope.