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Lab 5:

Clock Control Module CLKCTRL and Software Delays

Questions:

1. With the -00 optimization, the compiler leaves too many instructions between the CCP_CPU write instruction and the change to the CLKCTRL module. This makes it impossible to modify the CLKCTRL module because the Configuration Change Protection only allows 4 cycles to make changes.
2. For determining the relationship between CLK_CPU and CLK_PER, I set a prescaler of 4 with a clock frequency of 4 MHz for 1 CLK_PER of 1 MHz. Then I toggled a pin at 1/16 of the CLK_CPU frequency. I determined that the relationship was a dependent one, because the toggle frequency was 62.5 kHz, or 1/16 of 1 MHz, rather than 250 kHz, 1/16 of 4 MHz, as would be expected if CLK_PER didn't also affect CLK_CPU.
3. The error was proportional to the delay. For a 52.08333 us delay, I had to use a 48 us delay, for a 104.1666 us delay, I had to use a 99 us delay, and for a 208.333 us delay, I had to use a 201 us delay.